HP 83595A
RF PLUG-IN
(Including Options 002 and 004)

SERIAL NUMBERS

This manual applies directly to HP 83595A RF plug-in having serial number prefix 2718A.

For instruments with serial numbers 2645A and below, refer to Section 7 (Manual Backdating).

For additional information about serial numbers or the Manual Change Supplement, refer to INSTRUMENTS COVERED BY MANUAL in Section 1.

1400 FOUNTAINGROVE PARKWAY, SANTA ROSA, CA 95403 U.S.A.

MANUAL PART NO. 83595-90018
Microfiche Part Number 83595-90020

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HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard instrument product is warranted against defects in material and workmanship for a period of one year from date of delivery, or, in the case of certain major components listed in section six of this Operating and Service manual, for the specified period. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

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HP 83595A RF Plug-In

Section 6. REPLACEABLE PARTS

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SAFETY CONSIDERATIONS

GENERAL

This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation. This product has been designed and tested in accordance with international standards.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual (refer to Table of Contents).

Indicates hazardous voltages.

Indicates earth (ground) terminal.

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

BEFORE APPLYING POWER

Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an autotransformer make sure the common terminal is connected to the neutral (grounded side of the mains supply).

SERVICING

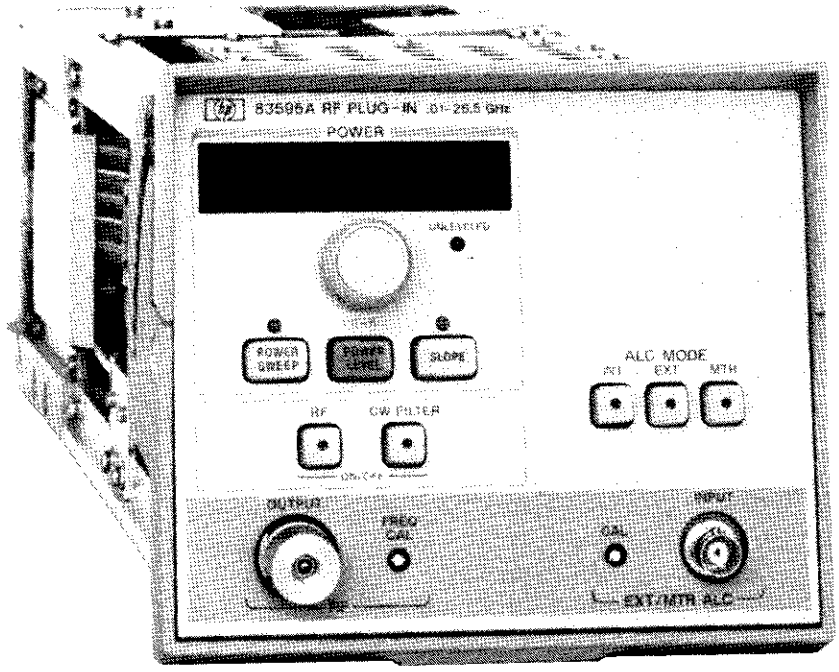
WARNING

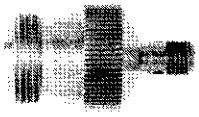
Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from their power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.





Adapter
SMA (f) to TYPE N (f)
(1250-1404)

Figure 1-1. HP 83595A RF Plug-in and Accessory Adapter

Section 1. General Information

INTRODUCTION

This manual contains the information required to install, operate, test, adjust, and service the Hewlett-Packard 83595A RF plug-in, shown in Figure 1-1. This manual is divided into eight major sections:

SECTION 1, GENERAL INFORMATION. This section contains:

- A brief description of the instrument
- Safety considerations
- Specifications
- Supplemental characteristics
- Instrument identification
- Options available
- Accessories available
- Recommended test equipment

SECTION 2, INSTALLATION. This section contains:

- Initial inspection
- Preparation for use
- Storage
- Shipment

SECTION 3, OPERATION. This section contains:

- RF plug-in configuration switch settings
- Frequency reference selection switch settings
- Frequency resolution characteristics in CW and swept frequency modes
- Crystal and power meter leveling instructions
- Front and rear panel features
- Error codes

SECTION 4, PERFORMANCE TESTS. This section contains procedures to verify published HP 83595A specifications.

SECTION 5, ADJUSTMENTS. This section contains procedures to adjust and align the HP 83595A after repair, or if the instrument fails a performance test.

SECTION 6, REPLACEABLE PARTS. This section contains information required to order all replaceable parts and assemblies.

SECTION 7, MANUAL BACKDATING. This section contains information on earlier shipment configurations.

SECTION 8, SERVICE. This section contains:

- Overall instrument block diagram
- Troubleshooting and repair procedures
- Information on each assembly within the instrument

SPECIFICATIONS

Instrument specifications are listed in Table 1-1. These specifications are the performance standards or limits against which the instrument is tested. Table 1-2 lists supplemental performance characteristics, which are not specifications, but are intended to provide additional information useful to your application by giving typical (but not warranted) performance parameters.

Table 1-1. Specifications for HP 83595A Installed in HP 8350 (1 of 2)

FREQUENCY[1]

Specification	Frequency Bands (GHz)					
	0.01 to 2.4	**2.4 to 7.0**	**7.0 to 13.5**	**13.5 to 20.0**	**20.0 to 26.5**	**0.01 to 26.5**
Accuracy (25°C ± 5°C)						
CW Mode	±5 MHz[2]	±5 MHz	±10 MHz	±10 MHz	±12 MHz	———
All Sweep Modes (Sweep time >100 ms)	±15 MHz[2]	±20 MHz	±25 MHz	±30 MHz	±35 MHz	±50 MHz[2]
Frequency Markers (Sweep time ≥100 ms)	±15 MHz[2] ±.5% of sweep width	±20 MHz ±.5% of sweep width	±25 MHz ±.5% of sweep width	±30 MHz ±.5% of sweep width	±35 MHz ±.5% of sweep width	±50 MHz[2] ±.5% of sweep width

POWER OUTPUT[1]

Specification	Frequency Bands (GHz)					
	0.01 to 2.4	**2.4 to 7.0**	**7.0 to 13.5**	**13.5 to 20.0**	**20.0 to 26.5**	**0.01 to 26.5**
Maximum Leveled Output Power[3,4,5] (25°C)	+10 dBm	+10 dBm	+10 dBm	+10 dBm	+4 dBm	+4 dBm
With Option 002	+10 dBm	+8.5 dBm	+8 dBm	+7 dBm	+1 dBm	+1 dBm
Power Level Accuracy[9] (internally leveled)	<±1.5 dB	<±1.3 dB	<±1.3 dB	<±1.4 dB	<±1.7 dB	<±1.8 dB
With Option 002[6] (at 0 dB attenuator step)	<±1.7 dB	<±1.5 dB	<±1.5 dB	<±1.6 dB	<±1.9 dB	<±2.0 dB
Power Sweep[7]						
Calibrated Range[8]	>15 dB	>15 dB	>15 dB	>15 dB	>9 dB	>9 dB
With Option 002	>15 dB	>13.5 dB	>13 dB	>12 dB	>6 dB	>6 dB

POWER VARIATION (at specified Maximum Leveled Power or below)

Specification	Frequency Bands (GHz)					
	0.01 to 2.4	**2.4 to 7.0**	**7.0 to 13.5**	**13.5 to 20.0**	**20.0 to 26.5**	**0.01 to 26.5**
Internally Leveled	±0.9 dB	±0.7 dB	±0.7 dB	±0.8 dB	±0.9 dB	±1.0 dB

FREQUENCY STABILITY

With 10 dB Power Level Change	±200 kHz	±200 kHz	±400 kHz	±600 kHz	±800 kHz	±800 kHz
With 3:1 Load SWR	±100 kHz	±100 kHz	±200 kHz	±300 kHz	±400 kHz	±400 kHz
Residual FM, Peak (10 Hz to 10 kHz bandwidth) (CW Mode with CW Filter)	<5 kHz	<5 kHz	<7 kHz	<9 kHz	<12 kHz	———
Spurious Signals at specified maximum leveled power						
Harmonics or Subharmonics (in dB below carrier)	>25 dB	>25 dB	>25 dB	>25 dB	>20 dB	>20 dB

Table 1-1. Specifications for HP 83595A Installed in HP 8350 (2 of 2)

MODULATION[1]

External FM

Maximum Deviations for Modulation Frequencies		
Modulation Frequencies	**Cross-Over Coupled**	**Direct Coupled**
DC to 100 Hz	±75 MHz	±12 MHz
100 Hz to 1 MHz	±7 MHz	±7 MHz
1 MHz to 2 MHz	±5 MHz	±5 MHz
2 MHz to 10 MHz	±1 MHz	±1 MHz

External AM
Maximum Input: 15V

Internal AM
Selectable (by internal jumper in HP 8350) to 1 kHz or 27.8 kHz square-wave modulation.

On/Off Ratio: ≥30 dB below specified maximum leveled power

Symmetry: 40/60

Minimum Settable Power: −5 dBm
With Option 002: −60 dBm

Attenuator Accuracy (±dB referenced from the 0 dB setting):

Frequency Range GHz	Attenuator Setting (dB)										
	5	10	15	20	25	30	35	40	45	50	55
0.01 to 12.4	0.4	0.6	0.7	0.7	0.9	0.9	1.8	1.8	2.0	2.0	2.2
12.4 to 18.0	0.5	0.7	0.9	0.9	1.2	1.2	2.0	2.0	2.3	2.3	2.5
18.0 to 26.50	0.7	1.0	2.5	2.5	3.0	3.0	4.2	4.2	4.4	4.4	4.6

GENERAL SPECIFICATIONS[1]

Minimum Sweep Time (over full band): 30 ms

Minimum Sweep Time (over single band): 10 ms

Band Switch Points: internal band switch points at approximately 2.4 GHz, 7.0 GHz, 13.5 GHz, and 20.0 GHz

RF Ouput Connector: precision 3.5 mm (m)

1. Unless otherwise noted, all specifications are at the RF OUTPUT connector and at 0° to 55°C.
2. Accuracy when calibrated with the FREQ CAL adjustment.
3. For temperatures greater than 25°C, maximum leveled output power typically degrades 0.1 dB/°C.
4. When RF Output is peaked with PEAK control.
5. 0.5 dB lower for Option 004.
6. Atttenuator switch points are every 5 dB starting at −5 dBm indicated power.
7. Power Sweep and slope compensation total must not exceed the specified power sweep calibrated range.
8. With Option 002, in power sweep or slope functions, power can exceed the attenuator step by the amount that the Power Sweep calibrated range exceeds 5 dB (i.e., if the calibrated range is 7 dB, power can exceed the attenuator step by 2 dB).
9. Includes power level variations.

Table 1-2. Supplemental Characteristics for HP 83595A Installed in HP 8350 (1 of 2)

NOTE: Values in this table are not specifications, but are typical characteristics included for user information.

FREQUENCY CHARACTERISTICS[1]

Characteristic	Frequency Bands (GHz)					
	0.01 to 2.4	2.4 to 7.0	7.0 to 13.5	13.5 to 20.0	20.0 to 26.5	0.01 to 26.5
Accuracy (25°C ±5°C)[2]						
CW Mode Typically	±2 MHz	±2 MHz	±3 MHz	±4 MHz	±5 MHz	±7 MHz
Manual Sweep	≤15 MHz	≤30 MHz	≤30 MHz	≤30 MHz	≤100 MHz	≤150 MHz
All Sweep Modes (sweep time 10 ms to 100 ms)	≤±5 MHz	≤±6 MHz	≤±8 MHz	≤±10 MHz	≤±35 MHz	≤±50 MHz
Sweep Mode Linearity[3]	≤±2 MHz	≤±2 MHz	≤±4 MHz	≤±6 MHz	≤±10 MHz	≤±15 MHz
Stability with Temperature	±200 kHz/°C	±200 kHz/°C	±400 kHz/°C	±600 kHz/°C	±800 kHz/°C	±800 kHz/°C
With Time (in a 10 minute period after one hour warmup at the same frequency setting):	<±100 kHz	<±100 kHz	<±200 kHz	<±300 kHz	<±400 kHz	<±400 kHz

OUTPUT CHARACTERISTICS[1]

Power Output

Resolution (displayed): 0.1 dB

Resolution (power): ±0.01 dB

Stability with Temperature (at specified maximum leveled power): ±0.1 dB/°C

POWER VARIATION (at specified maximum leveled power or below)

Characteristic	Frequency Bands (GHz)					
	0.01 to 2.4	2.4 to 7.0	7.0 to 13.5	13.5 to 20.0	20.0 to 26.5	0.01 to 26.5
Externally Leveled[4]						
Negative Crystal Detector[5] (Sweep time >100 ms)	±0.2 dB	±0.2 dB	±0.2 dB	±0.2 dB	±0.2 dB	±0.2 dB
Power Meter[6]	±0.2 dB	±0.2 dB	±0.2 dB	±0.2 dB	±0.2 dB	±0.2 dB
Residual AM in 100 kHz Bandwidth (in dB below carrier and at specified maximum leveled power)	≥50 dB	≥50 dB	≥50 dB	≥50 dB	≥50 dB	≥50 dB
Spurious Signals (in dB below carrier and at specified maximum leveled power)						
Harmonics and Subharmonics	>35 dB	>40 dB	>35 dB	>35 dB	>35 dB	>35 dB
Non Harmonics typically	>40 dB	>55 dB	>55 dB	>55 dB	>40 dB	>40 dB
Output SWR (internally leveled)	<1.9	<1.9	<1.9	<1.9	<1.9	<1.9
With Option 002	<2.0	<2.0	<2.0	<2.0	<2.2	<2.2

Table 1-2. Supplemental Characteristics for HP 83595A Installed in HP 8350 (2 of 2)

Impedance: 50 Ohms

Power Sweep[7]:

Accuracy (including linearity): typically ±1.5 dB
Resolution (displayed): 0.01 dB

Slope Compensation[7]

Linearity: typically <0.2 dB

Calibrated Range[8]: up to 5 dB/GHz; up to 15 dB for full sweep range

Resolution (displayed): 0.01 dB/GHz

MODULATION CHARACTERISTICS[1]

External AM

Frequency Response: 100 kHz

Input Impedance: 10k Ohm

Range of Amplitude Control: 15 dB

Sensitivity: Typically 1 dB/V

Pulse In

TTL compatible: logic high=RF on, logic low=RF off
0.01 to 26.5 GHz: Square-wave modulation up to 30 kHz.
0.01 to 7.0 GHz:
Rise/Fall Time: typically 50 ns
Minimum Pulse Width:
Leveled: typically 5 μs
Unleveled Power level set to +20 dBm: 100 ns

External FM

Frequency Response (DC to 2 MHz): ±3 dB

Sensitivity (switch selectable) Typically −20 MHz/V (FM Mode)
Typically −6 MHz/V (Phase-Lock Mode)
Input Impedance: 2000 Ohms nominal

GENERAL CHARACTERISTICS[1]

Frequency Reference Output: selectable 1V/GHz ±25 mV (0.01 to 18 GHz) or 0.5V/GHz ±25 mV (0.01 to 20 GHz) rear panel BNC output.

Auxiliary Output: rear panel 2.3 to 7 GHz fundamental oscillator output, nominally 0 dBm.

Weight: Net 6.0 kg (13.2 lb.); Shipping 9.2 kg (20 lb.)

1. Unless otherwise noted, all characteristics are at the RF OUTPUT connector and at 0° to 55°C.
2. Accuracy when calibrated with the FREQ CAL adjustment.
3. With respect to the SWEEP OUT voltage.
4. Discontinuity at 2.4 GHz bandswitch point is typically <0.25 dB.
5. Excludes coupler and detector variation. Crystal detector output should be between −10 mV and −200 mV at specified maximum leveled power.
6. Use HP 432A/B/C, HP 436A, or HP 438A Power Meters. Sweep time 100 seconds, typically ≥5 seconds/GHz but not ≤10 seconds.
7. Power Sweep and Slope compensation must not exceed the specified power sweep calibrated range.
8. With Option 002, in power sweep or slope functions, power can exceed the attenuator step by the amount that the Power Sweep calibrated range exceeds 10 dB (e.g., if the calibrated range is 12 dB, power can exceed the attenuator step by 2 dB).

SAFETY CONSIDERATIONS

Become familiar with all safety instructions in this manual before you use the HP 83595A RF plug-in. This product was designed and tested in accordance with international standards.

Manufacturer's Declaration

NOTE

This is to certify that this product meets the radio frequency interference requirements of Directive FTZ 1046/1984. The German Bundespost has been notified that this equipment was put into circulation and has been granted the right to check the product type for compliance with these requirements.

Note: If test and measurement equipment is operated with unshielded cables and/or used for measurements on open set-ups, the user must insure that under these operating conditions, the radio frequency interference limits are met at the border of his premises.

Model HP 83595A

NOTE

Hiermit wird bescheinigt, dass dieses Gerät/System in Übereinstimmung mit den Bestimmungen von Postverfügung 1046/84 funkentstört ist.

Der Deutschen Bundespost wurde das Inverkehrbringen dieses Gerätes/Systems angezeigt und die Berechtigung zur Überprüfung der Serie auf Einhaltung der Bestimmungen eingeräumt.

Zusatzinformation für Mess- und Testgeräte:

Werden Mess- und Testgeräte mit ungeschirmten Kabeln und/oder in offenen Messaufbauten verwendet, so ist vom Betreiber sicherzustellen, dass die Funk-Entstörbestimmungen unter Betriebsbedingungen an seiner Grundstücksgrenze eingehalten werden.

Safety Symbols

WARNING

This indicates a personal hazard. **WARNING** calls attention to a procedure, practice, etc., that, if not performed correctly, can cause personal injury. Do not continue past a **WARNING** until you fully understand and meet the stated conditions.

CAUTION

This indicates a mechanical or electrical hazard. **CAUTION** calls attention to an operating procedure, practice, etc., that, if not correctly performed or adhered to, can cause damage to (or destruction of) part or all of the instrument. Do not continue past a **CAUTION** until you fully understand and meet the stated conditions.

INSTRUMENTS COVERED BY THIS MANUAL

Attached to the rear panel of the HP 83595A is a serial number plate (see Figure 1-2). The serial number is in two parts:

1. First four digits followed by a letter comprise the serial number prefix.
2. The last five digits form a sequential suffix, unique to each instrument.

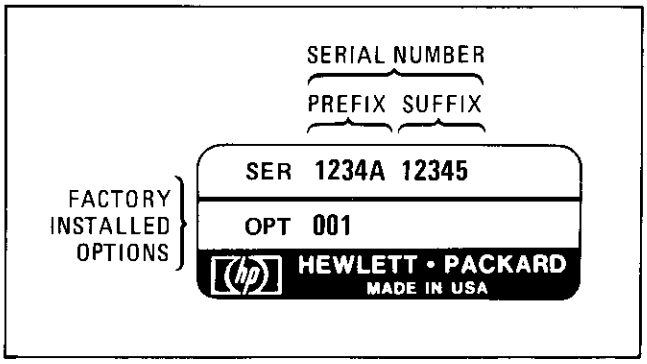


Figure 1-2. Typical Serial Number Plate

The contents of this manual apply directly to instruments having the same serial number prefix as those listed on the title page, under SERIAL NUMBER.

An instrument manufactured after the printing of this manual may have a serial prefix that is not listed on the title page. An unlisted serial prefix indicates that the instrument is different from those documented in this manual. The manual for the instrument is supplied with a manual changes supplement that contains information documenting the differences.

In addition to change information, the supplement may contain replacement information that applies to all instruments, regardless of their serial number.

To keep this manual as current as possible, request the latest manual changes supplement (HP Part No. 83595-90021). The supplement for this manual is keyed to its print date and part number, which appear on the title page. Complimentary copies of the supplement are available from your local Hewlett-Packard office.

ORDERING MANUAL/MICROFICHE

On the title page of this manual is a manual part number and a microfiche part number. Both can be used to order extra copies of this manual.

Microfiche are 10 X 15 cm (4 X 6 in) microfilm transparencies. Each microfiche contains reduced photocopies of the manual pages and the latest manual changes supplement.

The manual part number also appears on the back cover, in the lower left hand corner.

DESCRIPTION

The HP 83595A is an RF plug-in designed to be used with the HP 8350 sweep oscillator. The HP 83595A covers the frequency range of 0.01 to 26.5 GHz either in a single 0.01 to 26.5 GHz sweep, or in four single bands:

Band 0: 0.1 to 2.4 GHz
Band 1: 2.3 to 7.0 GHz
Band 2: 6.9 to 13.5 GHz
Band 3: 13.4 to 20.0 GHz
Band 4: 19.9 to 26.5 GHz

HP 83595A maximum leveled power is +10 dBm from 0.01 to 20.0 GHz, and +4 dBm from 20.0 to 26.5 GHz.

OPTIONS

Option 002 – 55 dB Attenuator

Option 002 instruments have a digitally controlled attenuator, positioned just before the RF output. Up to 55 dB of attenuation (in 5 dB steps) is automatically selected as required, to obtain the output power indicated on the HP 83595A.

Option 004 – Rear Panel RF Output

On Option 004 instruments, the Type-N RF output connector and the BNC EXT/MTR ALC input connector are on the rear panel instead of the front panel.

Option W30 – Extended Service

Option W30 adds two additional years of return-to-HP hardware support, to follow the first year of warranty. Option W30 can be ordered at the time of sale only. Instruments ordered with Option W30 are identified on the serial number label, or on a special identification label supplied with the instrument.

Option 910 – Extra Operating and Service Manual

A standard instrument is supplied with one operating and service manual. Option 910 provides an additional operating and service manual. To order extra operating and service manuals after initial shipment, order by the manual part number listed on the title page and the rear cover of this manual.

EQUIPMENT REQUIRED BUT NOT SUPPLIED

For a complete sweep oscillator unit, the HP 83595A RF plug-in must be installed in an HP 8350 sweep oscillator (see Section 2).

EQUIPMENT AVAILABLE

Service Accessories

A service accessory kit is available to facilitate servicing the HP 83595A and the HP 8350. For a complete list of available service accessories, see Table 1-3.

Power Meters and Crystal Detectors

An HP 432A/B/C, 436A, or 438A power meter; or a negative polarity output crystal detector can be used to externally level the HP 83595A RF output. See Section 3 for detailed information.

HP 8756A/8757A Scalar Network Analyzer

The HP 8350/83595A combination is compatible with the HP 8756A and 8757A scalar network analyzers.

HP 8510A Vector Network Analyzer

The HP 8350/83595A combination is compatible with the HP 8510A vector network analyzer.

Millimeter-Wave Source Modules

The HP 8350/83595A combination is compatible with the HP 83550 series millimeter-wave source modules, when used with an HP 8349B microwave amplifier.

RECOMMENDED TEST EQUIPMENT

Table 1-4 lists the equipment required to test and adjust the HP 83595A. Other equipment may be substituted if it meets or exceeds the indicated critical specifications.

Table 1-3. Service Accessories Available

Name	HP Part Number	Description
44-pin printed circuit board extender	08350-60031*	Extends printed circuit boards
RF plug-in extender cables	08350-60034* 08350-60035*	Extends RF plug-in Interface connector (P2) Extends RF plug-in Power Supply Interface connector (P1)
Adjustment tool	8830-0024	Fits miniature adjustment slot on potentiometers
Wrenches	08555-20097 8710-0946	5/16 inch slotted box/open end 15/64 inch open end
Service cables	8120-1578	18 inch Coax with SMA (m) connector on each end
Adapters	1250-1743 1250-1750 1250-1404 1250-1158 1250-1744 1250-1745 1250-1748 1250-1749	3.5 mm (m) to Type-N (m) 3.5 mm (m) to Type-N (f) Type-N (f) to SMA (f) SMA (f) to SMA (f) 3.5 mm (f) to Type-N (m) 3.5 mm (f) to Type-N (f) 3.5 mm (m) to 3.5 mm (m) 3.5 mm (f) to 3.5 mm (f)
Hex Balldriver	8710-0523*	Removes HP 8350 front panel hold down plate hex screws.
IC test clip	1400-0734* 1400-0979* 1400-1097*	16-pin IC test clip 20-pin IC test clip 40-pin IC test clip

*These items are included in a Service Accessories Kit, HP Part No. 08350-60020. Also included is HP Part No. 08350-60031, 44-pin printed circuit board extender (2 each).

Table 1-4. Recommended Test Equipment (1 of 2)

Instrument	Critical Specifications	Recommended Model	Use*
Sweep Oscillator	No substitute	HP 8350	P, A, T
Digital Voltmeter (DVM)	Range: −50V to +50V Accuracy: ±0.01% Input Impedance: ≥10M Ohms Computing Math	HP 3456A	A, T
Scalar Network Analyzer	Capable of both modulated and unmodulated (AC/DC detection) Transmission Measurements Power Resolution: ≤0.25 dB	HP 8757A	A, T
Detector	Compatible with Scalar Network Analyzer Frequency Range: 0.01 to 26.5 GHz Power Range: −20 +10 dBm	HP 85025B	A
Oscilloscope Probe	1:1 General Purpose Probe 10:1 Standard Divider	HP 10009B HP 10016B	A
Frequency Counter	Frequency Range: 0.01 to 26.5 GHz Input Impedance: 50 Ohms Resolution: ≤1 MHz	HP 5343A	P

Table 1-4. Recommended Test Equipment (2 of 2)

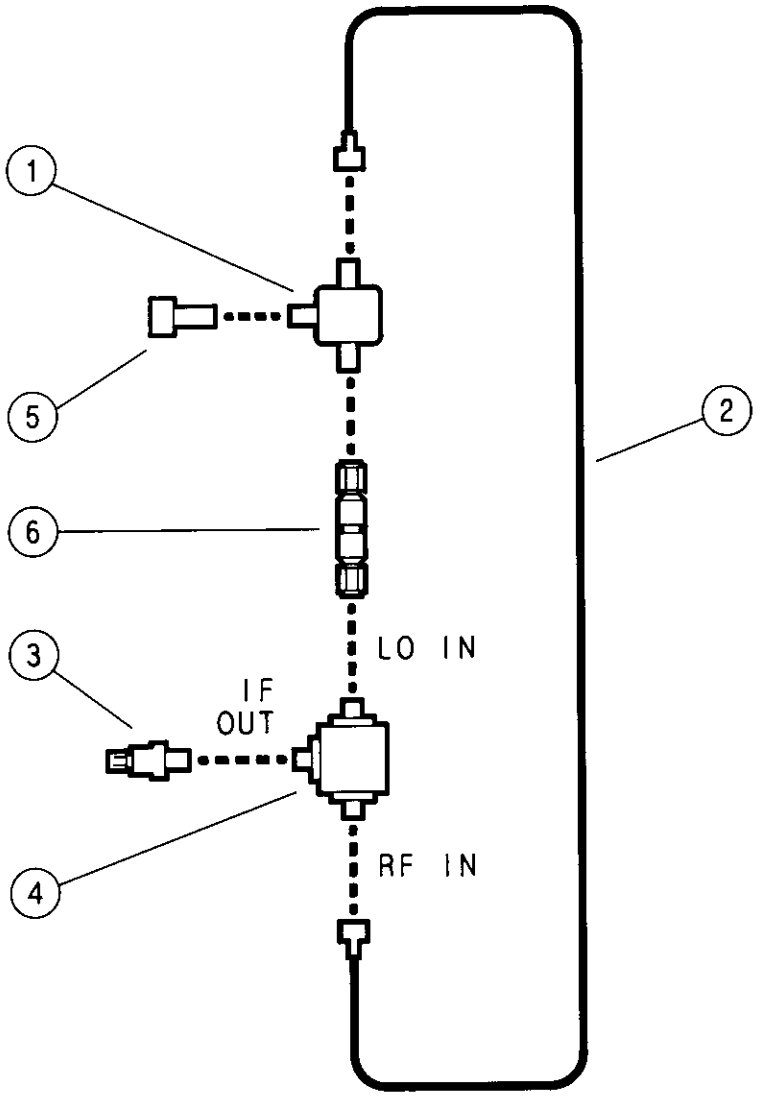
Instrument	Critical Specifications	Recommended Model	Use*
Spectrum Analyzer	Frequency Range: 0.01 to 26.5 GHz Residual FM: <100 Hz	HP 8566B	P, A, T
Resistor	1%, 0.125W	HP Part No. 0757-0416	A
Low Pass Filter	Cutoff Frequency: 6.8 GHz Impedance: 50 Ohms	HP 11684A	A
Function Generator	Frequency Range: 0.1 Hz to 10 MHz Sinewave and squarewave output Output Level: 10V p-p into 50 Ohms Output Level Flatness: ≤ ±3% from 10 Hz to 100 kHz ≤ ±10% from 100 kHz to 10 MHz	HP 3325A	P, A, T
Power Meter	Power Range: +20 to −10 dBm	HP 436A	P, A, T
Power Splitter	Frequency Range: 0.01 to 26.5 GHz Maximum Input Power: +27 dBm	HP 11667B	P, A
Power Sensor	Frequency Range: 0.05 to 26.5 GHz Maximum SWR: 1.25:1	HP 8485A	P, A, T
Crystal Detector	Frequency Response: 0.01 to 26.5 GHz Maximum Input Power: 200 mW	HP 8473C	P, A, T
Attenuator	Frequency Range: 0.01 to 26.5 GHz Maximum Input Power: +20 dBm Attenuation: 10 dB ±0.5 dB 3 dB ±0.5 dB 6 dB ±0.5 dB 20 dB ±0.5 dB	 HP 8493C Option 010 HP 8493C Option 003 HP 8493C Option 006 HP 8493C Option 002	P, A
16 dB Coupler	Frequency Range: 0.01 to 26.5 GHz Nominal Coupling: ≥22 dB Maximum Coupling Variation: ±1 dB Minimum Directivity: 26 dB	HP Part No. 0955-0125	
Oscilloscope	Dual Channel Bandwidth: DC to 100 MHz Vertical Sensitivity: ≤5m V/DIV Horizontal Sweep Rate: ≤0.1μS/DIV External Sweep Capability	HP 1741A	P, A, T
Spectrum Analyzer	Frequency Range: 0.01 to 12.4 GHz Residual FM: <100 Hz	HP 8566B	
Step Attenuator	Frequency Range: 0.01 to 26.5 GHz Incremental Attenuation: 0 to 70 dB in 10 dB steps Calibration Accuracy: ≤ ±0.1 at all steps	HP 8495D Option 890	P
Short	Frequency Range: 0.01 to 26.5 GHz Impedance: 50 ±1.5 Ohms	HP 11565A	P
50 Ohm Feedthru Termination	Type-N, 50 ±0.5 Ohms	HP 10100C	P
Delay Line Discriminator	Refer to Figure 1-3.		P
Measuring Receiver	Range: +30 dBm (1W) to −20 dBm (19μW) Input: SWR <1.15	HP 8902A	P
Frequency Meter	0.96 to 4.20 GHz 3.7 to 12.4 GHz 12.4 to 18 GHz 18.0 to 26.5 GHz	HP 536A HP 537A HP P532A HP K532A	P

*P = Performance Test; A = Adjustments; T = Troubleshooting

Table 1-5. Adapters and Cables

Name	HP Part Number	Description
Adapter	1250-1744*	Type-N (m) to 3.5 mm (f)
Adapter	1250-1533	Type-N (m) to BNC (m)
Cables (2)	08350-60039	SMB (f) to BNC (m)
Adapter	P281C Opt. 013	Waveguide to Coax (12.4 to 18.0 GHz)
Adapter	K281C	Waveguide to Coax (18.0 to 26.5 GHz)
Adapter	1250-0780	BNC (f) to Type-N (m)
Adapter	1250-1534	BNC (m) to Type-N (f)
Adapter	1250-1743*	Type-N (m) to 3.5 mm (m)
Adapter	1250-1781	BNC Tee
Adapter	1250-1745*	Type-N (f) to 3.5 mm (f)
Adapter	1250-1749	3.5 mm (f) to 3.5 mm (f)

*These items are included in Table 1-3, Service Accessories Available.



Item	Description	HP Part Number
1	Power Splitter	HP 11667B
2	Delay Line: 23.5 cm (9.2 inches) in length, SMA male connectors	83550-20034
3	Adapter: BNC (f) to SMA (m)	1250-1200
4	Mixer: Doubled Balanced	
	RHG Electronics Part No. DMS 1-26 RGH Electronics, Laboratories, Inc. Deer Park, NY 11729	0955-0307
5	Adapter: Type-N (m) to 3.5 mm (m)	1250-1743
6	Adapter: 3.5 mm (m) to 3.5 mm (m)	1250-1748

Figure 1-3. Delay Line Discriminator

Section 2. Installation

INTRODUCTION

Along with HP 83595A installation instructions, this section provides information on:

- Initial inspection.
- Damage claims.
- Preparation for use.
- Packaging.
- Storage.
- Shipment.

INITIAL INSPECTION

If the shipping container or cushioning material is damaged, keep it until the contents of the shipment are checked for completeness, and the instrument is checked both mechanically and electrically.

Procedures for checking electrical performance are given in Section 4. If the plug-in and mainframe do not pass the electrical performance tests, refer to the troubleshooting paragraphs located in Section 8.

Notify your nearest Hewlett-Packard office if any of the following conditions exist:

- The instrument does not pass the performance tests and, using the troubleshooting procedures in Section 8, you cannot correct the problem.
- The instrument does not pass the performance tests and you do not wish to troubleshoot the instrument yourself.
- The shipping contents are incomplete.
- There is mechanical damage or defect.

Notify the carrier if the shipping container is damaged or if the cushioning material shows signs of stress. Keep all shipping materials for the carrier's inspection. Hewlett-Packard will arrange for repair or replacement without waiting for a claim settlement.

PREPARATION FOR USE

Power Requirements

When properly installed, the HP 83595A RF plug-in receives all power from the HP 8350 sweep oscillator, through the rear panel interface connectors.

Configuration Switch

The RF plug-in configuration switch (A3S1) is an 8-section multiple switch located on the HP 83595A A3 digital interface assembly. Six of the eight sections correspond to separate RF plug-in functions, and can be modified, as required, for your application. Refer to Section 3, for a complete description of the configuration switch and instructions on how to set each function.

Interconnections

The HP 83595A has two rear panel interconnections to the HP 8350 sweep oscillator:

- The power supply interface connector (P1)
- The RF plug-in interface connector (P2)

Figures 2-1 and 2-2 provide complete listings of pins and associated signals for these connectors.

Mating Connectors

Table 2-1 lists:

- All HP 83595A externally mounted connectors.
- The HP part number for each connector.
- An industry identification.
- The HP part number of a mating connector.
- The part number of an alternate source for the mating connector.

Table 2-1. HP 83595A Mating Connectors

HP 83595A Connector			Mating Connector	
Connector Name	**HP Part No.**	**Industry Identification**	**HP Part No.**	**Alternate Source**
J1 RF OUTPUT	5061-5304	Type-N (f)	1250-0882	Specialty Connector 25-P117-2
J2 EXT/MTR ALC INPUT	1250-0118	BNC (f)	1250-0256	Specialty Connector 25-P118-1
J3 AUX OUTPUT	5061-5304	Type-N (f)	1250-0882	Specialty Connector 25-P117-2
J4 PULSE IN	1250-0118	BNC (f)	1250-0256	Specialty Connector 25-P118-1
J5 1.0/0.5 V/GHz	1250-0118	BNC (f)	1250-0256	Specialty Connector 25-P118-1
P1 POWER SUPPLY INTERFACE	Part of W28 Not Separately Replaceable	N/A	83525-60024	N/A
P2 RF PLUG-IN INTERFACE	Part of W29 Not Separately Replaceable	N/A	83525-60056	N/A

Operating Environment

The HP 83595A RF plug-in operates within the following environmental limits:

Temperature: 0° to +55°C (+32° to +131°F)

Humidity: 5% to 80% relative at +25° to +40°C (+77° to +105°F).

Provide protection from temperature extremes. Condensation can occur within the instrument if it is exposed to temperature extremes or to higher humidity levels.

Altitude: Up to 4572m (15,000 ft).

Cooling: When the HP 83595A is properly installed in the HP 8350 sweep oscillator, the RF plug-in obtains all its airflow cooling by forced ventilation from the HP 8350 fan.

A diagram of the various airflow cooling paths within the sweep oscillator is given in the *HP 8350 Sweep Oscillator Operating and Service Manual*, Section 2. Ensure that all airflow passages in both instruments are clear before installing the RF plug-in in the sweep oscillator.

Installation Instructions

To be functional, the HP 83595A RF plug-in must be installed in an HP 8350 sweep oscillator:

1. Turn the HP 8350 off.
2. To prevent damage, remove all connectors and accessories from the HP 83595A front and rear panel connectors.
3. Position the plug-in latching handle in the fully raised position. The handle should raise easily and hold in that position by spring tension.
4. Ensure that the HP 8350 plug-in channel is clear; align the RF plug-in in the channel and slide it carefully into place. It should slide back easily, without binding.
5. The latching handle slot engages with the locking pin just before the plug-in is fully seated in position.
6. Press the latching handle downward, while still pushing in on the RF plug-in, until the handle is fully latched (down) and the plug-in front panel is aligned with the sweep oscillator front panel.

STORAGE AND SHIPMENT

Environment

The instrument may be stored or shipped in environments within the following limits:

Temperature: -40° to +75°C (−40° to +167°F).

Humidity: 5% to 95% relative at 0° to +40°C (+32° to +105°F).

Protect the instrument from temperature extremes, which can cause condensation in the instrument.

Altitude: Up to 15240m (50,000 ft).

Packaging

Containers and materials identical to those used in factory packaging are available through your Hewlett-Packard office (see Figure 2-3). If, however, you choose to package the instrument with commercially available materials, follow these instructions:

1. Wrap the instrument in heavy paper.
2. Use a strong shipping container. A double-wall carton made of 159 kg (350 lb) test material is adequate.
3. Use shock absorbing material, a 76 to 102 mm (3 to 4 in) layer, around all sides of the instrument to provide a firm cushion and to prevent movement inside the container.
4. Seal the shipping container securely.
5. Mark the shipping container **FRAGILE**.

Returning Instrument for Service

If you ship the instrument to a Hewlett-Packard office or service center, please include a blue service tag (found at the end of Section 3), on which you provide the following information:

1. Your company name and address.
2. A technical contact person within your company, and their complete phone number.
3. The complete model and serial number of the instrument.
4. The type of service required.
5. Any other information that may expedite service.

When making inquiries, either by correspondence or by telephone, please refer to the instrument by model number and full serial number.

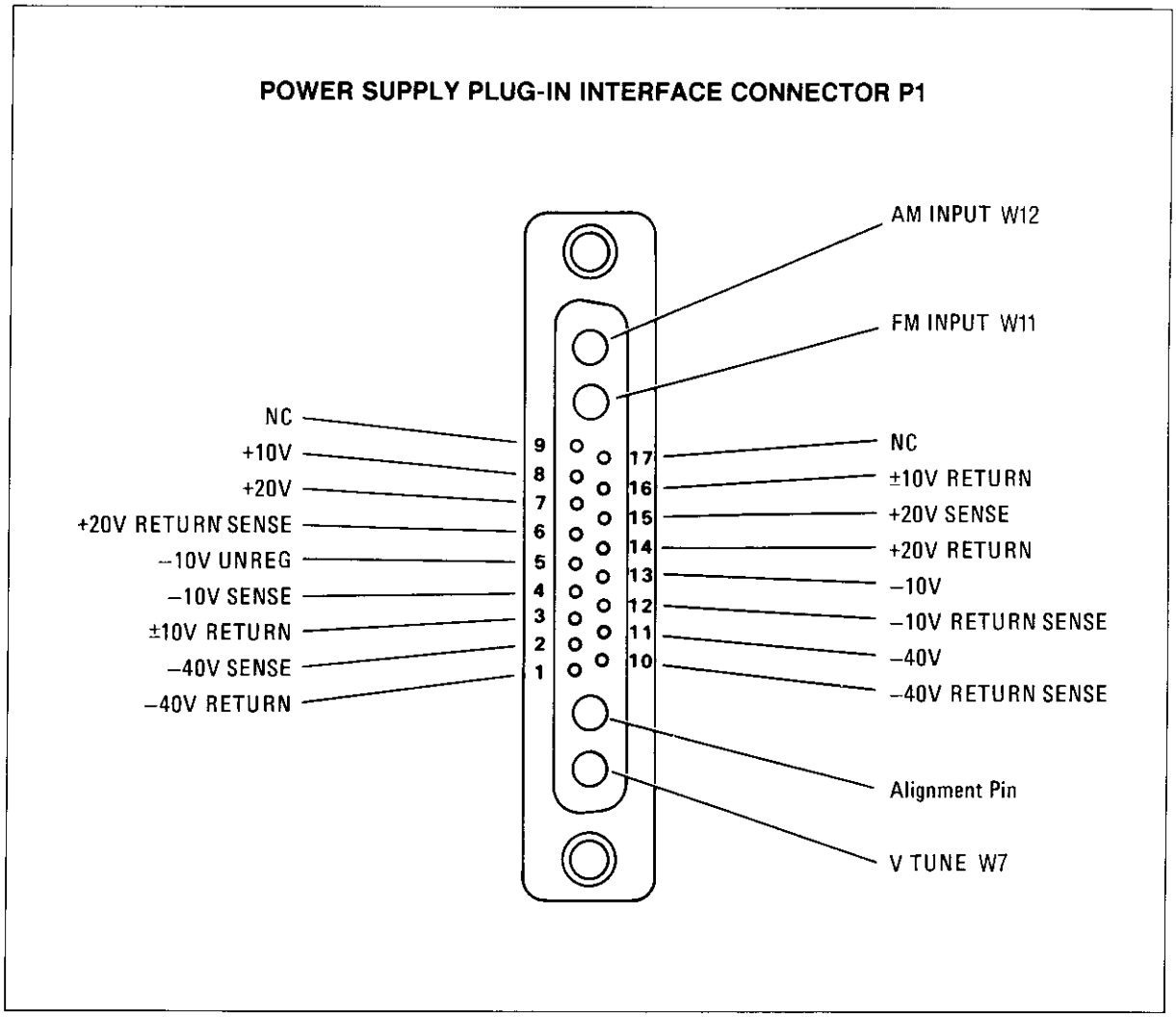


Figure 2-1. Interface Signals on Rear Panel Connector P1

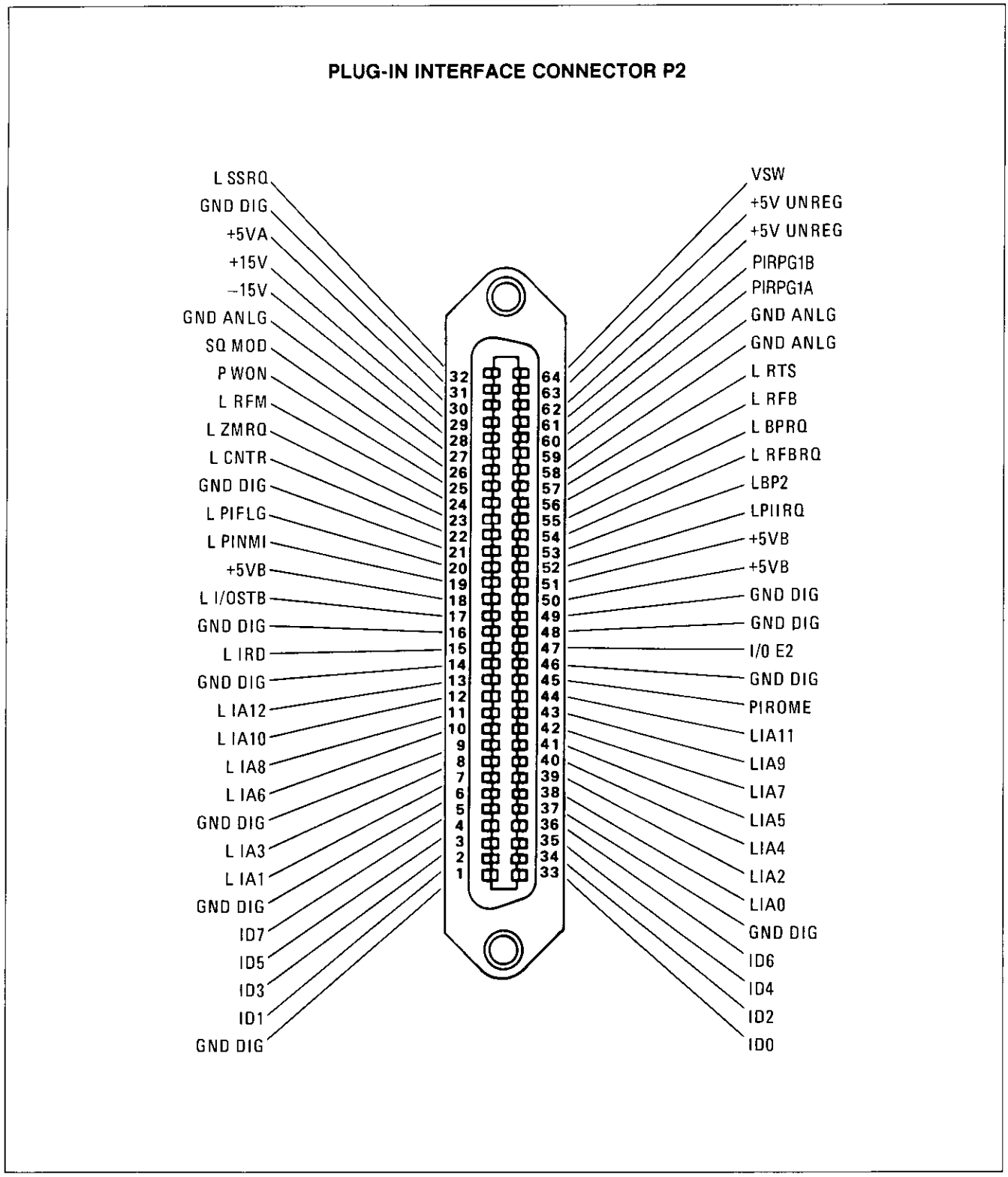
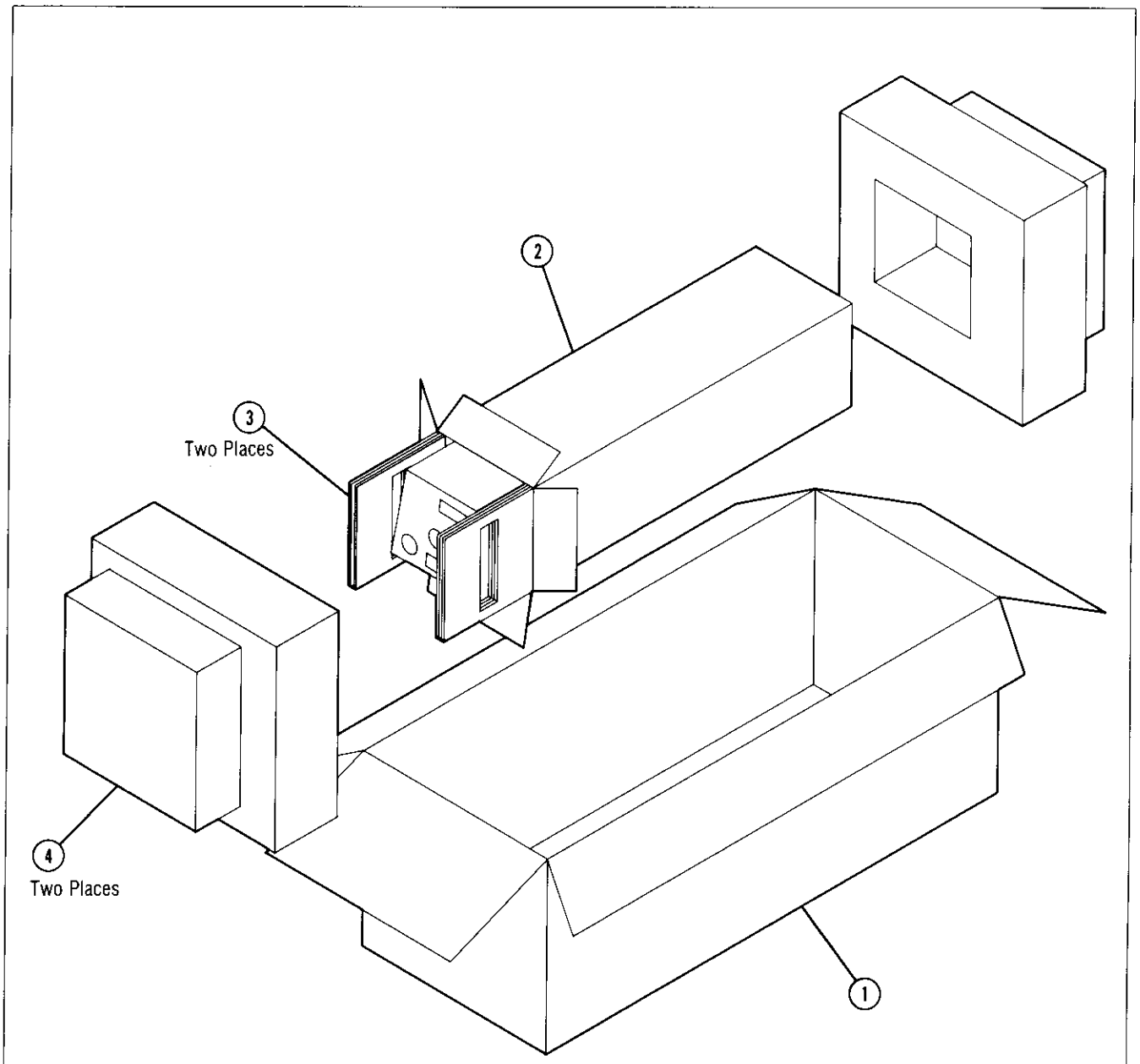


Figure 2-2. Interface Signals on Rear Panel Connector P2 (Front View)



Item	Quantity	HP Part Number	C D	Description
1	1	9211-3515	6	Outer Carton
2	1	9211-3514	5	Inner Carton
3	2	9220-3409	6	Side Pads - Corrugated Cardboard
4	2	9220-3406	3	Foam Pads
Not Shown	1	9222-0352	6	Poly Bag - to cover instrument

Figure 2-3. Packaging for Shipment Using Factory Packaging Materials

Section 3. Operation

INTRODUCTION

This section is divided into four major sections:

OPERATING CHARACTERISTICS explains the bandswitching and frequency resolution characteristics in CW and swept modes.

FRONT AND REAR PANEL FEATURES.

OPERATING INSTRUCTIONS provides information on:

- RF plug-in configuration switch.
- Frequency reference selection switch.
- Operator's checks.
- Millimeter-wave applications.
- Front panel frequency calibration.
- RF output power peaking.
- Internal, crystal detector, and power meter leveling.
- External FM and AM modulation.
- RF power control.
- Option 002 step attenuator.
- Alternate sweep mode.
- HP-IB
- Firmware revision number.
- Phase-Lock Operation.

OPERATOR'S MAINTENANCE includes information on:

- Plug-in error codes
- Fuses
- Service tags

OPERATING CHARACTERISTICS

BANDSWITCHING

HP 83595A provides an RF output of 0.01 to 26.5 GHz in four bands. When you sweep a range of frequencies larger than a single band, the switching between these bands is done automatically. Figure 3-1 illustrates the bandswitching points in the sequential and single band sweep modes. Note that if you select sweep frequencies carefully, you can avoid potential problems associated with bandswitching such as harmonics, sweep time, stability, or switching discontinuities.

If your application requires a large frequency range (over two or more bandswitch points), the minimum recommended frequency sweep time is 100 ms. This allows enough time for the bandswitch operation and for fundamental oscillator settling time. The time required to switch from one frequency band to another is fixed (approximately 15 ms); therefore, SWEEP TIME indicates only the time of the actual frequency sweep. As the sweep time is reduced (to a minimum of 10 ms), the bandswitch time becomes significant with respect to the actual frequency sweep time.

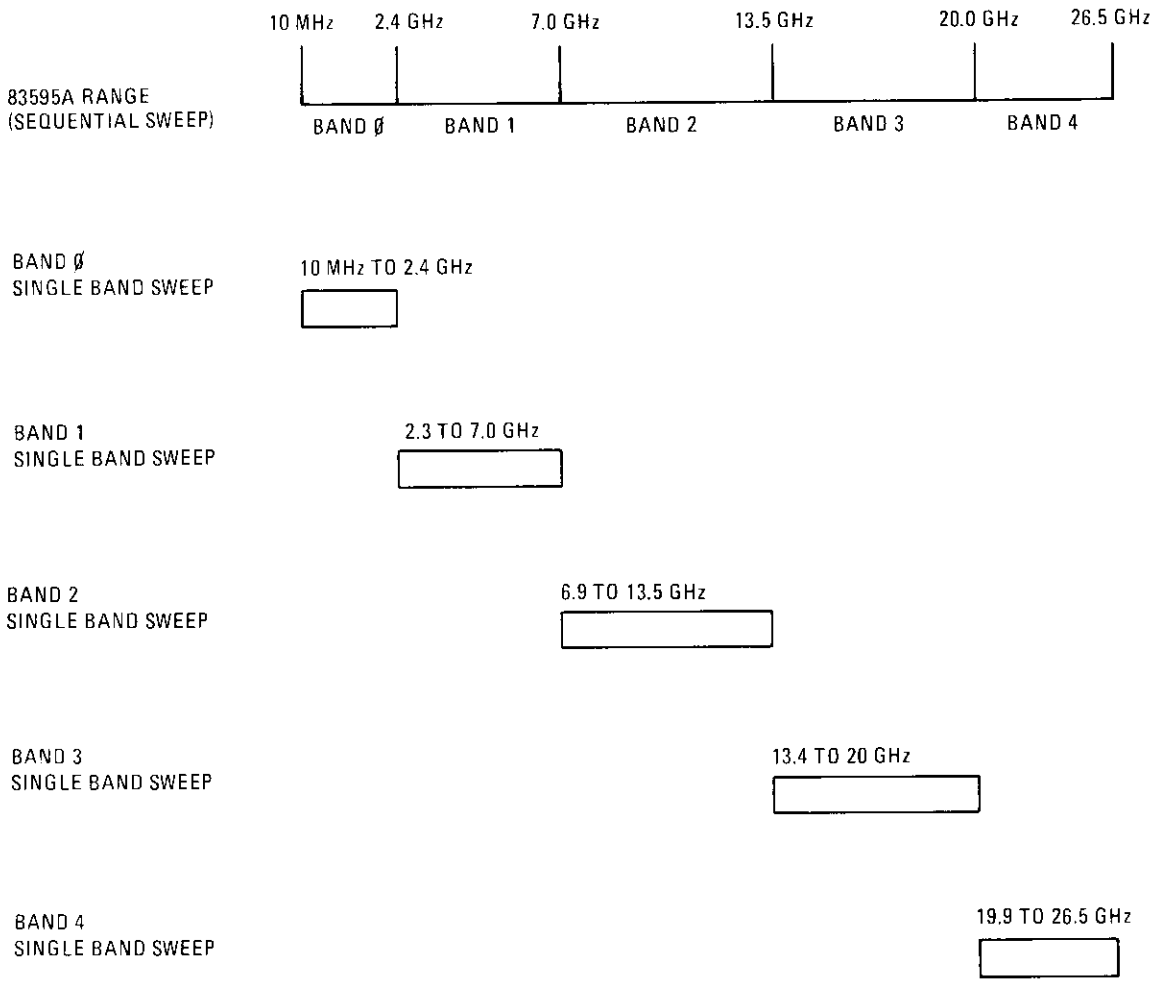


Figure 3-1. Bandswitching in Sequential and Single Band Sweep Modes

FREQUENCY RESOLUTION

Two areas relating to frequency resolution must be considered; these are input resolution and displayed resolution. Input resolution refers to the number of bits (8 bits = 256 points) used in the HP 8350's digital to analog converters (DACs) to generate the tuning voltage for a particular mode of operation. Table 3-1 cross references input resolution with each DAC used. Displayed frequency resolution refers to the number of digits displayed on the HP 8350 FREQUENCY displays.

Input Resolution

Figure 3-1 is a simplified block diagram of the frequency tuning circuits in the HP 8350. The net tuning voltage results from the summation of the three DAC outputs. With this DAC configuration the START/STOP sweep mode is computed by the microprocessor into a center frequency (CF) DAC and the vernier DAC, and the sweep width is determined by the ΔF DAC.

The CF DAC has 12 bits, hence 4096 points across the plug-in frequency band (including a 2% overrange and a 2% underrange of the band). The analog output ranges from zero to ten volts, which is used to specify the center frequency output of the plug-in. These parameters give the CF DAC a resolution of 0.024% (2.4 mV) over the full band (including overrange).

Resolution of center frequency is enhanced by a summed voltage generated by an 8-bit (256 points) vernier DAC. Vernier range is set to ±0.048% of RF plug-in bandwidth (including overrange). Vernier resolution is determined by dividing ± 0.048% bandwidth by 256 on the vernier DAC is equal to four points on the 12-bit CF DAC (two points on either side of CF). This increases CF resolution from 0.024% (2.4 mV) to 0.00038% (.04mV), and improves the relative accuracy of the CF by a similar factor. The absolute resolution accuracy still depends on the CF DAC.

NOTE: When adjusting the vernier through its end point, the CF DAC is incremented or decremented by the total value of the vernier (2 point on the CF DAC). At this time the accuracy of the center frequency is again entirely dependent on the linearity of the CF DAC, 0.005% of bandwidth.

Table 3-1. Input Resolution

	ΔF Display Frequency Width			
	0 MHz – 124 MHz	124 MHz – 1 GHz	1 GHz – 4.2 GHz	4.2 GHz – 26.5 GHz
DISPLAYED RESOLUTION	100 kHz	1 MHz	1 MHz	10 MHz
ΔF DISPLAY INDICATION	000.0 MHz	0000. MHz	0000. MHz	00.00 GHz

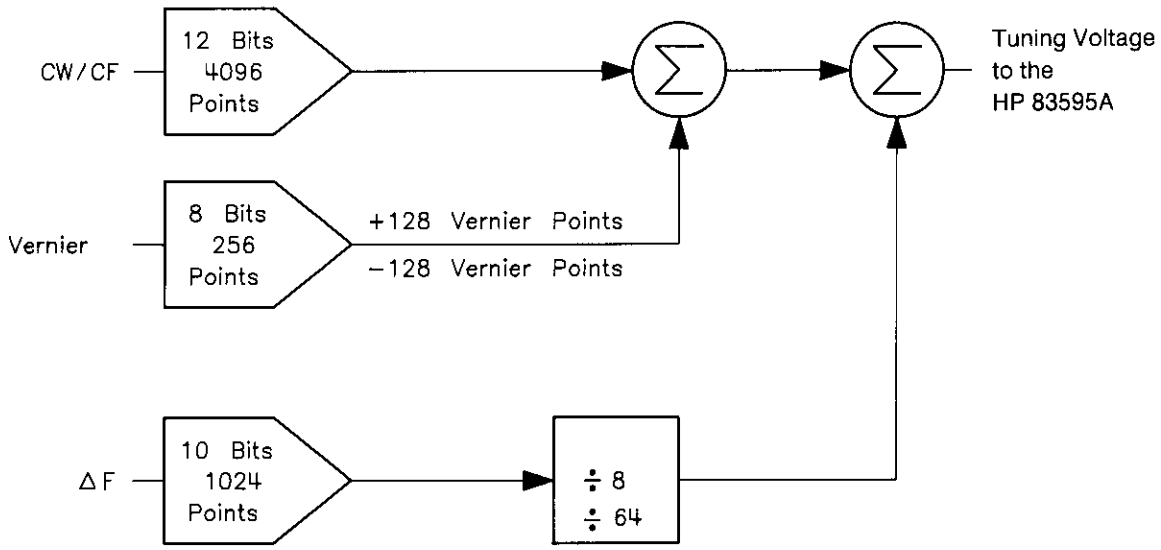


Figure 3-2. Simplified Tuning Voltage Block Diagram

The ΔF DAC has 10 bits (1024 points). The analog input to this DAC ranges from −10 to +10 volts to produce an even sweep on either side of the center frequency. The ΔF resolution improves with narrower sweep widths. For broad sweeps, the resolution is 0.1% of the full band. Greater resolution is provided for sweep widths less than 1/8 of the full band range. At these sweep widths, the resolution is improved to 0.012% of the full band. The greatest resolution is provided for sweep widths less than 1/64 of the full band range. At these sweep widths, the resolution is further improved to 0.0015% of the full band.

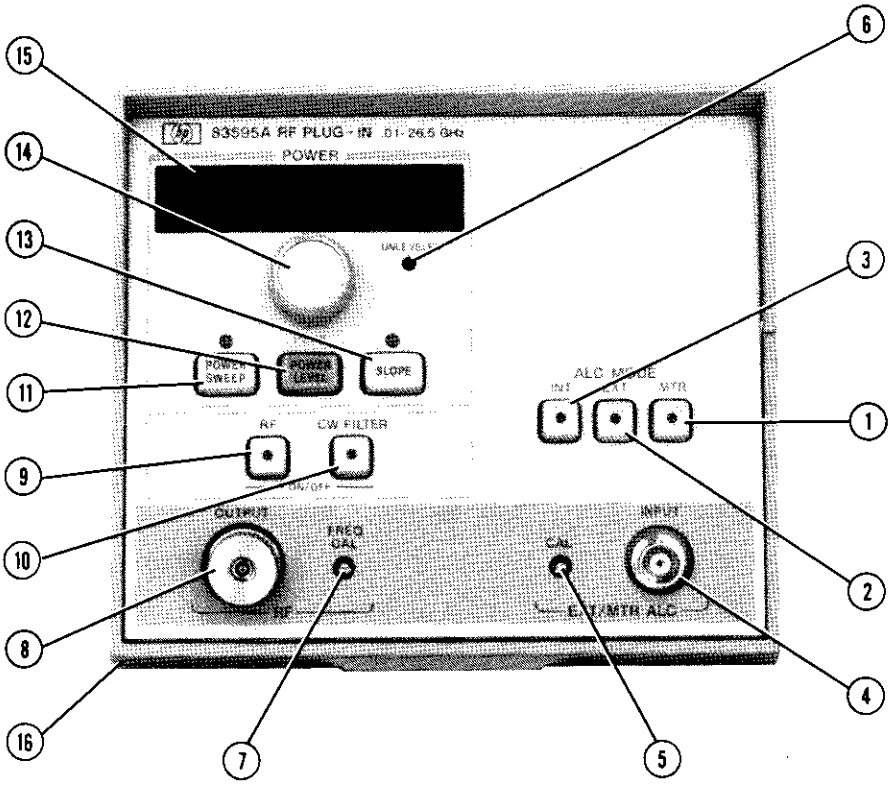
Display Resolution

Center frequency is always displayed with 1 MHz resolution. Likewise, vernier values are always displayed at a 10 kHz resolution. The display resolutions for ΔF values vary with sweep width (Table 3-2 shows the ΔF mode displayed resolution values versus displayed ΔF frequency sweep widths).

Table 3-2. ΔF Sweep Mode Displayed Resolution

	0 MHz	517 MHz	4.23 GHz	12.48 GHz
DISPLAYED RESOLUTION	100 kHz	1 MHz	10 MHz	
Δ DISPLAY INDICATION	X.X MHz XX.X MHz XXX.X MHz	XXX MHz X.XXX GHz	X.XX GHz XX.XX GHz	

FRONT PANEL FEATURES



1. **[MTR]**. Power meter automatic leveling control selection.
2. **[EXT]**. External automatic leveling control selection (negative crystal detector).
3. **[INT]**. Internal automatic leveling control selection.
4. **ALC INPUT**. BNC connector for power meter or external crystal leveling inputs (rear panel on option 004).
5. **CAL**. For setting external (MTR or EXT) leveling inputs.
6. **UNLEVELED** lamp. This lights if the output power is unleveled.
7. **FREQ CAL**. Fine frequency adjust, used for frequency calibration.
8. **RF OUTPUT**. APC-3.5 50-ohm RF output connector (rear panel on option 004).
9. **[RF ON/OFF]**. Used when zeroing a power meter or referencing an X-Y recorder.
10. **[CW FILTER]**. In CW mode, enables an oscillator filter to remove high frequency noise at the RF output (automatically disabled in swept mode).
11. **[POWER SWEEP]**. Used to set an increase in the power per sweep (dB/SWP).

    [SHIFT] [POWER SWEEP]. Locks internal attenuator setting. Allows independent control of ALC amplifier level.

12. **[POWER LEVEL].** Used to set the RF output power level.

    [SHIFT] [POWER LEVEL]. Used to adjust the YTM to track the YIG oscillator above the first switch point (2.4 GHz) for peaking maximum output power.

13. **[SLOPE].** Used to set the frequency slope compensation in dB/GHz (for use with lossy devices).

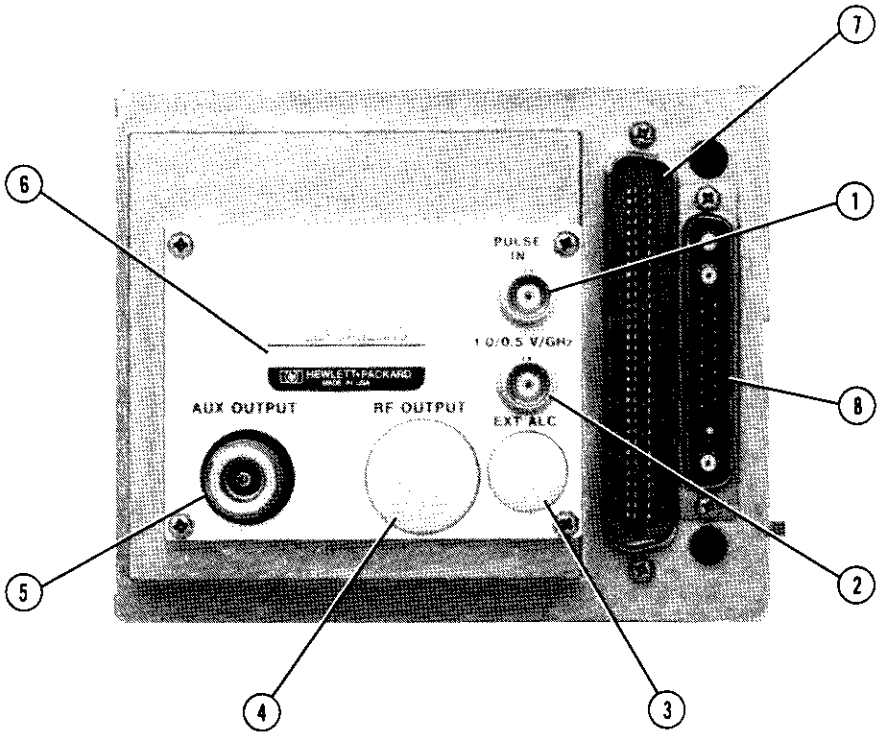
    [SHIFT] [SLOPE]. Locks ALC loop. Allows independent control of (option 002) internal step attenuator.

14. **POWER CONTROL KNOB.** Used to control power level, power sweep, peak, or slope.

15. **POWER DISPLAY.** Provides a readout of the selected power in dBm, dB/GHz, or dB/SWP (to a tenth of a dB/dBm).

16. **PLUG-IN LATCH HANDLE.** Used to remove, install, and latch the RF plug-in in the HP 8350 sweep oscillator.

REAR PANEL FEATURES



1. **PULSE IN**. External pulse or square-wave modulation input.

2. **0.5 V/GHz – 1 V/GHz**. Selectable (1 V/GHz or 0.5 V/GHz) BNC connector output that corresponds to the RF output frequency (0.01 to 18 GHz for 1 V/GHz and 0.01 to 26.5 GHz for 0.5 V/GHz). The HP 8410B/8411A network analyzer utilizes the 1.0 V/GHz output for phase-locking. The HP 83550 series millimeter-wave source modules use the 0.5 V/GHz as a frequency reference for millimeter-wave applications. See Figure 3-5 for instructions on how to set the frequency reference selection switch (A2S1).

3. **EXT ALC**. Replaces front panel EXT ALC connector on Option 004 plug-ins.

4. **RF OUTPUT**. Replaces front panel RF output connector in Option 004 plug-ins.

5. **AUX OUTPUT**. Type-N, 50 ohm connector that provides a 2.3 to 7.0 GHz fundamental oscillator output at approximately 0 dBm.

6. **Serial Number Plate**. Contains a ten digit serial number (for use in any correspondence concerning the plug-in) and applicable option number(s).

7. **RF Plug-In Interface Connector.** Connector through which the RF plug-in receives and sends digital and analog signals from and to the HP 8350.

8. **Power Supply Plug-In Interface Connector.** Connector through which the RF plug-in receives required power supplies from the HP 8350.

RF PLUG-IN CONFIGURATION SWITCH

The RF plug-in configuration switch is located on the digital interface assembly (A3), as shown in Figure 3-3.

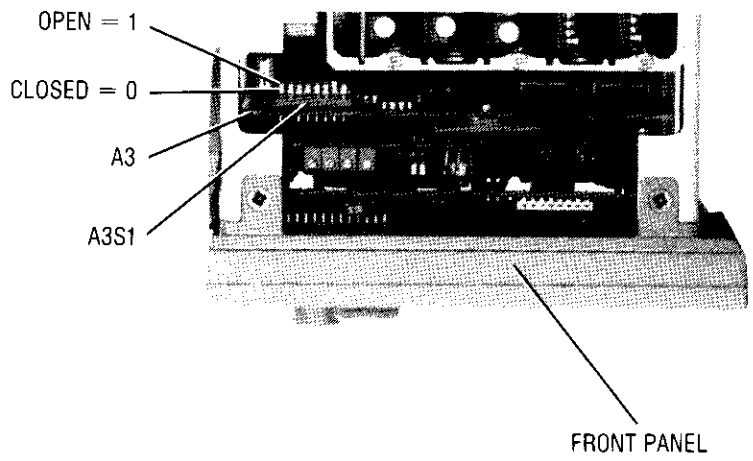


Figure 3-3. RF Plug-In Configuration Switch Location

Configuration switch A3S1 is set at the factory for a combination of operating modes (see Table 3-3). Using six of the eight switch sections, you can select other operating modes. Table 3-3 defines each switch segment and the position of each for the different operating modes.

NOTE: Configuration switch settings override the HP 8350 non-volatile memory settings at instrument preset. If you change the switch settings, you must press **[INSTR PRESET]** to load memory with the new configuration.

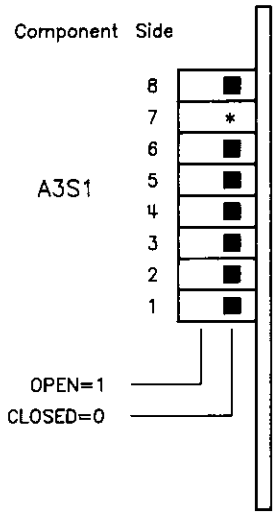
Table 3-3. RF Plug-In Configuration Switch Settings

Description	Switch Number							
	1	2	3	4	5	6	7	8
No RF Power at INSTRUMENT PRESET	x	x	x	1	x	x	x	x
RF Power at INSTRUMENT PRESET	x	x	x	0	x	x	x	x
−6 MHz/V FM Sensitivity	x	x	x	x	1	x	x	x
−20 MHz/V FM Sensitivity	x	x	x	x	0	x	x	x
Step Attenuator, Option 002, Installed	x	x	x	x	x	x	1	x
No Step Attenuator, Option 002, Installed	x	x	x	x	x	x	0	x

Switch A3S1 is set from the factory as follows:

Switch No.	Position
1	0
2	0
3	0
4	0
5	0
6	0
7	*
8	0

*"1" if Option 002 installed; "0" if Option 002 not installed.



NOTES:
Switch positions:

1 = Open = High
0 = Closed = Low (Ground)
X = Don't Care

FREQUENCY REFERENCE SELECTION SWITCH

Use position 1 on the frequency reference selection switch on the A2 assembly to set the desired frequency reference for your application. See Figure 3-4.

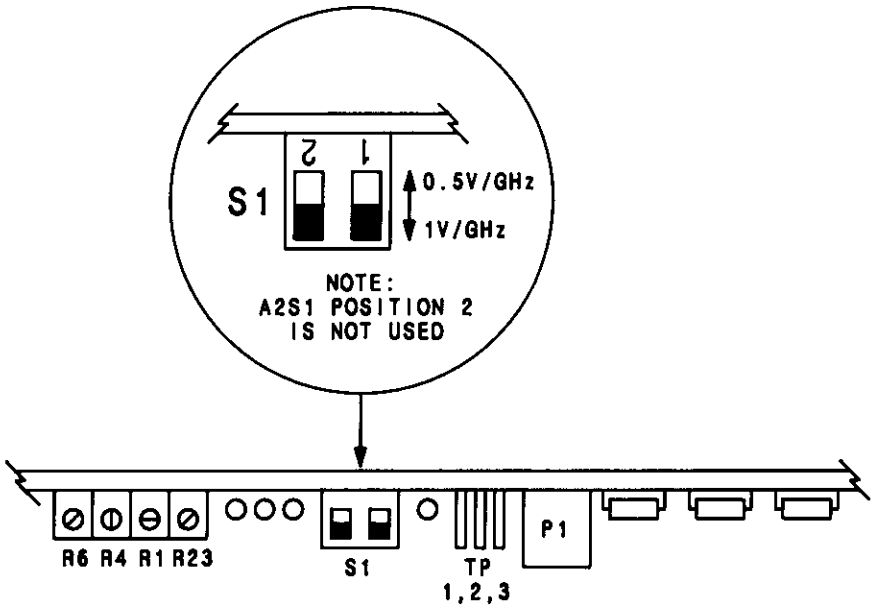


Figure 3-4. Frequency Reference Selection Switch, A2S1

OPERATOR'S CHECKS

The operator's check portion (local and remote) of the *HP 8350 Sweep Oscillator Operating and Service Manual* provides a quick evaluation of the main functions of both the HP 8350 and the 83595A.

If the instruments do not pass the operator's checks, the trouble may be in either unit. If you suspect the RF plug-in, refer to the troubleshooting paragraphs located in Section 8.

MILLIMETER-WAVE APPLICATION

Figure 3-5 shows a typical millimeter-wave test set up using an HP 83595A. Note that an HP 8349B microwave amplifier is required to produce the power level required by the millimeter-wave source module. Also notice that the HP 83550 series millimeter-wave source modules use the 0.5V/GHz as a frequency reference, this 1.0/0.5 V/GHz frequency reference output is switch selectable on the A2 interface assembly.

For details on millimeter wave applications, refer to the *HP 83590 Series Source System Guide* located in any millimeter-wave source module manual.

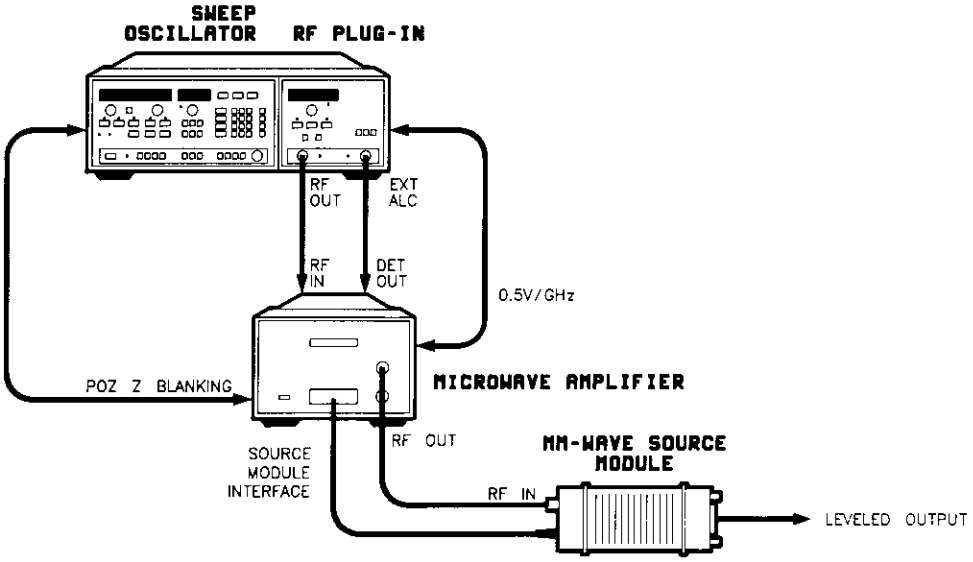


Figure 3-5. Typical millimeter-wave test setup

CAUTION

Turn the HP 8349B AC power OFF before connecting or disconnecting the source module interface cable.

FRONT PANEL FREQUENCY CALIBRATION

The first procedure calibrates the RF output frequency for band 0 using an external frequency counter. The alternate procedure is not as accurate as using an external counter, but typically calibrates band 0 frequency accuracy to within specifications.

NOTE: The HP 83595A may not meet frequency accuracy specifications unless you calibrate the band 0 RF output frequency.

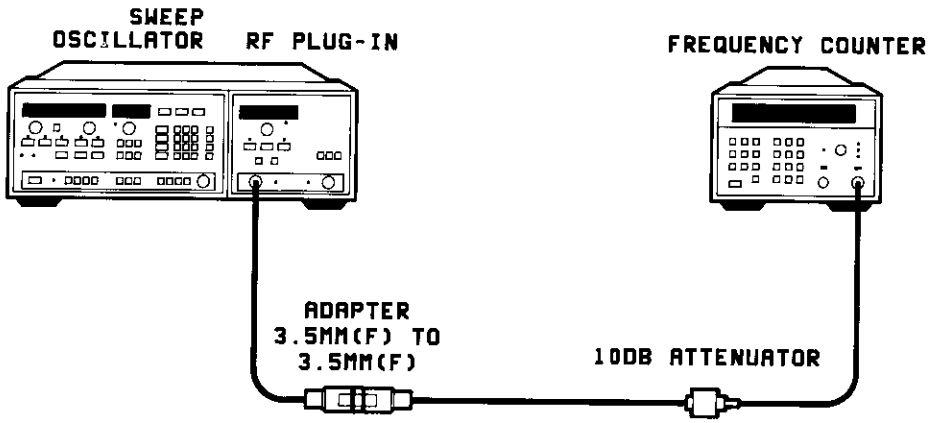


Figure 3-6. Front Panel FREQ CAL Equipment Set Up

Equipment

Sweep Oscillator Mainframe	HP 8350
Frequency Counter	HP 5343A
10 dB Attenuator	HP 8493C Option 010
Adapter 3.5 mm (f) to 3.5 mm (f)	HP Part No. 1250-1749

Procedure

1. Connect the equipment as shown in Figure 3-6. Turn on the instruments and let them warm up for at least 30 minutes. Ensure that the RF output power is on, either by instrument preset or by using the RF on/off key.
2. On the HP 8350, press **[INSTR PRESET] [CW] [5] [0] [MHz]**.
3. On the HP 83595A, adjust the FREQ CAL control for a frequency counter display of 50.0 MHz.

Alternate Procedure

1. Turn on the HP 8350/83595A and allow the instrument to warm up for at least 30 minutes.
2. On the HP 8350, press **[INSTR PRESET] [CW] [0] [MHz]**.
3. On the HP 83595A, adjust the FREQ CAL control through its range and note the portion of the range that the UNLEVELED light is on.
4. Set the FREQ CAL control to the center of the unleveled range noted in step 3.

RF OUTPUT POWER PEAKING

Due to normal operation and internal RF component tolerances, you may need to peak the RF output power to maximum specified output power in the internal leveled operating mode. Peaking optimizes the tracking between the fundamental oscillator and the frequency multiplier.

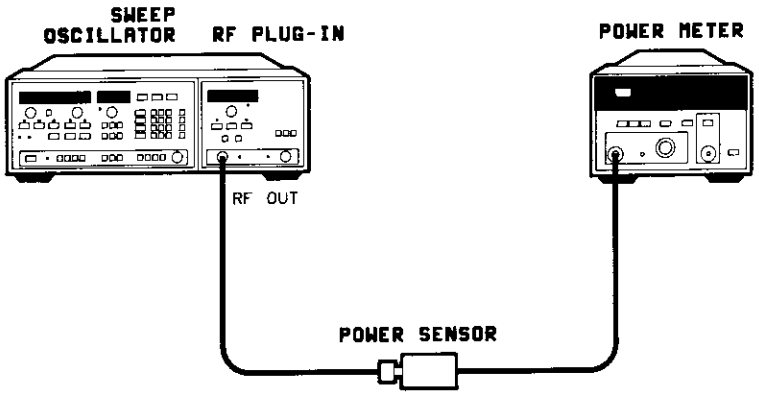


Figure 3-7. Peaking RF Output Power Equipment Setup

Equipment

Sweep Oscillator Mainframe	HP 8350
Power Meter	HP 436A
Power Sensor	HP 8485A
Adapter 3.5 mm (f) to 3.5 mm (f)	HP Part No. 1250-1749

Procedure

1. Connect the equipment as shown in Figure 3-7, and allow the instruments to warm up for at least 30 minutes.
2. On the HP 83595A, increase the RF output power until it becomes unleveled (or select external leveling, without an external detector connected).
3. On the HP 8350, press **[START] [2] [.] [4] [GHz]**.
4. On the HP 83595A, press **[SHIFT] [POWER LEVEL]** (to select PEAK), and adjust the power knob to maximize the RF output power from 2.4 to 26.5 GHz.

INTERNAL LEVELING

Internal leveling is the most convenient method of RF output leveling. A portion of the RF output power is internally coupled/detected and the resulting DC voltage (which is proportional to the RF power) is applied to the automatic leveling control circuit (ALC) to maintain a constant power output. The DC voltage is proportional to the RF power at low power levels and at high power levels the voltage is proportional to the RF voltage.

EXTERNAL CRYSTAL DETECTOR LEVELING

The RF output power can be leveled externally using a power splitter (or external directional coupler) and a negative output crystal detector. The advantage of a directional coupler is that it does not have as great a coupled loss as the 6 dB insertion loss with the power splitter, so you can obtain a higher maximum leveled output power, however it will typically have more ripple and slope.

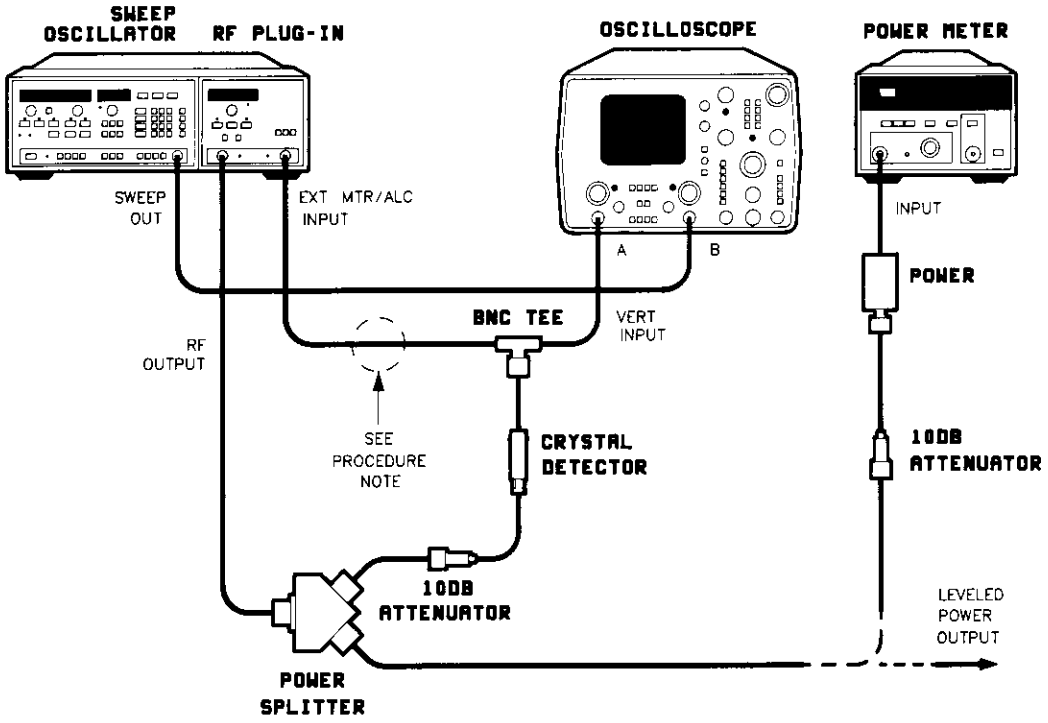


Figure 3-8. External Crystal Detector Leveling Setup

Equipment

Sweep Oscillator Mainframe	HP 8350
Oscilloscope	HP 1741A
Power Meter	HP 436A
Power Sensor	HP 8485A
Crystal Detector	HP 8473C
Power Splitter	HP 11667B
10 dB Attenuator (2 required)	HP 8493C, Opt 010
BNC Tee	HP P/N 1250-0781

Procedure

1. Connect the equipment as shown in Figure 3-8. Turn the instruments on and allow them to warm up for at least 30 minutes.
2. On the HP 8350, press **[INSTR PRESET] [CW]**.
3. On the HP 83595A, press **[EXT]**, and adjust the CAL adjustment for a power meter reading equal to the reading on the plug-in front panel (subtract out the losses due to the power splitter).
4. To use leveled RF power output to test external equipment, make the connection at the point marked leveled power output in Figure 3-9.

NOTE: Between 10 and 50 MHz, RF feedthrough as high as 3 dB may be observed on the envelope of the video output. During external leveling between 10 and 50 MHz, the RF feedthrough can be damped out by inserting the circuit shown in Figure 3-9 in the line to the RF plug-in EXT ALC INPUT of the RF plug-in.

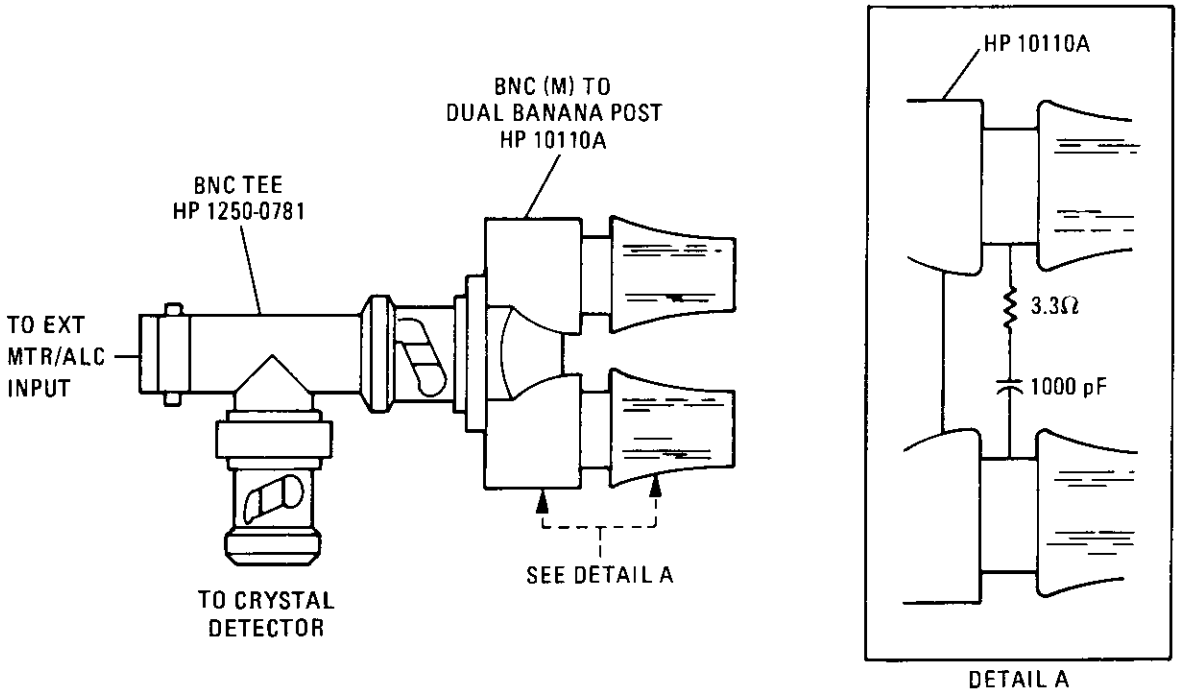


Figure 3-9. 10 to 50 MHz RF Feedthrough Dampening

EXTERNAL POWER METER LEVELING

RF output power can be leveled using a power meter and a power splitter (or directional coupler). When using power meter leveling, limit the sweep time to greater than 100 seconds for best power level accuracy.

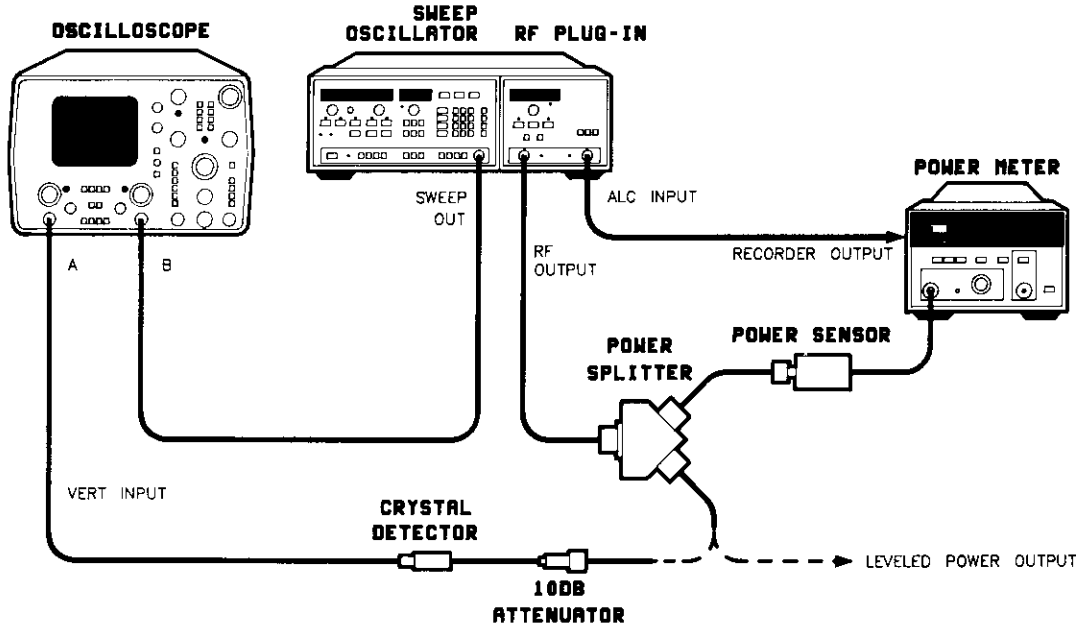


Figure 3-10. External Power Meter Leveling Set Up

Equipment

Sweep Oscillator Mainframe	HP 8350
Oscilloscope	HP 1741A
Power Meter	HP 436A, 438A
Power Sensor	HP 8485A
Crystal Detector	HP 8473C
Power Splitter	HP 11667B
10 dB Attenuator	HP 8493C, Opt 010
Adapter 3.5 mm (m) to 3.5 mm (m)	HP Part No. 1250-1749

Procedure

1. Turn on the instruments and allow 30 minutes for warm-up.
2. Zero and calibrate the power meter/sensor.

3. On the HP 8350:

   Press **[INSTR PRESET]**.

   Set SWEEP TIME to 100 sec.

   Press **[STOP] [2] [0] [GHz]**.

4. On the HP 83595A:

   Press **[MTR]** to select external power meter leveling.

   Adjust the ALC CAL for a +10 dBm reading on the power meter.

5. On the HP 8350:

   Press **[SINGLE]** to set the single sweep mode. Press **[SINGLE]** again to start a sweep. Note that if you press **[SINGLE]** a third time, the sweep stops. Once single sweep is set, this key acts like an on/off switch for the sweep.

   To use leveled RF output power for testing external equipment, make the connection at the point marked leveled power output, in Figure 3-10.

EXTERNAL FM

You can frequency modulate (FM) the HP 83595A RF output signal applying an external modulation signal to the HP 8350 rear panel FM INPUT connector. A positive going voltage at the FM INPUT causes the output frequency to decrease, while a negative going voltage causes the output frequency to increase.

You can set the sensitivity and the coupling of the modulating signal via the RF plug-in configuration switch (A3S1) (refer to Table 3-3).

EXTERNAL AM

There are two types of external amplitude modulation:

Pulse Modulation

Pulsed or square-wave modulation can be applied to the HP 83595A rear panel PULSE IN connector. This input provides an on/off power ratio of greater than 30 dB below specified maximum leveled power.

For the best pulse modulation performance, set the RF output power at +20 dBm (unleveled). With this power setting, a pulse repetition rate of up to 1 MHz is possible from 0.01 to 7.0 GHz or a 30 kHz rate for frequencies of 7.0 to 26.5 GHz. With leveled power, pulse repetition rates can be up to 100 kHz at frequencies of 0.01 to 7.0 GHz. Frequencies of 7.0 to 26.5 GHz can be square-wave modulated at repetition rates up to 30 kHz.

See Section 1 for details of on the modulation characteristics for this input.

Amplitude Modulation

The HP 8350 rear panel AM INPUT provides linear amplitude changes (up to approximately 15 dB) proportional to the modulating input voltage. Frequency response is limited to approximately 100 kHz.

For maximum depth of modulation (maximum modulation index), set the power level to the middle of the output power control range (e.g. +2.5 dBm for a plug-in with calibrated power control from −5 to +10 dBm). For plug-ins equipped with option 002 (55 dB step attenuator), the middle of the attenuator range should be selected.

A positive DC voltage at the AM INPUT causes an increase in the RF output power; a negative DC voltage causes a decrease in the RF output power.

RF POWER CONTROL

Power Level

The HP 83595A provides a maximum leveled RF output power of +10 dBm. A front panel LED indicates when the RF output becomes unleveled. The power level is controlled by the front panel rotary pulse generator (RPG), the HP 8350 data entry controls (keypad and step keys), or through HP-IB control via the HP 8350. This function when enabled allows setting the output power level for all ALC modes. Calibrated power level is available during internal leveling only.

You can turn off the RF output with the **[RF ON/OFF]** key. Power ON is indicated by the LED in the center of the key. You can set the HP 83595A to have either maximum specified power or RF power OFF at INSTR PRESET. Refer to Table 3-3 for the proper configuration switch setting.

Power Sweep

When this function is enabled (LED on) the RF output power can be swept with an increase in power per sweep (dB/SWP). The level of the power sweep starting point is the power level programmed before the power sweep function is turned on. The settable range is −5 to +10 dB/SWP and is limited by the dynamic range of the ALC loop.

The power sweep width can be entered via the keyboard, step keys, or the RF plug-in RPG. The level of the power sweep end point is determined by the sum of the starting power level and the sweep width. Power sweep is turned off and reset to 0 dB/SWP whenever INSTR PRESET is initiated.

Slope

When this function is enabled (LED on) the frequency slope compensation can be set via the keyboard, step keys or the RF plug-in RPG. It allows positive slope compensation for devices with linear losses proportional to frequency (cables). Slope is turned off and reset to 0 dB/GHz whenever INSTR PRESET is initiated.

Option 002 − Attenuator

With option 002, the RF output power can be continuously controlled from maximum leveled output power down to −60 dBm. When the selected power setting goes below −5 dBm, the step attenuator increments as required in 5 dB steps, to a maximum attenuation of 55 dB. Within the individual 10 dB attenuation steps, the ALC loop adjusts the output power to ensure optimum modulator range and stable output characteristics.

[SHIFT] [POWER SWEEP]. When an HP 8350 front panel **[SHIFT]** function is used together with an HP 83595A **[POWER SWEEP]** function, you can control power within the ALC range without changing the attenuator settings. Data can be entered using the keyboard, step keys, or the RF plug-in RPG and the display disregards the attenuator settings and only displays the ALC setting.

The sum of the independent ALC power level (SHIFT POWER SWEEP) and the independent attenuator setting (SHIFT SLOPE) equal the RF power level (power displayed with the POWER LEVEL key).

[SHIFT] [SLOPE]. When an HP 8350 front panel **[SHIFT]** function is used together with an HP 83595A **[SLOPE]** function, you can control the attenuator step settings without affecting the ALC settings. Data can be entered using the keyboard, step keys, or the RF plug-in RPG and the display indicates the attenuator setting (0.0, −5.0, −10.0, −15.0, −20.0, −25.0, −30.0, −35.0, −40.0, −45.0, −50.0, or −55.0 are the possible values). Note that the keyboard entries are truncated down to a multiple of 5 dB.

The sum of the independent ALC power level (SHIFT POWER SWEEP) and the independent attenuator setting (SHIFT SLOPE) equal the RF power level (power displayed with the POWER LEVEL key).

This mode is exited by pressing either POWER LEVEL, POWER SWEEP, or SLOPE keys. The ALC and attenuator step setting are now automatically controlled by the firmware.

ALTERNATE SWEEP MODE

If the option 002 attenuator is installed and you select alternate sweep mode, a default condition of 1 second/sweep can occur. This default condition happens only when the POWER settings of the two alternate sweeps require that the attenuator switch after each sweep. So that the attenuator relay coils do not overheat, which can cause damage, the attenuator is prevented from switching faster than 1 step per second.

HP-IB

All front panel functions, except for the FREQ CAL and ALC CAL adjustments can be altered by computer control via the HP-IB bus connection on the HP 8350.

FIRMWARE REVISION NUMBER

Press **[SHIFT] [9] [9]** on the HP 8350. The plug-in firmware revision number appears in the HP 83595A POWER display window. Various measurement systems (scalar, vector network analyzers) require a specific firmware revision. For compatibility requirements contact your local HP sales/ service office for further information.

PHASE-LOCK OPERATION

The required CW frequency for the HP 83595A is automatically tuned and locked by the HP 5344S microwave source synchronizer, with the HP 5344S acting as an HP-IB controller. No manual tuning is required. The HP 8350 sweep oscillator and the HP 5344S microwave source synchronizer must be set to the same HP-IB address.

NOTE: This set up can be used for phase-locking from 0.01 to 18.0 GHz, the range of the HP 11691D directional coupler. For phaselocking without the use of a broadband coupling device, the 83595A rear panel AUX OUTPUT fundamental oscillator frequency signal can be used.

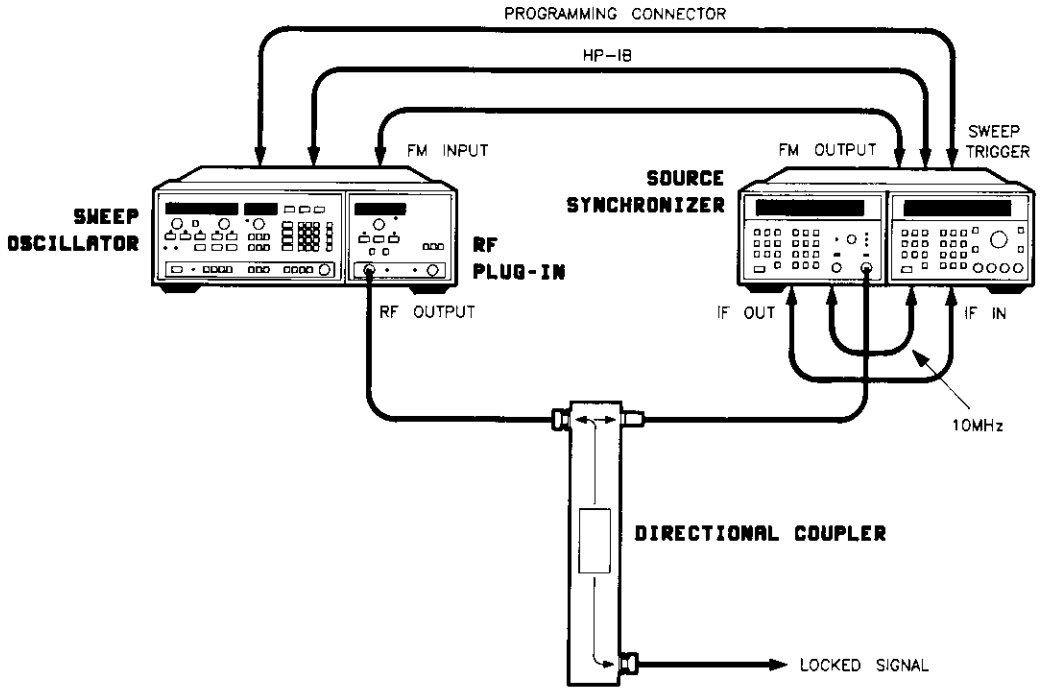


Figure 3-11. Phase-Locking Using the HP 5344S Microwave Source Synchronizer

Equipment

Sweep Oscillator Mainframe	HP 8350
Source Synchronizer	HP 5344S Option 043
Directional Coupler	HP 11691D
Adapter 3.5 mm (f) to Type-N (f)	HP Part No. 1250-1745

Procedure

1. Set the HP 83595A configuration switch (A3S1) for an FM sensitivity of −6 MHz/V, cross over coupled FM and AUX OUTPUT phase-lock (see Table 3-3).

2. Connect the equipment as shown in Figure 3-11. Turn the instruments on and let them warm up for at least one hour.

3. On the sweep oscillator, check the HP-IB address:

   Press **[SHIFT] [LCL]**. The HP-IB address will be shown on the HP 8350 FREQUENCY/TIME display.

4. On the microwave source synchronizer:

   Set the HP 5344S HP-IB address to the same address as the HP 8350 (factory set at 19,10011).

   Set the HP 5344S to the System Controller mode by setting the top HP-IB switch to the left (SYS CONT).

5. On the sweep oscillator/RF plug-in:

   Press **[INSTR PRESET]**.

   Press **[CW FILTER]** to turn it off.

   Press **[POWER LEVEL]** and set a power level between 0 and +5 dBm.

6. On the microwave source synchronizer:

   Check that both MANUAL LOCK and AUTO LOCK are set to off (pushbutton LEDs off). Verify that the front panel CONT lamp is on.

7. Press **[MODE]** until the CW annunciator lights. The MODE key will scroll through four modes of operation. If you pass CW, continue pressing MODE until you return to CW.

8. Enter the frequency required for the HP 83595A RF output signal.

   Press **[AUTO LOCK]**. The HP 83595A RF output signal will now be programmed and locked to the specified CW frequency.

OPERATOR'S MAINTENANCE

PLUG-IN ERROR CODES

The HP 8350 sweep oscillator and the HP 83595A RF plug-in have a series of internal power-on self tests which will indicate an error code on either the HP 8350 frequency or the HP 83595A power displays, should a failure occur.

Error codes E001 through E016 are specific to the HP 8350 and indicate a possible failure in the sweep oscillator. Refer to the *HP 8350 Operating and Service Manual* for information and troubleshooting procedures.

Error code E050 through E099 are specific to the HP 83595A and indicate a possible failure in the RF plug-in. Refer to Section 8 for more information.

FUSES

HP 83595A power supplies are fused in the HP 8350 sweep oscillator. Refer to the *HP 8350 Sweep Oscillator Operating and Service Manual* for fuse locations and replacement instructions.

BLUE SERVICE TAGS

If the HP 83595A requires service, you can send the instrument to your local HP service organization, as described in Section 2. Before sending the instrument in, fill out and attach one of the blue service tags. On the FAILURE SYMPTOMS/SPECIAL CONTROL SETTINGS portion of the tag, record any error codes noted.

Section 4. Performance Tests

INTRODUCTION

The procedures in this section test the electrical performance of the HP 8350 sweep oscillator/ 83595A RF plug-in combination, with the RF plug-in specifications used as the performance standards. The plug-in specifications are listed in Table 1-1 of Section 1. These performance tests do not require access to the interior of the HP 83595A RF plug-in.

NOTE: Allow the HP 83595A RF plug-in and the HP 8350 sweep oscillator to warm-up for at least one hour before you begin any performance tests.

EQUIPMENT REQUIRED

The equipment required to performance test the HP 83595A is listed in Table 1-4 of Section 1. Any equipment that satisfies the critical specifications given in the table can be substituted for the recommended model.

OPERATION VERIFICATION

Operation Verification consists of performing the following tests:

- Frequency Range and Accuracy
- Output Amplitude

The HP-IB functions can be verified using the program listed in Section IV of the *HP 8350 Operating and Service Manual*.

These tests provide reasonable assurance that the sweep oscillator and plug-in are functioning properly and should meet the needs of an incoming inspection (80% verification).

TEST RECORDS

Table 4-9 provides a tabulated index of the performance tests, their acceptable limits, and a column for recording actual measurements. Use this test record when performing a calibration (100% verification).

Table 4-10 is the test record to use for recording the results of an operational verification. A column for recording pass/fail indications is provided.

RELATED ADJUSTMENTS

Table 4-1 lists the performance tests, and references associated adjustments for each test that is provided in Section 5 of this manual. If the result of a performance test is out of the specified limits, the associated adjustment may correct this condition.

TEST SEQUENCE

Perform the tests in the order that they appear.

CALIBRATION CYCLE

For the HP 83595A, perform the tests in this section at intervals of twelve months or less.

Table 4-1. Performance Tests and Related Adjustments

Performance Tests	Related Adjustment
4-1. Frequency Range and Accuracy	
CW Frequency Accuracy	5-1. −10V Reference on A8 YO Driver 5-3. YO and YTM DAC Calibration 5-4. Preliminary Frequency Accuracy
Swept Frequency Accuracy	5-2. Sweep Control Adjustments 5-3. YO and YTM DAC Calibration 5-4. Preliminary Frequency Accuracy 5-5. YO Retrace Compensation 5-6. YO Delay Compensation 5-10. Band Overlap Compensation
Marker Accuracy	5-1. −10 Volt Reference on A8 YO Driver 5-2. Sweep Control Adjustments 5-3. YO and YTM DAC Calibration 5-4. Preliminary Frequency Accuracy 5-5. YO Retrace Compensation 5-6. YO Delay Compensation 5-10. Band Overlap Compensation
4-2. Output Amplitude	
Maximum Leveled Power Output Power Variations	5-12. ALC Adjustment 5-14. ALC Internally Leveled Flatness 5-16. ALC Gain Adjustment
Power Level Accuracy	5-12. ALC Adjustment 5-14. ALC Internally Leveled Flatness 5-16. ALC Gain Adjustment
Power Sweep Range	5-17. Power Sweep
4-3. Frequency Stability	
4-4. Residual FM	
4-5. Spurious Signals	5-8. SRD Bias
4-6. External Frequency Modulation	5-18. FM Driver Adjustments
4-7. Square-Wave On/Off Ratio and Symmetry	5-17. ALC Gain Adjustment
4-8. Step Attenuator Accuracy (Option 002)	

4-1. Frequency Range and Accuracy Test

SPECIFICATION

Frequency Range: 0.01 to 26.5 GHz

Frequency Accuracy: (25° ±5° C):

Bands (GHz)	0.01 to 2.4	2.4 to 7.0	7.0 to 13.5	13.5 to 20.0	20.0 to 26.5	0.01 to 26.5
CW Mode	±5 MHz	±5 MHz	±10 MHz	±10 MHz	±12 MHz	———
All Sweep Modes (Sweep time >100 ms)	±15 MHz	±20 MHz	±25 MHz	±30 MHz	±35 MHz	±50 MHz
Frequency Markers (sweep time ≥ 100 ms)	±15 MHz ±0.5% of sweep width	±20 MHz ±0.5% of sweep width	±25 MHz ±0.5% of sweep width	±30 MHz ±0.5% of sweep width	±35 MHz ±0.5% of sweep width	±50 MHz ±0.5% of sweep width

DESCRIPTION

A frequency counter is used to check frequency range and accuracy in the CW mode. The frequency counter is also used to check swept frequency accuracy and markers in the START/STOP mode.

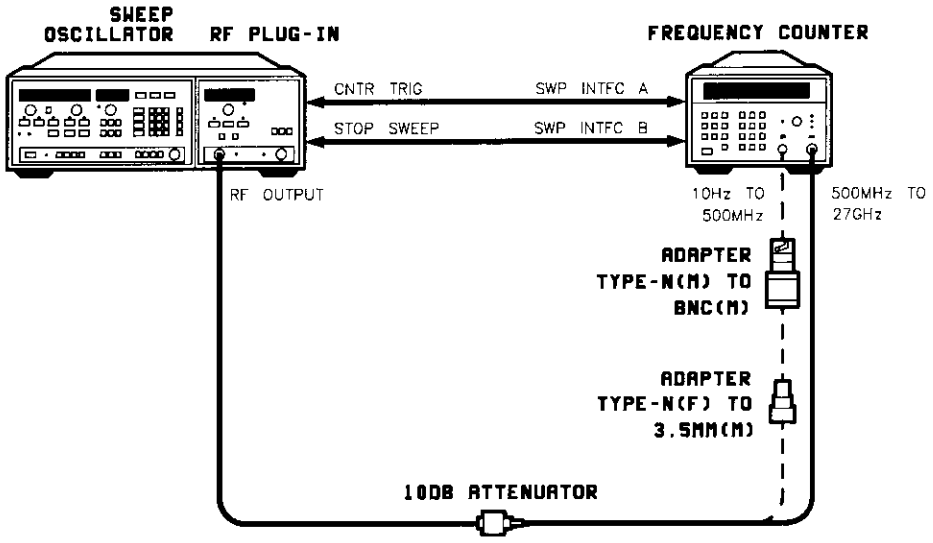


Figure 4-1. Frequency Range and CW Accuracy Test Setup

4-1. Frequency Range and Accuracy Test (Cont'd)

EQUIPMENT

Sweep Oscillator Mainframe	HP 8350
Frequency Counter	HP 5343A
10 dB Attenuator	HP 8493C Option 010
Adapter 3.5 mm (f) to 3.5 mm (f)	HP Part No. 1250-1749
Adapter Type-N (m) to 3.5 mm (f)	HP Part No. 1250-1744
Adapter Type-N (m) to BNC (m)	HP Part No. 1250-1533
Cables (2), SMB (f) to BNC (m)	HP Part No. 08350-60039

PROCEDURE

1. Connect the equipment as shown in Figure 4-1 and press **[INSTR PRESET]** on the HP 8350/83595A. Allow at least one hour warm-up. Note that the sweep oscillator display indicates a start frequency of 10 MHz and a stop frequency of 26.5 GHz.

2. On the frequency counter, set the controls as follows:

LINE	ON
SAMPLE RATE	minimum (full CCW)
Range Connector	As required
Impedance Switch	50 Ω
ACQ TIME (rear panel)	FAST

NOTE: Before proceeding with the test, perform the front panel frequency calibration located in Section 3.

Frequency Range

3. On the sweep oscillator/RF plug-in, set CW to the start frequency of the RF plug-in. If the frequency counter reads greater than 10 MHz, rotate the HP 8350 CW control counterclockwise until the frequency counter reads 10.00 MHz or lower. Record this reading on the test record.

4. Set the CW control to the high end frequency of the RF plug-in. If the frequency counter reads lower than 26.5 GHz, rotate the CW control clockwise until the frequency counter reads 10.00 MHz or lower. Record this reading on the test record.

CW Frequency Accuracy

Table 4-2. CW Frequency Accuracy

Bands (Accuracy)				
Band 0 (±5 MHz)	**Band 1 (±5 MHz)**	**Band 2 (±10 MHz)**	**Band 3 (±10 MHz)**	**Band 4 (±12 MHz)**
10 MHz	4.0 GHz	10 GHz	17.0 GHz	24.0 GHz
1.0 GHz	2.5 GHz	7.1 GHz	14.0 GHz	21.0 GHz
2.4 GHz	7.0 GHz	13.5 GHz	20.0 GHz	26.5 GHz

5. Check the CW frequency accuracy for each CW frequency listed in Table 4-2. Verify that the frequency counter indication at these points is within the accuracy tolerance specified. Follow the sequence of frequencies listed for each band from top to bottom to avoid band crossover problems. Record the readings on the test record.

4-1. Frequency Range and Accuracy Test (Cont'd)

Swept Frequency Accuracy

Table 4-3. Swept Frequency Accuracy

Band	Start	Stop	Tolerance
Full Band	10 MHz	26.5 GHz	±50 MHz
Band 0	10 MHz	2.4 GHz	±15 MHz
Band 1	2.4 GHz	7.0 GHz	±20 MHz
Band 2	7.0 GHz	13.5 GHz	±25 MHz
Band 3	13.5 GHz	20.0 GHz	±30 MHz
Band 4	20.0 GHz	26.5 GHz	±35 MHz

6. On the frequency counter, press **[RESET] [SWP M]** (light on), **[Blue Key] [1 kHz]**.
7. On the sweep oscillator/RF plug-in:

   Press **[INSTR PRESET]** and set the sweep time to 105 msec.

   Enter the start and stop frequencies for the band you wish to check (see Table 4-3).
8. Press **[START] [SHIFT]** and **[M2]**. Check the frequency counter reading for a start frequency listed in Table 4-3 and record the reading on the test record.
9. Press **[STOP] [SHIFT]** and **[M2]**. Check the frequency counter reading for a stop frequency listed in Table 4-3 and record the reading on the test record.
10. Repeat steps 6 through 9 for each band.

Frequency Marker Accuracy

Table 4-4. Frequency Marker Accuracy

Band	Sweep Range		Marker Frequencies					
	Start	Stop	M1	M2	M3	M4	M5	Tolerance
Full Band	0.01 to 26.5 GHz		1.0 GHz	4.0 GHz	12.0 GHz	18.0 GHz	24.0 GHz	±182.45 MHz
Band 0	0.01 to 2.4 GHz		1.0 GHz	2.0 GHz	—	—	—	±26.95 MHz
Band 1	2.4 to 7.0 GHz		3.0 GHz	6.0GHz	—	—	—	±43.0 MHz
Band 2	7 to 13.5 GHz		8.0 GHz	12.0 GHz	—	—	—	±57.5 MHz
Band 3	13.5 to 20 GHz		15.0 GHz	18.0 GHz	—	—	—	±62.5 MHz
Band 4	20 to 26.5 GHz		21.0 GHz	25.0 GHz	—	—	—	±82.5 MHz

11. On the HP 8350, press **[INSTR PRESET]**. Set the sweep time to 105 msec. Set the start/stop frequencies for the first sweep range as listed in Table 4-4. Set the markers to the frequencies listed in Table 4-4 as they correspond to the particular sweep range.
12. Press **[SHIFT] [M2]**, and the first marker. Verify that the frequency counter reads within the tolerance given in Table 4-4. Record the reading on the test record. Repeat for each of the remaining markers in the sweep range.
13. Repeat for each frequency range in Table 4-4 and for each marker in that frequency range. Record the readings on the test record.

4-1A. Alternate Swept Frequency and Marker Accuracy Test

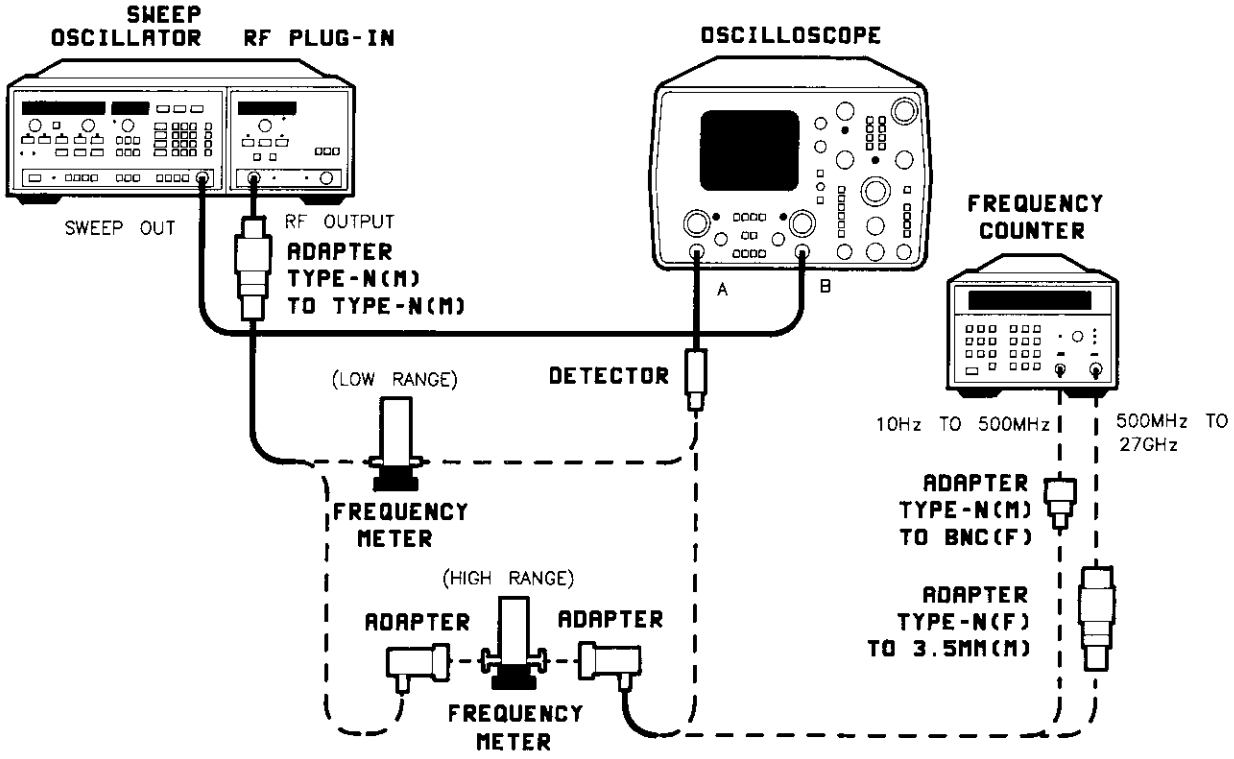


Figure 4-1A. Alternate Swept Frequency Accuracy Test Setup

EQUIPMENT

Sweep Oscillator Mainframe	HP 8350
Crystal Detector	HP 8473C
Frequency Counter	HP 5343A
Oscilloscope	HP 1741A
Frequency Meters:	
0.96 to 4.2 GHz	HP 536A
3.7 to 12.4 GHz	HP 537A
12.4 to 18.0 GHz	HP 532A
18.0 to 26.5 GHz	HP K532A
Adapter Type-N (m) to Type-N (m)	HP Part No. 1250-1528
Adapter Type-N (m) to 3.5 mm (f)	HP Part No. 1250-1744
Adapters (Waveguide to Coax)	
12.4 to 18.0 GHz	HP P281C Option 013
18.0 to 26.5 GHz	HP K281C

PROCEDURE

1A. Connect equipment as shown in Figure 4-1A. Use the frequency meter necessary to cover the tested frequency range of the HP 83595A.

4-1A. Alternate Swept Frequency and Marker Accuracy Test (Cont'd)

2A. On the sweep oscillator/RF plug-in:

Press **[INSTR PRESET]** and then set sweep time to 105 msec.

NOTE: To use the frequency meters for swept and marker frequency accuracy, first calibrate the frequency meters. Calibrate meters by using the frequency counter to set the HP 8350 swept CW frequency to each frequency listed on the test record, then connect the oscilloscope and adjust the frequency meter to dip trace. Record the difference between actual and frequency meter reading.

Swept Frequency Accuracy

3A. Adjust the frequency meter to move the notch on oscilloscope trace to the start frequency. Check and record corrected frequency meter reading on test record.

4A. Adjust frequency meter to move the notch on oscilloscope trace to the stop frequency. Check and record corrected frequency meter reading on test record.

Frequency Marker Accuracy

5A. On the sweep oscillator/RF plug-in:

Press **[INSTR PRESET]** and set sweep time to 105 msec.

6A. Set the HP 8350 frequency markers to the frequencies listed in Table 4-4. Adjust the frequency meter notch over each marker and record the corrected frequency meter reading on the test record.

4-2. Output Amplitude Test

SPECIFICATION

Minimum Settable Power: −5 dBm
With Option 002: −60 dBm

Specification	Frequency Bands (GHz)					
	0.01 to 2.4	2.4 to 7.0	7.0 to 13.5	13.5 to 20.0	20.0 to 26.5	0.01 to 26.5
Maximum Leveled Output Power	+10 dBm	+10 dBm	+10 dBm	+10 dBm	+4 dBm	+4 dBm
With Option 002	+10 dBm	+8.5 dBm	+8 dBm	+7 dBm	+1 dBm	+1 dBm
Power Level Accuracy	< ±1.5 dB	< ±1.3 dB	< ±1.3 dB	< ±1.4 dB	< ±1.7 dB	< ±1.8 dB
With Option 002 (at 0 dB attenuator step)	< ±1.7 dB	< ±1.5 dB	< ±1.5 dB	< ±1.6 dB	< ±1.9 dB	< ±2.0 dB
Power Variation (at specified Maximum Leveled Power or below)						
Internally Leveled	±0.9 dB	±0.7 dB	±0.7 dB	±0.8 dB	±0.9 dB	±1.0 dB

DESCRIPTION

A power meter is used to check power level accuracy, maximum leveled output power, and power variations.

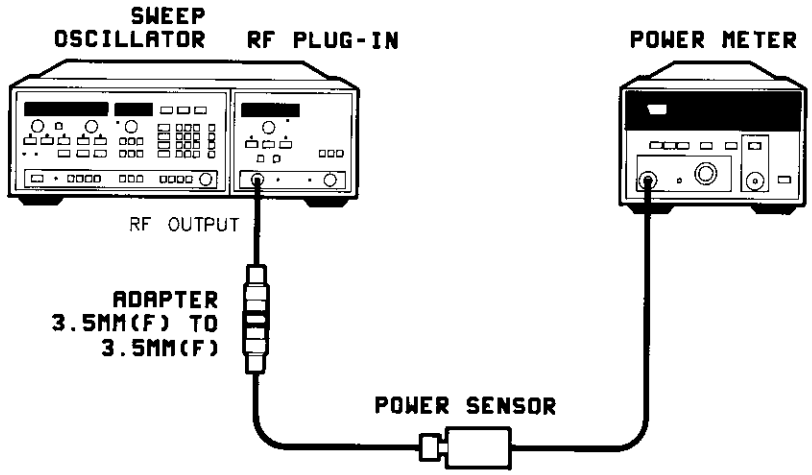


Figure 4-2. Output Amplitude Test Setup

4-2. Output Amplitude Test (Cont'd)

EQUIPMENT

Sweep Oscillator Mainframe ..... HP 8350
Power Meter ..... HP 436A
Power Sensor
10 MHz to 18 GHz ..... HP 8481A
50 MHz to 26.5 GHz ..... HP 8485A
Adapter 3.5 mm (f) to 3.5 mm (f) ..... HP Part No. 1250-1749

PROCEDURE

1. Connect the equipment as shown in Figure 4-2. Do not connect the power meter/sensor to the HP 83595A power output. Allow at least one hour of warm-up.

2. On the power meter/sensor:

   Press **[dBm]** mode.

   Zero and calibrate the power meter. Set the CAL FACTOR to 100%. By leaving the CAL FACTOR set at 100% it ensures minimum specifications will be met.

3. On the sweep oscillator/RF plug-in:

   Press **[INSTR PRESET]**. Press SWEEP **[MAN]**.

Maximum Leveled Power

Table 4-5. Frequency and Power Settings

Frequency Range	Maximum Leveled Power		Power Sweep Range		Power Level Accuracy	
	(Standard)	(Option 002)	(Standard)	(Option 002)	Standard	(Option 002)
0.01 to 2.4 GHz	+10 dBm	+10 dBm	15 dB/SWP	14 dB/SWP	$<\pm$1.5 dB	$<\pm$1.7 dB
2.4 to 7.0 GHz	+10 dBm	+8.5 dBm	15 dB/SWP	13.5 dB/SWP	$<\pm$1.3 dB	$<\pm$1.5 dB
7.0 to 13.5 GHz	+10 dBm	+8 dBm	15 dB/SWP	13 dB/SWP	$<\pm$1.3 dB	$<\pm$1.5 dB
13.5 to 20 GHz	+10 dBm	+7 dBm	15 dB/SWP	12 dB/SWP	$<\pm$1.4 dB	$<\pm$1.6 dB
20.0 to 26.5 GHz	+4 dBm	+1 dBm	9 dB/SWP	6 dB/SWP	$<\pm$1.7 dB	$<\pm$1.9 dB
0.01 to 26.5 GHz	+4 dBm	+1 dBm	9 dB/SWP	6 dB/SWP	$<\pm$1.8 dB	$<\pm$2.0 dB

4. Connect the power meter/sensor to the RF plug-in power output.

5. On the sweep oscillator/RF plug-in:

   Set the start/stop frequencies and power level for the first frequency range listed in Table 4-5.

   Slowly tune the FREQUENCY/TIME control and note the minimum power level in the range. Set the frequency at this low power point, press **[MAN] [X] [X] [.] [X] [X]**.

4-2. Output Amplitude Test (Cont'd)

6. Adjust the POWER LEVEL control for a power meter reading equal to the specified maximum leveled output power (subtract out the attenuation caused by the attenuator). Note and record the power level on the test record.

   Repeat steps 5 and 6 for the remaining frequency ranges listed in Table 4-5.

NOTE: If any readings exceed the specification, repeat the test using the exact CAL FACTOR information listed on the power sensor and the calibration data provided for the attenuator. By using this information you can reduce the measurement uncertainty to ± 0.5 dB.

Output Power Variation

Table 4-6. Output Power Variations

Power Variation (at specified Maximum Leveled Power or below)	**Frequency Range (GHz)**					
	0.01 to 2.4	2.4 to 7.0	7.0 to 13.5	13.5 to 20.0	20.0 to 26.5	0.01 to 26.5
Internally Leveled	±0.9 dB	±0.7 dB	±0.7 dB	±0.8 dB	±0.9 dB	±1.0 dB

7. On the power meter, press **[dB REF]**.
8. On the sweep oscillator/RF plug-in:

   Set the start/stop frequencies and power level for the first frequency range listed in Table 4-6.

   Slowly tune the FREQUENCY/TIME control through the entire frequency range. Note and record the maximum power deviation on the test record.

9. On the power meter, press **[dBm]**. Record the data on the test record.
10. Repeat steps 7 through 9 for the remaining frequency range settings in Table 4-6.

Power Level Accuracy

11. On the sweep oscillator/RF plug-in:

    Set the start/stop frequencies and the power level for the first frequency range in Table 4-5 (0.01 to 2.40 GHz at +10 dBm).

12. Slowly tune the FREQUENCY/TIME control through the entire frequency range and note the maximum power level variations above and below the displayed power level setting. Record these readings on the test record.
13. Press **[POWER LEVEL] [STEP SIZE] [2]**. Use the step down **[▼]** key to step the power down 2 dB.
14. Repeat steps 12 and 13 to check the power level accuracy over the full calibrated range (down to −5 dBm) and record the data on the test record.

4-2. Output Amplitude Test (Cont'd)

15. Repeat steps 11 through 14 at the remaining frequency ranges and power levels listed in Table 4-5.

Power Sweep Range

16. Press the following keys on the sweep oscillator/RF plug-in:

    [START] [1] [0] [MHz]
    [STOP] [2] [.] [4] [GHz]
    [SHIFT] [CW]
    [TIME] [1] [0] [sec]
    [POWER SWEEP] (light on)

17. Adjust the power sweep for maximum leveled power (UNLEVELED light off). Observe the power meter display to verify a power sweep from at least −5 dBm to +10 dBm. Record the power meter level change from start to stop frequencies on the test record.

18. Press **[POWER SWEEP]** to turn the power sweep function off.

19. Repeat steps 16 through 18 at the remaining frequency ranges listed in Table 4-5. Record the results of the power meter level change from start to stop frequencies on the test record.

4-3. Frequency Stability Test

SPECIFICATION

Specification	Frequency Bands (GHz)				
	0.01 to 2.4	2.4 to 7.0	7.0 to 13.5	13.5 to 20.0	20.0 to 26.5
Stability					
With 10% Line Voltage Change	±50 kHz	±50 kHz	±100 kHz	±150 kHz	±200 kHz
With 10 dB Power Level Change	±200 kHz	±200 kHz	±400 kHz	±600 kHz	±800 kHz
With 3:1 Load SWR	±100 kHz	±100 kHz	±200 kHz	±300 kHz	±400 kHz

DESCRIPTION

A frequency counter is used to check frequency change due to output power level changes and load impedance changes.

EQUIPMENT

Sweep Oscillator Mainframe ..... HP 8350
Frequency Counter ..... HP 5343A
10 dB Attenuator ..... HP 8493C Option 010
Short ..... HP 11565A
3 dB Attenuator ..... HP 8493C Option 003
16 dB Coupler ..... HP Part No. 0955-0125
Adapter 3.5 mm (f) to 3.5 mm (f) ..... HP Part No. 1250-1749

4-3. Frequency Stability Test (Cont'd)

PROCEDURE

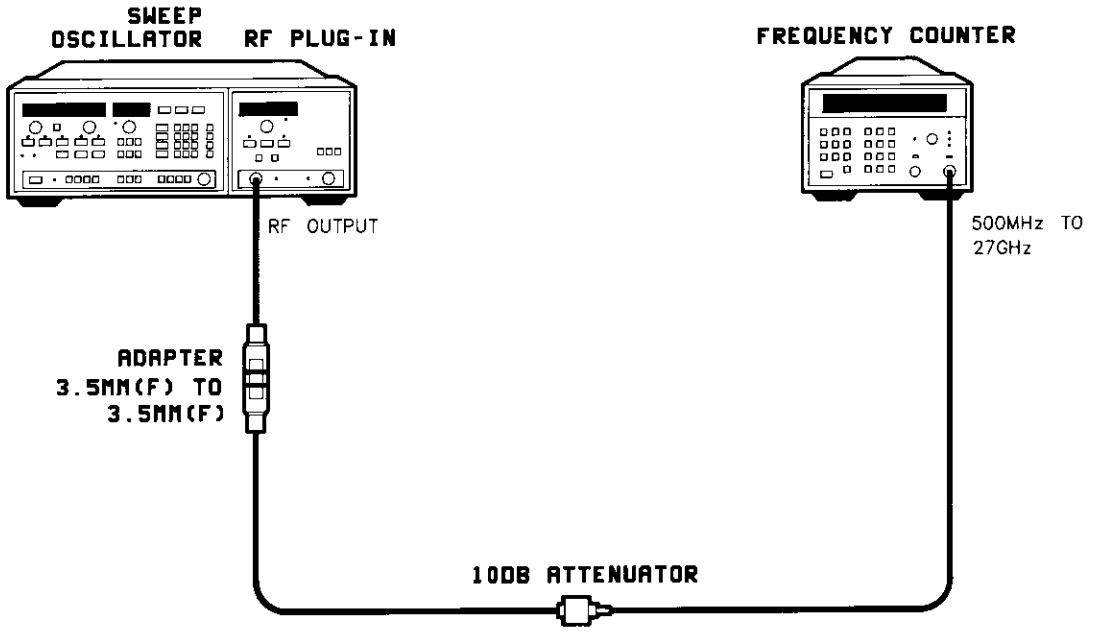


Figure 4-3. Frequency Change with 10 dB Power Level Change Test Setup

Frequency Change with 10 dB Power Level Change

1. Connect the equipment as shown in Figure 4-3. Turn the equipment on and press **[INSTR PRESET]** on the sweep oscillator/RF plug-in. Allow one hour warm-up.
2. On the sweep oscillator/RF plug-in, press:

   [CW] [1] [GHz]

   [POWER LEVEL] [0] [dBm].

   To minimize drift, allow 5 minutes before continuing with the test.
3. On the frequency counter, rotate the SAMPLE RATE knob to HOLD. Press **[SET] [OFS MHz] [Blue Key]**. Rotate the frequency counter SAMPLE RATE knob counterclockwise to its original position.
4. On the sweep oscillator/RF plug-in, press **[POWER LEVEL] [1] [0] [dBm]**.
5. Verify that the frequency change is less than that given in Table 4-7. Record the reading on the test record. Reset the RF plug-in output power to 0 dBm.
6. Repeat steps 2 through 5 for the remaining frequencies listed Table 4-7.

Table 4-7. Frequency Change with 10 dB Power Level Change

Band	CW Frequency	Frequency Change
Band 0	1.0 GHz	±200 kHz
Band 1	6.0 GHz	±200 kHz
Band 2	12.0 GHz	±400 kHz
Band 3	18 GHz	±600 kHz
Band 4	24 GHz	±800 kHz

4-3. Frequency Stability Test (Cont'd)

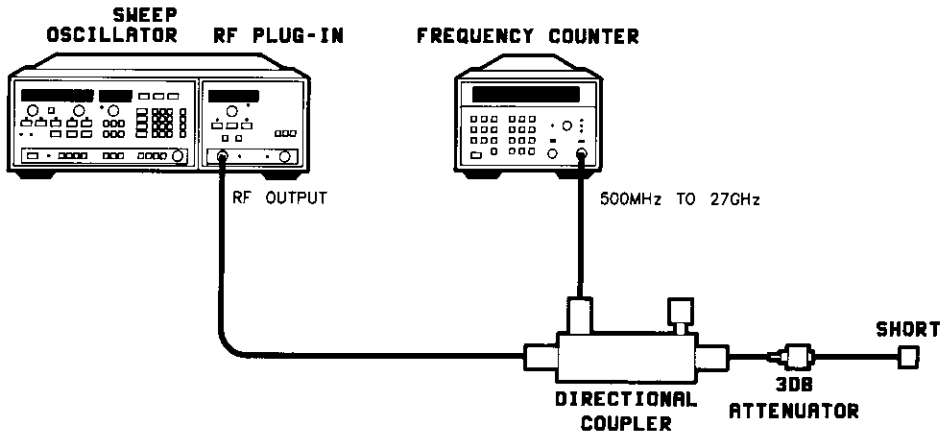


Figure 4-4. Frequency Change with 3:1 Load SWR Test Setup

Frequency Change with 3:1 Load SWR

7. Connect the equipment as shown in Figure 4-4.
8. On the sweep oscillator/RF plug-in:

   Press **[INSTR PRESET] [CW] [1] [GHz]**.

   Press **[POWER LEVEL] [4] [dBm]**. To minimize drift, allow five minutes before continuing with the test.
9. On the frequency counter:

   Rotate the SAMPLE RATE knob to HOLD.

   Press **[SET] [OFS MHz] [Blue Key]**.

   Rotate the frequency counter SAMPLE RATE knob counterclockwise, to its original position.
10. Move the adjustable short through its range and observe the frequency counter for the greatest positive and negative frequency change. Check that the peak-to-peak change is less than that given in Table 4-8. Record the reading on the test record.
11. Repeat steps 8 through 10 for the remaining frequencies listed in Table 4-8.

Table 4-8. Frequency Change with 3:1 Load SWR

Band	CW Frequency	Frequency Change
Band 0	1.0 GHz	±50 kHz
Band 1	6.0 GHz	±50 kHz
Band 2	12.0 GHz	±100 kHz
Band 3	18 GHz	±150 kHz
Band 4	24 GHz	±200 kHz

4-4. Residual FM Test

SPECIFICATION

10 Hz to 10 kHz Bandwidth:	0.01 to 2.4 GHz:	<5 kHz (peak)
(CW mode with CW Filter on)	2.0 to 7.0 GHz:	<5 kHz (peak)
	7.0 to 13.5 GHz:	<7 kHz (peak)
	13.5 to 20.0 GHz:	<9 kHz (peak)
	20.0 to 26.5 GHz:	<12 kHz (peak)

DESCRIPTION

The RF output of the HP 83595A is downconverted by the spectrum analyzer with direct readings made using a measuring receiver.

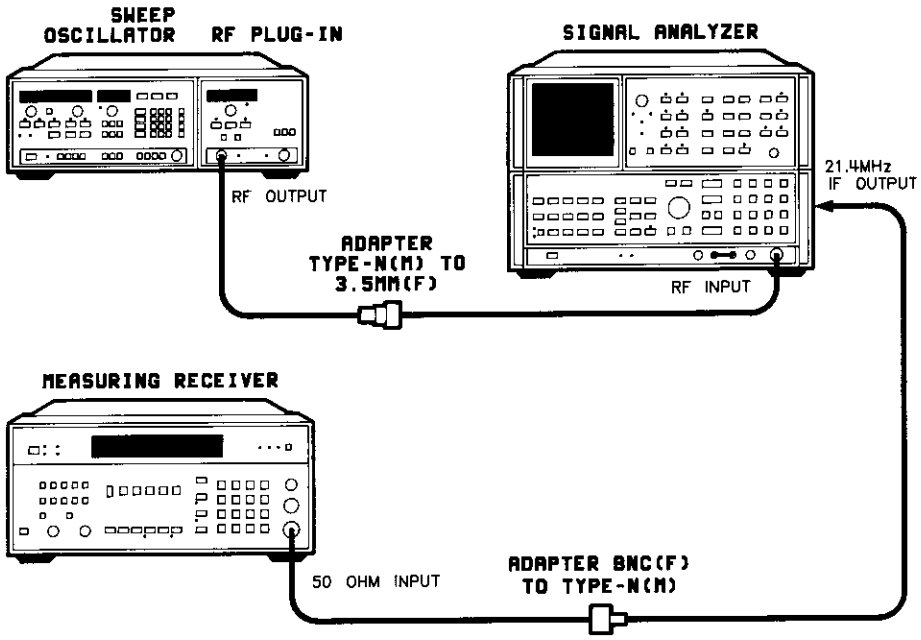


Figure 4-5. Residual FM Test Setup

EQUIPMENT

Sweep Oscillator Mainframe	HP 8350
Spectrum Analyzer	HP 8566B
Measuring Receiver	HP 8902A
Adapter BNC (f) to Type-N (m)	HP Part No. 1250-0780
Adapter Type-N (m) to 3.5 mm (f)	HP Part No. 1250-1744

4-4. Residual FM Test (Cont'd)

PROCEDURE

1. Connect the equipment as shown in Figure 4-5. Allow at least one hour warm-up.
2. On the sweep oscillator/RF plug-in:

   Press **[INSTR PRESET] [CW] [1] [GHz]**. Check that the CW filter is on (light on).
3. On the spectrum analyzer, press the following keys:

   [INSTRUMENT PRESET]
   [CENTER FREQUENCY] [1] [GHz]
   [PEAK SEARCH]
   [MKR→REF LVL]
   [RES BW] [1] [MHz]
   [FREQUENCY SPAN] [5] [0] [GHz]

   Use the PEAK SEARCH and MKR→CF functions as necessary to keep the signal in the center of the screen. Then press:

   [FREQUENCY SPAN] [0] [GHz]

   The spectrum analyzer is now being used as a down converter only.
4. On the measuring receiver, press the following keys:

   [INSTRUMENT PRESET]
   HIGH PASS FILTER **[50 Hz]**
   LOW PASS FILTER **[15 kHz]**
   [FM] [AUTOMATIC OPERATION]
   [PEAK +] [PEAK HOLD]

   Wait 30 seconds and record the displayed residual FM on the test record.
5. Repeat steps 2 through 4 with the CW of the sweep oscillator/RF plug-in and the center frequency of the spectrum analyzer set to 4 GHz, 10 GHz, 15 GHz, and then 21 GHz.

4-4A. Alternate Residual FM Test

DESCRIPTION

The CW RF output signal is slope-detected by using the linear portion of a spectrum analyzer resolution bandwidth filter in the zero-span mode.

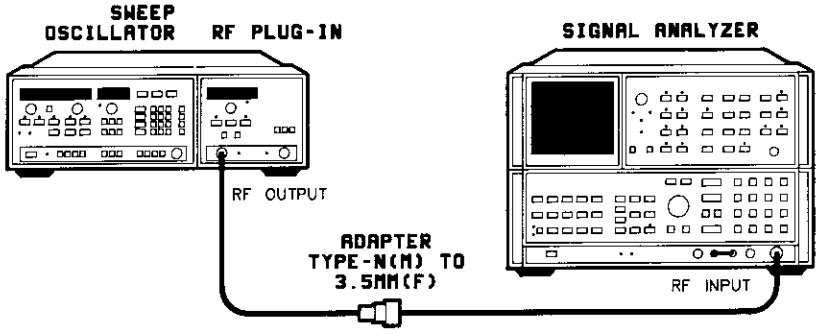


Figure 4-5A. Residual FM Test Setup

EQUIPMENT

Sweep Oscillator Mainframe	HP 8350
Spectrum Analyzer	HP 8566B
Adapter 3.5 mm (f) to Type-N (m)	HP Part No. 1250-1744

PROCEDURE

1A. Connect the equipment as shown in Figure 4-5A. Allow equipment to warm up for 30 minutes.

2A. On the sweep oscillator/RF plug-in, press the following keys:

[INSTR PRESET]
[CW] [4] [GHz]

3A. On the spectrum analyzer, press the following keys:

[INSTRUMENT PRESET]
[CENTER FREQUENCY] [4] [GHz]
[FREQUENCY SPAN] [5] [0] [MHz]
[PEAK SEARCH]
[MKR→CF]
[MKR→REF LVL]
[VIDEO BW] [1] [0] [kHz]
[RES BW] [1] [0] [0] [kHz]
SCALE **[LIN]**

4-4A. Alternate Residual FM Test (Cont'd)

Use the PEAK SEARCH and MKR→CF functions as necessary to keep the signal in the center of the screen.

Press **[FREQUENCY SPAN]** and step **[◆]** key to span down. When the frequency span is at the lowest span, press the following keys:

[FREQUENCY SPAN] [0] [Hz]
[SWEEP TIME] [1] [0] [sec]

4A. Press **[CENTER FREQUENCY]** and use the RPG (Rotary Pulse Generator) control to keep the signal between the 5th and 8th division from bottom screen. Refer to Figure 4-6.

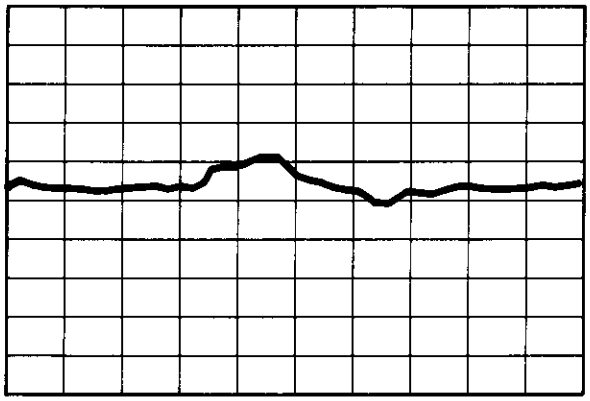


Figure 4-6. Residual FM Signal as displayed on a Spectrum Analyzer

5A. Note the maximum peak-to-peak deviation to verify the residual FM is within tolerance and record the data on the test record.

NOTE: The vertical sensitivity (5th through 8th graticules only) is 11.1 kHz/div.

6A. Repeat steps 2A through 5A with the CW of the sweep oscillator/RF plug-in and the center frequency of the spectrum analyzer set to 4 GHz, 10 GHz, 15 GHz, and then 21 GHz. Record the results on the test record.

4-5. Spurious Signal Test

SPECIFICATION (below the fundamental at specified maximum leveled power; 20°to 30°C).

Spurious Signals (at specified Maximum Leveled Power)	Frequency Range (GHz)					
	0.01 to 2.4	2.4 to 7.0	7.0 to 13.5	13.5 to 20.0	20.0 to 26.5	0.01 to 26.5
Harmonics or Subharmonics (in dB below carrier)	>25 dB	>25 dB	>25 dB	>25 dB	>20 dB	>20 dB
Non-Harmonics	>25 dB	>50 dB	>50 dB	>50 dB	>50 dB	>25 dB

DESCRIPTION

The RF output signal from the sweep oscillator is displayed on a spectrum analyzer to verify that harmonic and non-harmonic spurious signals are at or below the specified level.

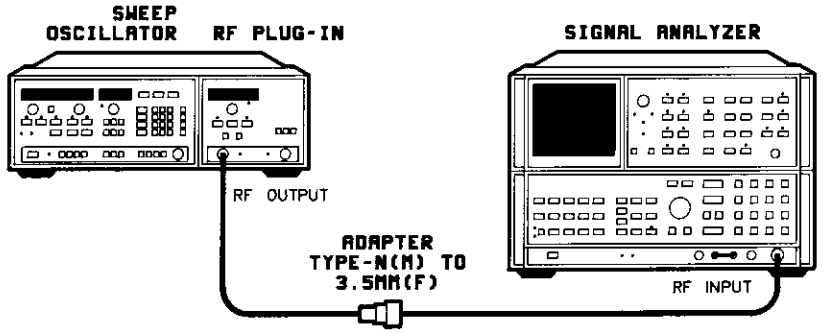


Figure 4-7. Spurious Signals Test Setup

EQUIPMENT

Sweep Oscillator Mainframe ..... HP 8350
Spectrum Analyzer ..... HP 8566B
Adapter Type-N (f) to 3.5 mm (f) ..... HP Part No. 1250-1745

PROCEDURE

1. Connect the equipment as shown in Figure 4-7 and allow at least one hour warm-up.

4-5. Spurious Signal Test (Cont'd)

2. On the spectrum analyzer press the following keys:

   [INSTR PRESET]
   [ATTEN] [3] [0] [+ dBm]
   [REFERENCE LEVEL] [1] [0] [+dBm].

3. On the sweep oscillator/RF plug-in press:

   [INSTR PRESET]
   [START] [1] [0] [MHz]
   [STOP] [2] [.] [4] [GHz]
   [CW] [1] [0] [MHz]. Check that CW Filter is on (light on).
   [POWER LEVEL] [1] [0] [dBm].

4. On the sweep oscillator/RF plug-in, adjust the CW control through the entire RF plug-in frequency range (0.01 to 2.4 GHz) and check for harmonic and non-harmonic spurious signals (see SPECIFICATIONS). Record the data on the test record.

5. Repeat step 4 for sweep ranges of 2.4 to 7.0, 7.0 to 13.5 GHz, 13.5 to 20 GHz and then at +4 dBm for 20.0 to 26.5 GHz. Record the results on the test record.

NOTE: The spectrum analyzer originates some mixing products that may appear on the display. To determine if a signal is a mixing product, increase the spectrum analyzer input attenuation by 10 dB and note if the signal decreases in amplitude by 10 dB. Return the attenuation to the original position. If the signal in question comes from an external source, it will change by 10 dB as the attenuation is increased. If the signal in question originates in the spectrum analyzer, the signal level will change by greater or less than 10 dB, or it will not change at all.

Rotating the HP 8350 CW control can generate noise spikes. These signals should disappear when you stop rotating the CW control.

If you find a spurious signal that appears out of specifications, first ensure that the fundamental signal amplitude is at the maximum specified power level, then check the spurious level by substituting a known amplitude signal on the spectrum analyzer.

4-6. External Frequency Modulation Test

SPECIFICATION

Modulation Frequency	Cross-Over Coupled	Direct Coupled
DC to 100 Hz:	±75 MHz	±12 MHz
100 Hz to 1 MHz:	±7 MHz	±7 MHz
1 MHz to 2 MHz:	±5 MHz	±5 MHz
2 MHz to 10 MHz:	±1 MHz	±1 MHz

DESCRIPTION

The RF output is modulated with a 100 Hz, 1 MHz, 2 MHz, and 10 MHz external signal. The 100 Hz deviation is measured directly on a spectrum analyzer. The deviation at higher frequencies is measured using a delay line discriminator and an oscilloscope to observe an increase in the modulation until distortion occurs. The frequency change is measured on a frequency counter.

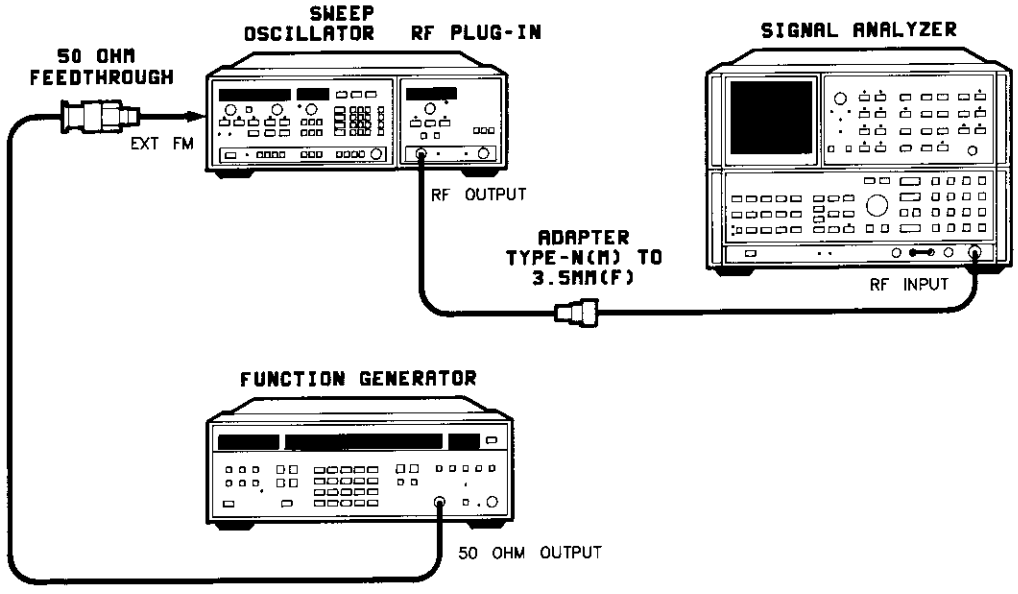


Figure 4-8. 100 Hz External Frequency Modulation Test Setup

4-6. External Frequency Modulation Test (Cont'd)

EQUIPMENT

Sweep Oscillator Mainframe	HP 8350
Spectrum Analyzer	HP 8566B
Oscilloscope	HP 1741A
Frequency Counter	HP 5343A
Function Generator/Synthesizer	HP 3325A
10 dB Attenuator	HP 8493C Option 010
Power Splitter	HP 11667B
Delay Line Discriminator	See Figure 1-3
50 Ohm Feedthru Termination	HP 10100C
BNC tee	HP Part No. 1250-1781
Adapter Type-N (m) to 3.5 mm (f)	HP Part No. 1250-1744

PROCEDURE

100 Hz Modulation

1. Ensure that the RF plug-in configuration switch (A3S1) is set to −20 MHz/V, Direct Coupled FM (see Section 5, for details on how to set A3S1).

2. Connect the equipment as shown in Figure 4-8. Turn all instruments on and allow them to warm-up for 30 minutes.

3. On the sweep oscillator/RF plug-in:

   Press **[INSTR PRESET]** and **[CW] [1] [GHz]**.

   Press **[DISPL BLANK]** to turn off the display blanking (light off).

   Press **[CW FILTER]** to turn the filter off (light off).

4. On the spectrum analyzer press:

   [INSTRUMENT PRESET] [0-2.5 GHz].
   [PEAK SEARCH] [SIGNAL TRACK] [MKR→CF]
   [FREQUENCY SPAN] [1] [GHz] [SIGNAL TRACK].

5. On the function generator/synthesizer:

   Set the frequency to a 100 Hz sinewave, with minimum amplitude.

   Use the modify and step up keys to slowly increase the amplitude. Monitor the signal on the spectrum analyzer. Deviation from the center line should be symmetrical at first, and become non-symmetrical as deviation increases.

6. Note the point at which the deviation becomes non-symmetrical and verify that the modulation is greater than ±12 MHz. Record this reading on the test record.

4-6. External Frequency Modulation Test (Cont'd)

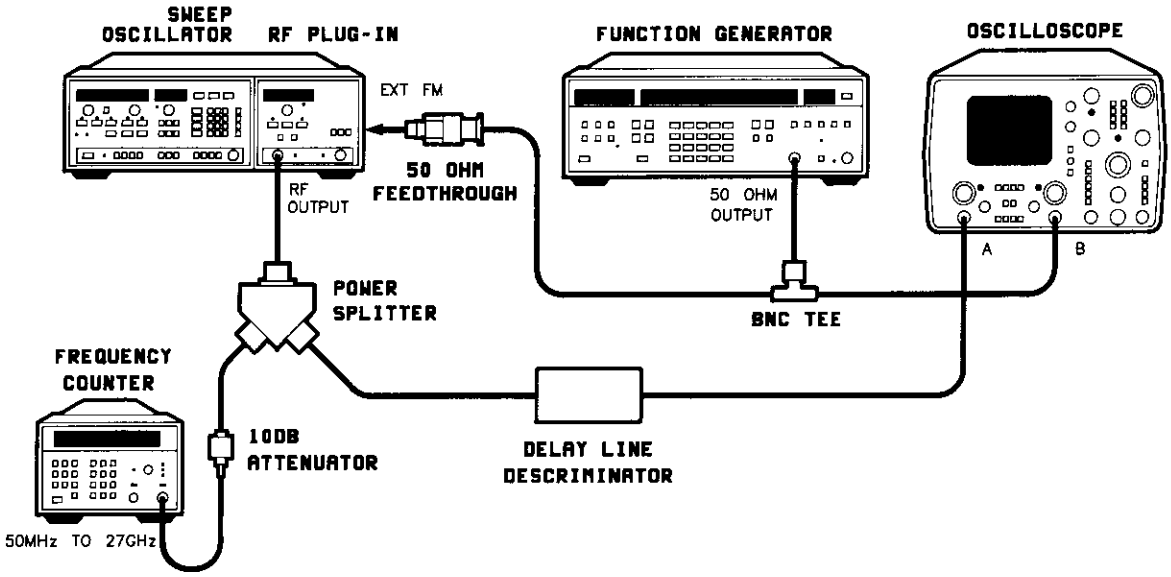


Figure 4-9. Test Setup for >100 Hz Frequency Modulation

FM Modulation >100 Hz

7. Connect the equipment as shown in Figure 4-9. Do not connect the function generator/synthesizer.

8. On the oscilloscope, set both inputs to 50 ohms.

9. On the functon generator/synthesizer, set the frequency to 1 MHz. Set the output amplitude to 0.1 volt peak-to-peak.

10. On the sweep oscillator/RF plug-in:

    Press **[CW]** and adjust the CW VERNIER for a delay line discriminator output of 0V, as observed on Channel A of the oscilloscope. Note the frequency counter reading.

11. Connect the function generator/synthesizer output to the rear panel FM INPUT, and adjust the oscilloscope (Channel A) for a clear display of the function generator/synthesizer sinewave. If the output is offset, the test is invalid.

12. On the function generator/synthesizer, increase the output amplitude until the deviation displayed on Channel A becomes non-symmetrical or distorted. Use the oscilloscope Channel B to monitor the function generator/synthesizer output.

13. On the oscilloscope, mark the positive and negative peaks of the sinewave displayed on Channel A with a grease pencil.

4-6. External Frequency Modulation Test (Cont'd)

14. On the sweep oscillator/RF plug-in, disconnect the function generator/synthesizer from the FM INPUT, and adjust the CW/CW VERNIER to the grease pencil marks. Note the frequency counter readings.

15. Calculate the difference between the frequency counter reading in step 10 and the readings in step 14. Verify that the difference is greater than ± 7 MHz. Record this reading on the test record.

16. Set the function generator/synthesizer to 2 MHz then 10 MHz repeating steps 9 through 15 for each frequency and record the results on the test record.

4-7. Square-Wave On/Off Ratio and Symmetry Test

SPECIFICATION

On/Off Ratio:	≥ 30 dB
Symmetry:	40/60

DESCRIPTION

The On/Off ratio is checked on the amplitude axis of a video triggered spectrum analyzer display. The symmetry is checked by calculating the On/Off ratio on the horizontal axis.

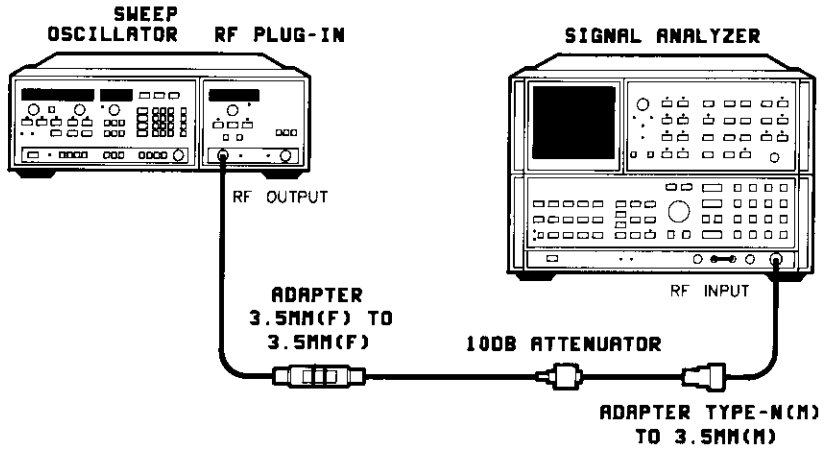


Figure 4-10. AM On/Off Ratio and Square-Wave Symmetry Test Setup

EQUIPMENT

Sweep Oscillator Mainframe	HP 8350
10 dB Attenuator	HP 8493C Option 010
Spectrum Analyzer	HP 8566B
Adapter 3.5 mm (f) to 3.5 mm (f)	HP Part No. 1250-1749

PROCEDURE

1. Connect the equipment as shown in Figure 4-10. Turn all instruments on and allow them to warm-up for 30 minutes.
2. On the sweep oscillator/RF plug-in:

   Press **[INSTR PRESET] [CW] [4] [GHz]**.

   Press **[POWER LEVEL] [1] [0] [dBm]**.

   Press **[⌐¬MOD]** to turn square-wave modulation on (light on).

4-7. Square-Wave On/Off Ratio and Symmetry Test (Cont'd)

3. On the spectrum analyzer, press the following keys:

   [INSTRUMENT PRESET]
   [CENTER FREQUENCY] [4] [GHz]
   [PEAK SEARCH]
   [MKR→REF LVL]
   [SIGNAL TRACK]
   [ATTEN] verify or set **[1] [0] [+dBm]**
   [FREQUENCY SPAN] [5] [0] [MHz]
   [RES BW] verify or set **[3] [MHz]**
   [ZOOM]
   [FREQUENCY SPAN] [0] [GHz]
   [SIGNAL TRACK]
   TRIGGER **[VIDEO]**
   For 1kHz: SWEEP **[TIME] [.] [5] [msec]**.
   For 27.775 kHz: SWEEP **[TIME] [5] [0] [μsec]**

4. On the spectrum analyzer, adjust the reference level, if necessary, to set the signal to the top of the display. Adjust the video trigger LEVEL for a stable signal. Verify that the On/Off ratio (peak-to-peak signal variation) is greater than the value given on the test record.

5. Verify that the square-wave symmetry is between 40 and 60 percent. Record the data on the test record.

4-8. Step Attenuator Accuracy (Option 002) Test

SPECIFICATION

Accuracy (± dB referenced from the 0 dB setting):

Attenuator Accuracy	Frequency Range (GHz)	Attenuator Setting (dB)										
		5	10	15	20	25	30	35	40	45	50	55
(±dB referenced from the 0 dB setting)	0.01 to 12.4 GHz	0.4	0.6	0.7	0.7	0.9	0.9	1.8	1.8	2.0	2.0	2.2
	12.4 to 18 GHz	0.5	0.7	0.9	0.9	1.2	1.2	2.0	2.0	2.3	2.3	2.5
	18 to 26.5 GHz	0.7	1.0	2.5	2.5	3.0	3.0	4.2	4.2	4.4	4.4	4.6

DESCRIPTION

The HP 83595A RF output is compared to a specially calibrated attenuator and displayed on a spectrum analyzer.

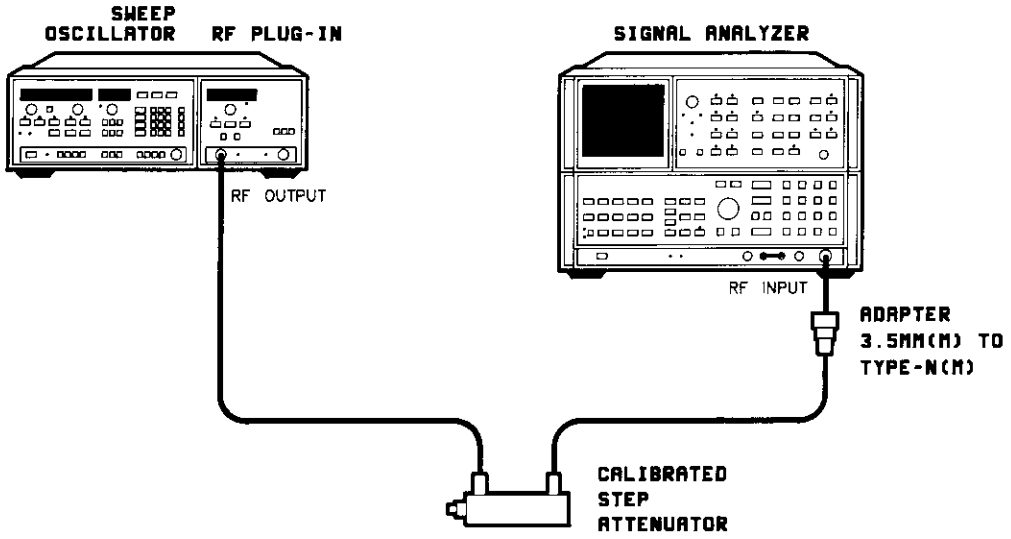


Figure 4-11. Attenuator Accuracy Test Setup

4-8. Step Attenuator Accuracy (Option 002) Test (Cont'd)

EQUIPMENT

Sweep Oscillator Mainframe	HP 8350
Step Attenuator	HP 8495A Option 890
Spectrum Analyzer	HP 8566B
Adapter Type-N (m) to 3.5 mm (m)	HP Part No. 1250-1743

PROCEDURE

1. Connect the equipment as shown in Figure 4-11. Turn the instruments on and allow 30 minutes to warm-up.

2. On the sweep oscillator/RF plug-in press:

   [INSTR PRESET]
   [CW] [5] [GHz]
   [POWER LEVEL] [1] [0] [dBm]
   [SHIFT] [SLOPE] (allows independent control of internal step attenuator).

3. Set the step attenuator to 50 dB.

4. On the spectrum analyzer, press the following keys:

   [INSTRUMENT PRESET]
   [CENTER FREQUENCY] [5] [GHz]
   [ATTEN] [0] [+dBm]
   [REFERENCE LEVEL] [5] [0] [-dBm]
   [RES BW] [1] [0] [0] [kHz]
   [VIDEO BW] [1] [0] [kHz]
   [FREQUENCY SPAN] [↑] until the signal is in view.
   [VIDEO BW] [1] [0] [0] [Hz]
   [ENTER dB/DIV] [2] [+dBm]

5. On the sweep oscillator/RF plug-in:

   Press **[POWER LEVEL] [STEP SIZE] [1] [0] [dBm]**.

6. Note the actual attenuation values on the step attenuator calibration report (option 890), at the frequency and attenuation steps in Table 4-10. Calculate the reference attenuator error for each step:

   Attenuation Error = (CRA − CSA) − (RS − SS)
   CRA = Calibrated Reference Attenuator
   CSA = Calibrated Step Attenuator
   RS = Reference Setting
   SS = Step Setting

For example, for a reference setting of 70 dB, the calculation for the 30 dB step setting is:

RS = 50 dB
SS = 30 dB

The calibration report says that:

The 70 dB setting = 69.55 dB
The 30 dB setting = 30.80 dB

Attenuation Error = (69.55 − 30.80) − (70 − 30)
= −1.25 dB

7. On the spectrum analyzer:

   Press **[PEAK SEARCH] [MKR→CF] [Δ]**.

8. On the sweep oscillator/RF plug-in:

   Press the step down **[▼]** key to increase the RF plug-in attenuation by 10 dB.

   At the same time, decrease the attenuation on the step attenuator by 10 dB.

9. Wait for the spectrum analyzer to sweep 5 times before reading the measurement. Record the power level variation from the spectrum analyzer display window.

10. Algebraically add the attenuation error and deviation from the 0 reference, and record the sum in Table 4-10. Repeat steps 8 through 10 for the other attenuation values.

11. Repeat the entire procedure with the sweep oscillator/RF plug-in CW and the spectrum analyzer CF set to 15 GHz and then again for 19 GHz. Record the results on the test record.

Table 4-9. Attenuator Accuracy

Attenuator Accuracy	Frequency Range (GHz)	Attenuator Setting (dB)										
		5	10	15	20	25	30	35	40	45	50	55
(±dB referenced from the 0 dB setting)	0.01 to 12.4 GHz	0.4	0.6	0.7	0.7	0.9	0.9	1.8	1.8	2.0	2.0	2.2
	12.4 to 18 GHz	0.5	0.7	0.9	0.9	1.2	1.2	2.0	2.0	2.3	2.3	2.5
	18 to 26.5 GHz	0.7	1.0	2.5	2.5	3.0	3.0	4.2	4.2	4.4	4.4	4.6

Table 4-10. Performance Test Record (1 of 9)

HP 83595A RF PLUG-IN Tested by_____

Serial No._____ Date_____

Humidity*_____ Temperature*_____

(*optional)

SPECIFICATIONS TESTED Limits	Step	TEST Conditions	LOWER LIMIT	MEASURED VALUE	UPPER LIMIT
4-1. FREQUENCY RANGE AND ACCURACY TEST					
Frequency Range	3.	Start Frequency = 10 MHz			
	4.	Stop Frequency = 26.5 GHz			
CW Frequency Accuracy	5.	CW Frequency = 10 MHz	5 MHz		15 MHz
		CW Frequency = 1.0 GHz	.995 GHz		1.005 GHz
		CW Frequency = 2.4 GHz	2.395 GHz		2.405 GHz
		CW Frequency = 4.0 GHz	3.995 GHz		4.005 GHz
		CW Frequency = 2.5 GHz	2.495 GHz		2.505 GHz
		CW Frequency = 7.0 GHz	6.995 GHz		7.005 GHz
		CW Frequency = 10.0 GHz	9.99 GHz		10.01 GHz
		CW Frequency = 7.1 GHz	7.09 GHz		7.11 GHz
		CW Frequency = 13.5 GHz	13.49 GHz		13.51 GHz
		CW Frequency = 17.0 GHz	16.99 GHz		17.01 GHz
		CW Frequency = 14.0 GHz	13.99 GHz		14.01 GHz
		CW Frequency = 20.0 GHz	19.99 GHz		20.01 GHz
		CW Frequency = 24.0 GHz	23.988 GHz		24.012 GHz
		CW Frequency = 21.0 GHz	20.988 GHz		21.012 GHz
		CW Frequency = 26.5 GHz	26.488 GHz		26.512 GHz
Swept Frequency Accuracy					
Full Band	8./3A.	Start 10 MHz ± 50 MHz	0 MHz		60 MHz
	9./4A.	Stop 26.5 GHz ± 50 MHz	26.45 GHz		26.55 GHz
Band 0	8./3A.	Start 10 MHz ± 15 MHz	0 MHz		25 MHz
	9./4A.	Stop 2.4 GHz ± 15 MHz	2.385 GHz		2.415 GHz
Band 1	8./3A.	Start 2.4 GHz ± 20 MHz	2.38 GHz		2.420 GHz
	9./4A.	Stop 7.0 GHz ± 20 MHz	6.98 GHz		7.02 GHz
Band 2	8./3A.	Start 7.0 GHz ± 25 MHz	6.975 GHz		7.025 GHz
	9./4A.	Stop 13.5 GHz ± 25 MHz	13.475 GHz		13.525 GHz
Band 3	8./3A.	Start 13.5 GHz ± 30 MHz	13.47 GHz		13.53 GHz
	9./4A.	Stop 20.0 GHz ± 30 MHz	19.97 GHz		20.03 GHz
Band 4	8./3A.	Start 20.0 GHz ± 35 MHz	19.965 GHz		20.035 GHz
	9./4A.	Stop 26.5 GHz ± 35 MHz	26.465GHz		26.535 GHz

Table 4-10. Performance Test Record (2 of 9)

SPECIFICATIONS TESTED Limits	Step	TEST Conditions	LOWER LIMIT	MEASURED VALUE	UPPER LIMIT
4-1. FREQUENCY RANGE AND ACCURACY TEST (cont'd.)					
Frequency Marker Accuracy					
Full Band	12./6A.	M1 at 1 GHz	.81755 GHz	_____	1.18245 GHz
		M2 at 4 GHz	3.81755 GHz	_____	4.18245 GHz
		M3 at 12 GHz	11.81755 GHz	_____	12.18245 GHz
		M4 at 18 GHz	17.81755 GHz	_____	18.18245 GHz
		M5 at 24 GHz	23.81755 GHz	_____	24.18245 GHz
Band 0		M1 at 1 GHz	.97305 GHz	_____	1.02695 GHz
		M2 at 2 GHz	1.97305 GHz	_____	2.02695 GHz
Band 1		M1 at 3 GHz	2.957 GHz	_____	3.043 GHz
		M2 at 6 GHz	5.957 GHz	_____	6.043 GHz
Band 2		M1 at 8 GHz	7.9425 GHz	_____	8.0575 GHz
		M2 at 12 GHz	11.9425 GHz	_____	12.0575 GHz
Band 3		M1 at 15 GHz	14.9375 GHz	_____	15.0625 GHz
		M2 at 18 GHz	17.9375 GHz	_____	18.0625 GHz
Band 4		M1 at 21 GHz	20.9175 GHz	_____	21.0825 GHz
		M2 at 25 GHz	24.9175 GHz	_____	25.0825 GHz
4-2. OUTPUT AMPLITUDE TEST Standard or Option 004					
Maximum Leveled Power	6.				
0.01 to 2.4 GHz		+10 dBm	+10 dBm	_____	
2.4 to 7.0 GHz		+10 dBm	+10 dBm	_____	
7.0 to 13.5 GHz		+10 dBm	+10 dBm	_____	
13.5 to 20.0 GHz		+10 dBm	+10 dBm	_____	
20.0 to 26.5 GHz		+4 dBm	+4 dBm	_____	
0.01 to 26.5 GHz		+4 dBm	+4 dBm	_____	
Output Power Variation					
0.01 to 2.4 GHz	9.	+10.0 dBm	+9.1 dBm	_____	+10.9 dBm
2.4 to 7.0 GHz		+10.0 dBm	+9.3 dBm	_____	+10.7 dBm
7.0 to 13.5 GHz		+10.0 dBm	+9.3 dBm	_____	+10.7 dBm
13.5 to 20.0 GHz		+10.0 dBm	+9.2 dBm	_____	+10.8 dBm
20.0 to 26.5 GHz		+4 dBm	+3.1 dBm	_____	+4.9 dBm
0.01 to 26.5 GHz		+4 dBm	+3.0 dBm	_____	+5.0 dBm

Table 4-10. Performance Test Record (3 of 9)

SPECIFICATIONS TESTED Limits	Step	TEST Conditions	LOWER LIMIT	MEASURED VALUE	UPPER LIMIT
4-2. OUTPUT AMPLITUDE TEST (cont'd.)					
Power Level Accuracy					
0.01 to 2.4 GHz	12.	+10 dBm	+8.5 dBm	_____	+11.5 dBm
	14.	+8 dBm	+6.5 dBm	_____	+9.5 dBm
		+6 dBm	+4.5 dBm	_____	+7.5 dBm
		+4 dBm	+2.5 dBm	_____	+5.5 dBm
		+2 dBm	+0.5 dBm	_____	+3.5 dBm
		0 dBm	−1.5 dBm	_____	+1.5 dBm
		−2 dBm	−3.5 dBm	_____	−0.5 dBm
		−4 dBm	−5.5 dBm	_____	−2.5 dBm
		−5 dBm	−6.5 dBm	_____	−3.5 dBm
2.4 to 7.0 GHz	15.	+10 dBm	+8.7 dBm	_____	+11.3 dBm
		+8 dBm	+6.7 dBm	_____	+9.3 dBm
		+6 dBm	+4.7 dBm	_____	+7.3 dBm
		+4 dBm	+2.7 dBm	_____	+5.3 dBm
		+2 dBm	+0.7 dBm	_____	+3.3 dBm
		0 dBm	−1.3 dBm	_____	+1.3 dBm
		−2 dBm	−3.3 dBm	_____	−0.7 dBm
		−4 dBm	−5.3 dBm	_____	−2.7 dBm
		−5 dBm	−6.3 dBm	_____	−3.7 dBm
7.0 to 13.5 GHz		+10 dBm	+8.7 dBm	_____	+11.3 dBm
		+8 dBm	+6.7 dBm	_____	+9.3 dBm
		+6 dBm	+4.7 dBm	_____	+7.3 dBm
		+4 dBm	+2.7 dBm	_____	+5.3 dBm
		+2 dBm	+0.7 dBm	_____	+3.3 dBm
		0 dBm	−1.3 dBm	_____	+1.3 dBm
		−2 dBm	−3.3 dBm	_____	−0.7 dBm
		−4 dBm	−5.3 dBm	_____	−2.7 dBm
		−5 dBm	−6.3 dBm	_____	−3.7 dBm

Table 4-10. Performance Test Record (4 of 9)

SPECIFICATIONS TESTED Limits	Step	TEST Conditions	LOWER LIMIT	MEASURED VALUE	UPPER LIMIT
4-2. OUTPUT AMPLITUDE TEST (cont'd.)					
13.5 to 20.0 GHz	15.	+10 dBm	+8.6 dBm	_____	+11.4 dBm
		+8 dBm	+6.6 dBm	_____	+9.4 dBm
		+6 dBm	+4.6 dBm	_____	+7.4 dBm
		+4 dBm	+2.6 dBm	_____	+5.4 dBm
		+2 dBm	+0.6 dBm	_____	+3.4 dBm
		0 dBm	−1.4 dBm	_____	+1.4 dBm
		−2 dBm	−3.4 dBm	_____	−0.6 dBm
		−4 dBm	−5.4 dBm	_____	−2.6 dBm
		−5 dBm	−6.4 dBm	_____	−3.6 dBm
20.0 to 26.5 GHz		+4 dBm	+2.3 dBm	_____	+5.7 dBm
		+2 dBm	+0.3 dBm	_____	+3.7 dBm
		0 dBm	−1.7 dBm	_____	+1.7 dBm
		−2 dBm	−3.7 dBm	_____	−0.3 dBm
		−4 dBm	−5.7 dBm	_____	−2.3 dBm
		−5 dBm	−6.7 dBm	_____	−3.3 dBm
0.01 to 26.5 GHz		+4 dBm	+2.2 dBm	_____	+5.8 dBm
		+2 dBm	+0.2 dBm	_____	+3.8 dBm
		0 dBm	−1.8 dBm	_____	+1.8 dBm
		−2 dBm	−3.8 dBm	_____	−0.2 dBm
		−4 dBm	−5.8 dBm	_____	−2.2 dBm
		−5 dBm	−6.8 dBm	_____	−3.2 dBm
Power Sweep					
	17.	0.01 to 2.4 GHz	15 dB	_____	
	19.	2.4 to 7.0 GHz	13.5 dB	_____	
		7.0 to 13.5 GHz	13 dB	_____	
		13.5 to 20.0 GHz	12 dB	_____	
		20.0 to 26.5Hz	6 dB	_____	
		0.01 to 26.5 GHz	6 dB	_____	

Table 4-10. Performance Test Record (5 of 9)

SPECIFICATIONS TESTED Limits	Step	TEST Conditions	LOWER LIMIT	MEASURED VALUE	UPPER LIMIT
4-2. OUTPUT AMPLITUDE TEST Option 002					
Maximum Leveled Power	6.				
0.01 to 2.4 GHz		+10 dBm	+10 dBm	_____	
2.4 to 7.0 GHz		+8.5 dBm	+8.5 dBm	_____	
7.0 to 13.5 GHz		+8.0 dBm	+8.0 dBm	_____	
13.5 to 20.0 GHz		+7.0 dBm	+7.0 dBm	_____	
20.0 to 26.5 GHz		+1.0 dBm	+1.0 dBm	_____	
0.01 to 26.5 GHz		+1.0 dBm	+1.0 dBm	_____	
Output Power Variation					
0.01 to 2.4 GHz	9.	+10.0 dBm	+9.1 dBm	_____	+10.1 dBm
2.4 to 7.0 GHz		+8.5 dBm	+7.8 dBm	_____	+9.2 dBm
7.0 to 13.5 GHz		+8.0 dBm	+7.3 dBm	_____	+8.7 dBm
13.5 to 20.0 GHz		+7.0 dBm	+6.2 dBm	_____	+7.8 dBm
20.0 to 26.5 GHz		+1.0 dBm	+0.1 dBm	_____	+1.9 dBm
0.01 to 26.5 GHz		+1.0 dBm	+0.1 dBm	_____	+1.9 dBm
Power Level Accuracy					
0.01 to 2.4 GHz	12.	+10 dBm	+8.3 dBm	_____	+11.7 dBm
	14.	+8 dBm	+6.3 dBm	_____	+9.7 dBm
		+6 dBm	+4.3 dBm	_____	+7.7 dBm
		+4 dBm	+2.3 dBm	_____	+5.7 dBm
		+2 dBm	+0.3 dBm	_____	+3.7 dBm
		0 dBm	−1.7 dBm	_____	+1.7 dBm
		−2 dBm	−3.7 dBm	_____	−0.3 dBm
		−4 dBm	−5.7 dBm	_____	−2.3 dBm
		−5 dBm	−6.7 dBm	_____	−3.3 dBm
2.4 to 7.0 GHz	15.	+8.5 dBm	+7.0 dBm	_____	+10 dBm
		+6.5 dBm	+5.0 dBm	_____	+8 dBm
		+4.5 dBm	+3.0 dBm	_____	+6 dBm
		+2.5 dBm	+1.0 dBm	_____	+4 dBm
		+0.5 dBm	−1.0 dBm	_____	+ 2 dBm
		−1.5 dBm	−3.0 dBm	_____	0 dBm
		−3.5 dBm	−5.0 dBm	_____	−2 dBm
		−5 dBm	−6.5 dBm	_____	−3.5 dBm

Table 4-10. Performance Test Record (6 of 9)

SPECIFICATIONS TESTED Limits	Step	TEST Conditions	LOWER LIMIT	MEASURED VALUE	UPPER LIMIT
4-2. OUTPUT AMPLITUDE TEST (cont'd.)					
7.0 to 13.5 GHz		+8.0 dBm	+6.5 dBm	_____	+9.5 dBm
		+6.0 dBm	+4.5 dBm	_____	+7.5 dBm
		+4.0 dBm	+2.5 dBm	_____	+5.5 dBm
		+2.0 dBm	+0.5 dBm	_____	+3.5 dBm
		0 dBm	−1.5 dBm	_____	+1.5 dBm
		−2.0 dBm	−3.5 dBm	_____	−0.5 dBm
		−4.0 dBm	−5.5 dBm	_____	−2.5 dBm
		−5.0 dBm	−6.5 dBm	_____	−3.5 dBm
13.5 to 20.0 GHz	15.	+7.0 dBm	+5.4 dBm	_____	+8.6 dBm
		+5.0 dBm	+3.4 dBm	_____	+6.6 dBm
		+3.0 dBm	+1.4 dBm	_____	+4.6 dBm
		+1.0 dBm	−0.6 dBm	_____	+2.6 dBm
		−1.0 dBm	−2.6 dBm	_____	+0.6 dBm
		−3.0 dBm	−4.6 dBm	_____	−1.4 dBm
		−5.0 dBm	−6.6 dBm	_____	−3.4 dBm
20.0 to 26.5 GHz		+1.0 dBm	−0.9 dBm	_____	+2.9 dBm
		−1.0 dBm	−2.9 dBm	_____	+0.9 dBm
		−3.0 dBm	−4.9 dBm	_____	−1.1 dBm
		−5.0 dBm	−6.9 dBm	_____	−3.1 dBm
0.01 to 26.5 GHz		+1.0 dBm	−1.0 dBm	_____	+3.0 dBm
		−1.0 dBm	−3.0 dBm	_____	+1.0 dBm
		−3.0 dBm	−5.0 dBm	_____	−1.0 dBm
		−5.0 dBm	−7.0 dBm	_____	−3.0 dBm
Power Sweep					
	17.	0.01 to 2.4 GHz	15 dB	_____	
	19.	2.4 to 7.0 GHz	13.5 dB	_____	
		7.0 to 13.5 GHz	13 dB	_____	
		13.5 to 20.0 GHz	12 dB	_____	
		20.0 to 26.5 GHz	9 dB	_____	
		0.01 to 26.5 GHz	6 dB	_____	

Table 4-10. Performance Test Record (7 of 9)

SPECIFICATIONS TESTED Limits	Step	TEST Conditions	LOWER LIMIT	MEASURED VALUE	UPPER LIMIT
4-3. FREQUENCY STABILITY TEST (cont'd.)					
Frequency Change with 10 dB Power Level Change					
Band 0	5.	1.0 GHz	.9998 GHz	_____	1.0002 GHz
Band 1	6.	6.0 GHz	5.9998 GHz	_____	6.0002 GHz
Band 2		12.0 GHz	11.9996 GHz	_____	12.0004 GHz
Band 3		18.0 GHz	17.9994 GHz	_____	18.0006 GHz
Band 4		24.0 GHz	23.9992 GHz	_____	24.0008 GHz
Frequency Change with 3:1 Load SWR					
Band 0	10.	CW 1 GHz	.99995 GHz	_____	1.00005 GHz
Band 1	11.	CW 6 GHz	5.99995 GHz	_____	6.00005 GHz
Band 2		CW 12 GHz	11.9999 GHz	_____	12.0001 GHz
Band 3		CW 18 GHz	17.99985 GHz	_____	18.000015 GHz
Band 4		CW 24 GHz	23.9998 GHz	_____	24.0002 GHz
4-4. RESIDUAL FM TEST	4./5A.	CW 1 GHz		_____	5 kHz
	5./6A.	CW 4 GHz		_____	5 kHz
		CW 10 GHz		_____	7 kHz
		CW 15 GHz		_____	9 kHz
4-5. SPURIOUS SIGNAL TEST					
Harmonic Related	4.	0.01 to 2.4 GHz	25 dBc	_____	
	5.	2.4 to 7.0 GHz	25 dBc	_____	
		7.0 to 13.5 GHz	25 dBc	_____	
		20.0 to 26.5 GHz	20 dB	_____	
		0.01 to 26.5 GHz	20 dB	_____	
Non-Harmonics	4.	0.01 to 2.4 GHz	25 dBc	_____	
	5.	2.4 to 7.0 GHz	50 dBc	_____	
		7.0 to 13.5 GHz	50 dBc	_____	
		13.5 to 20 GHz	50 dBc	_____	
		20.0 to 26.5 GHz	50 dBc	_____	

Table 4-10. Performance Test Record (8 of 9)

SPECIFICATIONS TESTED Limits		Step	TEST Conditions			LOWER LIMIT	MEASURED VALUE	UPPER LIMIT
4-6. EXTERNAL FREQUENCY MODULATION TEST								
CW at 1 GHz		6.	DC to 100 Hz			.988 GHz	_____	1.012 GHz
		15.	100 Hz to 1 MHz			.993 GHz	_____	1.007 GHz
		16.	1 MHz to 2 MHz			.995 GHz	_____	1.005 GHz
			2 MHz to 10 MHz			.999 GHz	_____	1.001 GHz
4-7. SQUARE-WAVE ON/OFF RATIO AND SYMMETRY TEST								
CW at 4 GHz		4.	On/Off Ratio			30 dB	_____	
		5.	Symmetry			40%	_____	60%
4-8. STEP ATTENUATOR ACCURACY (Option 002)								
0.01 to 12.4 GHz		2.	CW frequency = 5.0 GHz					
Step Attenuator Setting	RF plug-in Output Power		Attenuator Error	+	Deviation from Reference			
55 dB	+10 dBm	10.	Ref		Ref			Ref
50 dB	5 dBm		_____	+	_____	−0.4 dB	_____	+0.4 dB
45 dB	0 dBm		_____	+	_____	−0.6 dB	_____	+0.6 dB
40 dB	− 5 dBm		_____	+	_____	−0.7 dB	_____	+0.7 dB
35 dB	−10 dBm		_____	+	_____	−0.7 dB	_____	+0.7 dB
30 dB	−15 dBm		_____	+	_____	−0.9 dB	_____	+0.9 dB
25 dB	−20 dBm		_____	+	_____	−0.9 dB	_____	+0.9 dB
20 dB	−25 dBm		_____	+	_____	−1.8 dB	_____	+1.8 dB
15 dB	−30 dBm		_____	+	_____	−2.0 dB	_____	+2.0 dB
10 dB	−35 dBm		_____	+	_____	−2.0 dB	_____	+2.0 dB
5 dB	−40 dBm		_____	+	_____	−2.0 dB	_____	+2.0 dB
0 dB	−45 dBm		_____	+	_____	−2.2 dB	_____	+2.2 dB

Table 4-10. Performance Test Record (9 of 9)

SPECIFICATIONS TESTED Limits		Step	TEST Conditions			LOWER LIMIT	MEASURED VALUE	UPPER LIMIT
4-8. STEP ATTENUATOR ACCURACY (Option 002) (cont'd)								
12.4 to 18.0 GHz		11.	CW frequency = 15.0 GHz					
Step Attenuator Setting	RF plug-in Output Power		Attenuator Error	+	Deviation from Reference			
55 dB	+10 dBm	10.	Ref		Ref			Ref
50 dB	5 dBm		_____	+	_____	−0.5 dB	_____	+0.5 dB
45 dB	0 dBm		_____	+	_____	−0.7 dB	_____	+0.7 dB
40 dB	− 5 dBm		_____	+	_____	−0.9 dB	_____	+0.9 dB
35 dB	−10 dBm		_____	+	_____	−0.9 dB	_____	+0.9 dB
30 dB	−15 dBm		_____	+	_____	−1.2 dB	_____	+1.2 dB
25 dB	−20 dBm		_____	+	_____	−1.2 dB	_____	+1.2 dB
20 dB	−25 dBm		_____	+	_____	−2.0 dB	_____	+2.0 dB
15 dB	−30 dBm		_____	+	_____	−2.0 dB	_____	+2.0 dB
10 dB	−35 dBm		_____	+	_____	−2.3 dB	_____	+2.3 dB
5 dB	−40 dBm		_____	+	_____	−2.3 dB	_____	+2.3 dB
0 dB	−45 dBm		_____	+	_____	−2.5 dB	_____	+2.5 dB
18.0 to 20.0 GHz			CW frequency = 19.0 GHz					
Step Attenuator Setting	RF plug-in Output Power		Attenuator Error	+	Deviation from Reference			
55 dB	+10 dBm		Ref		Ref			Ref
50 dB	5 dBm		_____	+	_____	−0.7 dB	_____	+0.7 dB
45 dB	0 dBm		_____	+	_____	−1.0 dB	_____	+1.0 dB
40 dB	− 5 dBm		_____	+	_____	−2.5 dB	_____	+2.5 dB
35 dB	−10 dBm		_____	+	_____	−2.5 dB	_____	+2.5 dB
30 dB	−15 dBm		_____	+	_____	−3.0 dB	_____	+3.0 dB
25 dB	−20 dBm		_____	+	_____	−3.0 dB	_____	+3.0 dB
20 dB	−25 dBm		_____	+	_____	−4.2 dB	_____	+4.2 dB
15 dB	−30 dBm		_____	+	_____	−4.2 dB	_____	+4.2 dB
10 dB	−35 dBm		_____	+	_____	−4.4 dB	_____	+4.4 dB
5 dB	−40 dBm		_____	+	_____	−4.4 dB	_____	+4.4 dB
0 dB	−45 dBm		_____	+	_____	−4.6 dB	_____	+4.6 dB

Table 4-11. Operation Verification Test Record (1 of 4)

HP 83595A RF PLUG-IN Tested by_____

Serial No._____ Date_____

	Specification	Pass	Fail
4-1. Frequency Range and Accuracy Test			
Frequency Range	0.01 to 20 GHz		
CW Frequency Accuracy	10.0 MHz ± 5 MHz		
	1.0 GHz ± 5 MHz		
	2.4 GHz ± 5 MHz		
	4.0 GHz ± 5 MHz		
	2.5 GHz ± 5 MHz		
	7.0 GHz ± 5 MHz		
	10 GHz ± 10 MHz		
	7.1 GHz ± 10 MHz		
	13.5 GHz ± 10 MHz		
	17.0 GHz ± 10 MHz		
	14.0 GHz ± 10 MHz		
	20.0 GHz ± 10 MHz		
	24.0GHz ± 12 MHz		
	21.0 GHz ± 12 MHz		
	26.5 GHz ± 12 MHz		
Swept Frequency Accuracy			
Full Band	10 MHz ± 50 MHz		
	26.5 GHz ± 50 MHz		
Band 0	10 MHz ± 15 MHz		
	2.4 GHz ± 15 MHz		
Band 1	2.4 GHz ± 20 MHz		
	7.0 GHz ± 20 MHz		
Band 2	7.0 GHz ± 25 MHz		
	13.5 GHz ± 25 MHz		
Band 3	13.5 GHz ± 30 MHz		
	20.0 GHz ± 30 MHz		
Band 4	20.0 GHz ± 35 MHz		
	26.5 GHz ± 35 MHz		

Table 4-11. Operation Verification Test Record (2 of 4)

HP 83595A RF PLUG-IN Tested by_____

Serial No._____ Date_____

	Specification	Pass	Fail
4-1. Frequency Range and Accuracy Test (cont'd.)			
Frequency Marker Accuracy			
(Full Band) M1 at 1 GHz	±150 MHz		
M2 at 4 GHz	± 150 MHz		
M3 at 8 GHz	± 150 MHz		
M4 at 18 GHz	± 150 MHz		
M5 at 24 GHz	± 150 MHz		
(Band 0) M1 at 1 GHz	±26 MHz		
M2 at 2 GHz	± 26 MHz		
(Band 1) M1 at 3 GHz	±43 MHz		
M2 at 6 GHz	± 43 MHz		
(Band 2) M1 at 8 GHz	±58 MHz		
M2 at 12 GHz	± 58 MHz		
(Band 3) M1 at 15 GHz	±63 MHz		
M2 at 18 GHz	± 63 MHz		
(Band 4) M1 at 21 GHz	±82.5 MHz		
M2 at 25 GHz	± 82.5 MHz		
4-2. Output Amplitude Test			
Maximum Leveled Power			
0.01 to 2.4 GHz	>+10 dBm		
2.4 to 7.0 GHz	>+10 dBm		
7.0 to 13.5 GHz	>+10 dBm		
13.5 to 20.0 GHz	>+10 dBm		
20.0 to 26.5 GHz	>+4 dBm		
0.01 to 26.5 GHz	>+4 dBm		
Output Power Variation			
0.01 to 2.4 GHz	± 0.9 dB		
2.4 to 7.0 GHz	± 0.7 dB		
7.0 to 13.5 GHz	±0.7 dB		
13.5 to 20 GHz	±0.8 dB		
20.0 to 26.5 GHz	±0.9 db		
0.01 to 26.5 GHz	±2.0 dB		

Table 4-11. Operation Verification Test Record (3 of 4)

HP 83595A RF PLUG-IN Tested by_____

Serial No._____ Date_____

	Specification	Pass	Fail
4-2. Output Amplitude Test (cont'd.)			
Power Level Accuracy			
0.01 to 2.4 GHz			
+ 10 dBm	± 1.5 dB		
+ 8 dBm	±1.5 dB		
+ 6 dBm	±1.5 dB		
+ 4 dBm	±1.5 dB		
+ 2 dBm	±1.5 dB		
− 0 dBm	±1.5 dB		
− 2 dBm	±1.5 dB		
− 4 dBm	±1.5 dB		
−5 dBm	±1.5 dB		
2.4 to 7.0 GHz			
+ 10 dBm	± 1.3 dB		
+ 8 dBm	±1.3 dB		
+ 6 dBm	±1.3 dB		
+ 4 dBm	±1.3 dB		
+2 dBm	±1.3 dB		
0 dBm	±1.3 dB		
− 2 dBm	±1.3 dB		
− 4 dBm	±1.3 dB		
− 5 dBm	±1.3 dB		
7.0 to 13.5 GHz			
+ 10 dBm	± 1.3 dB		
+ 8 dBm	±1.3 dB		
+ 6 dBm	±1.3 dB		
+ 4 dBm	±1.3 dB		
+ 2 dBm	±1.3 dB		
0 dBm	±1.3 dB		

Table 4-11. Operation Verification Test Record (4 of 4)

HP 83595A RF PLUG-IN Tested by_____

Serial No._____ Date_____

	Specification	Pass	Fail
4-2. Output Amplitude Test (cont'd.)			
− 2 dBm	±1.3 dB		
− 4 dBm	±1.3 dB		
− 5 dBm	±1.3 dB		
13.5 to 20.0 GHz			
+10 dBm	±1.4 dB		
+8 dBm	±1.4 dB		
+6 dBm	±1.4 dB		
+4 dBm	±1.4 dB		
+2 dBm	±1.4 dB		
0 dBm	±1.4 dB		
−2 dBm	±1.4 dB		
− 4 dBm	±1.4 dB		
− 5 dBm	±1.4 dB		
20.0 to 26.5 GHz			
+4 dBm	±1.7 dB		
+2 dBm	±1.7 dB		
PP0 dBm	±1.7 dB		
−2 dBm	±1.7 dB		
−4 dBm	±1.7 dB		
−5 dBm	±1.7 dB		
20.0 to 26.5 GHz			
+4 dBm	±1.8 dB		
+2 dBm	±1.8 dB		
PP0 dBm	±1.8 dB		
−2 dBm	±1.8 dB		
−4 dBm	±1.8 dB		
−5 dBm	±1.8 dB		
Power Sweep Range			
0.01 to 2.4 GHz	15 dB		
2.4 to 7.0 GHz	13.5 dB		
7.0 to 13.5 GHz	13 dB		
13.5 to 20.0 GHz	12 dB		
20.0 to 26.5 GHz	6 dB		
0.01 to 26.5 GHz	6 dB		

Section 5. Adjustments

INTRODUCTION

This section provides adjustment procedures for the HP 83595A RF plug-in. These procedures should not be performed as routine maintenance but should be used (1) after replacement of a part or component, or (2) when performance tests show that the specifications of Table 1-1 cannot be met. Table 5-1 lists all of the adjustments by reference designation, adjustment name, adjustment number, and description. Each procedure includes a test setup illustration and one or more adjustment location illustrations. Table 5-2 lists each assembly and its related adjustment.

NOTE: Allow the HP 83595A RF plug-in and the HP 8350 sweep oscillator mainframe to warm up for 30 minutes prior to making any adjustments. Use a **non-metallic** adjustment tool whenever possible.

SAFETY CONSIDERATIONS

Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings which must be followed to ensure safe operation and to retain the instrument in safe condition. Service and adjustments should be performed only by a skilled person who is aware of the hazard involved.

WARNING

Adjustments in this section are performed with power supplied to the instrument while protective covers are removed. There are voltages at points in the instrument which can, if contacted, cause personal injury. Be extremely careful. Adjustments should be performed only by a skilled person who is aware of the hazard involved. Capacitors inside the instrument may still be charged, even if the instrument has been disconnected from its source of supply.

EQUIPMENT REQUIRED

The equipment required for the adjustment procedures is listed in Section I of this manual. If the test equipment recommended is not available, other equipment may be used if its performance meets the critical specifications listed in the table. The specified equipment required for each adjustment is referenced in each procedure.

RELATED ADJUSTMENTS

Interactive adjustments are noted in the adjustment procedures. Table 5-2 indicates by adjustment number the adjustments that must be performed if an assembly has been repaired or replaced or if an adjustment has been made to an assembly.

ADJUSTMENT PROCEDURE

Adjustment procedures are given in the proper sequence to allow for interrelated adjustments.

Table 5-1. Adjustments (1 of 2)

Adjustment Number and Name	Description	Potentiometer(s) Affected
5-1. −10V Reference on A8 YO Driver	Adjusts the −10V reference power supply.	A8R44 (−10V)
5-2. Sweep Control Adjustments	Scales the HP 8350 VTUNE (tuning voltage) for use by the A7 SYTM and A8 YO driver assemblies. Also optimizes the bandswitch sequencing.	A6R16 (TV GAIN), A6R21 (DAC CAL), A6R24 (B3), A6R26 (B2), A6R28 (B1), A6R30 (B0), A6R34 (−10V Offset) A6R37 (SP)
5-3. YO and YTM DAC Calibration	Calibrates the voltage tune and offset DACs on the A8 YO driver and A7 SYTM assemblies. Optimizes the delay compensation circuits.	A7R18 (Z), A7R19 (GAIN), A7R22 (ZRO), A7R24 (OFS), A8R19 (GAIN), A8R22 (ZRO), A8R24 (OFS)
5-4. Frequency Accuracy	Matches the displayed frequency to the RF plug-in output frequency by programming in a correction factor.	A8S1 (OFFSET) A8S2 (GAIN)
5-5. YO Retrace Compensation	Fine tunes the retrace compensation circuit to maximize the YO frequency setting time during bandswitch.	A8R55 (RTC COMP)
5-6. YO Delay Compensation	Optimizes delay compensation circuit for fast sweep speeds.	A8R10 (HI), A8R12 (LO), A8R18 (Z)
5-7. Slow Sweep SYTM to YO Tracking	Optimizes the output power by tracking the passband or the SYTM with the output of the YIG oscillator.	A6R73 (2L), A6R68 (2H), A6R74 (3L), A6R69 (3H) A6R78 (T) A7R51 (B1 OFS), A7S1 (OFFSET), A7S2 (GAIN)
5-8. SRD BIAS	Sets the SRD bias for the SYTM to obtain maximum output power.	A6R12 (C), A6R63 (3HL), A6R68 (2H), A6R69 (3H), A6R70 (4H) A6R73 (2L), A6R74 (3L), A6R75 (4L) A6R78 (T)
5-9. YTM Delay Compensation	The YTM delay compensation circuit is adjusted to optimize the YTM to YO tracking over varying sweep rates.	A7R10 (SGL HI), A7R12 (SGL LO), A7R42 (SEQ HI), A7R43 (SEQ LO), A7R45 (SEQ TC), A7R46 (SGL TC), A7R55 (RTC COMP)

Table 5-1. Adjustments (2 of 2)

Adjustment Number and Name	Description	Potentiometer(s) Affected
5-10. Band Overlap	The gain of the variable gain amplifier (A6) is adjusted for a smooth frequency transition between bands.	A6R24 (B3), A6R26 (B2), A6R28 (B1)
5-11. Frequency Reference 1V/GHz Output	The frequency reference rear panel output is adjusted for a 1V/GHz output.	A2R1 (GAIN), A2R4 (OFFSET), A2R6 (BAND 0 OFFSET), A2R23 (BAND 0 GAIN)
5-12. ALC Adjustment	Compensates for DC offsets in the detected RF path and the main ALC amplifier.	A4C23, A4R1 (SLP), A4R7 (0 HI), A4R8 (1 HI), A4R9 (0 MD), A4R10 (1 MD), A4R12 (1 LO), A4R13 (0 LO), A4R14 (BIAS), A4R15 (GAIN), A4R78, A4R81, A4R82
5-13. Power Calibration	Calibrates power at three points over the leveled power range.	A4R1 (SLP), A4R7 (0 HI), A4R8 (1 HI), A4R9 (0 MD), A4R10 (1 MD), A4R12 (1 LO), A4R13 (0 LO)
5-14. ALC Internal Leveled Flatness	Optimizes ALC flatness.	A5R34 (BP1), A5R36 (BP2), A5R38 (BP3), A5R40 (BP4), A5R41 (SL1), A5R42 (SL2), A5R43 (SL3), A5R44 (SL4), A5R48 (SLP)
5-15. Squarewave Symmetry Adjustment	Minimizes squarewave overshoot and adjusts the duty cycle.	A4C23 (SYM 1), A4R92, A4R99 (SYM 2)
5-16. ALC Gain Adjustment	Maximizes ALC loop gain without producing oscillations.	A4R15 (GAIN)
5-17. Power Sweep	Output of the power sweep circuit is adjusted for correct sweep.	A5R50 (PWSP)
5-18. FM Driver	The FM driver high frequency offset is adjusted for a zero volt drive with no FM applied.	A5C14 (LO), A5R19 (FM OFFSET), A5R31*, A5R75 (HI)

* Selected Value Resistor

Table 5-2. Related Adjustments

Assembly Changed or Repaired	Related Assemblies (in order of Adjustments)	Perform the Following Paragraph Numbers
A1/A2 Front Panel	A2	5-11
A3 Digital Interface	A3	(Refer to Table 3-3 in Operation Section)
A4 ALC	A4, A5	5-12 thru 5-16
A5 FM	A4, A5	5-12 thru 5-18
A6 Sweep Control	A6, A8, A7	5-2 thru 5-10
A7 YTM Driver	A6, A8, A7	5-2 thru 5-10
A8 YO Driver	A6, A8, A7	5-2 thru 5-10
A11 Cavity Oscillator	A4, A5	5-12 thru 5-16
A12 Switched YIG Tuned Multiplier	A6, A8, A7, A2	5-2 thru 5-11
A13 2.2 to 7.0 GHz Oscillator	A6, A8, A7, A2, A5	5-2 thru 5-7, 5-10, 5-11, and 5-18
A14 Power Amplifier	A4, A5	5-12 thru 5-16
A15 DC Return	A4, A5	5-12 thru 5-16
A16 Modulator/Splitter	A4, A5	5-12 thru 5-16
A17 0.01 to 2.4 GHz Amplifier	A4, A5	5-12 thru 5-16
A18 Modulator/Mixer	A4, A5	5-12 thru 5-16
AT1 Isolator	A4, A5	5-12 thru 5-16
DC1 Directional Detector	A4, A5	5-12 thru 5-16
DC2 Directional Coupler	A4, A5	5-12 thru 5-16

5-1. −10 Volt Reference on A8 YO Driver

DESCRIPTION

The −10 volt reference voltage source on the A8 YO driver board is used as a reference voltage for the DACs on the A4 ALC, A6 sweep control, A7 YTM driver, and A8 YO driver boards. The −10 volt reference output voltage is set by the A8R44 −10V adjustment while monitoring A8TP12.

EQUIPMENT

Digital Voltmeter	HP 3456A
Sweep Oscillator Mainframe	HP 8350

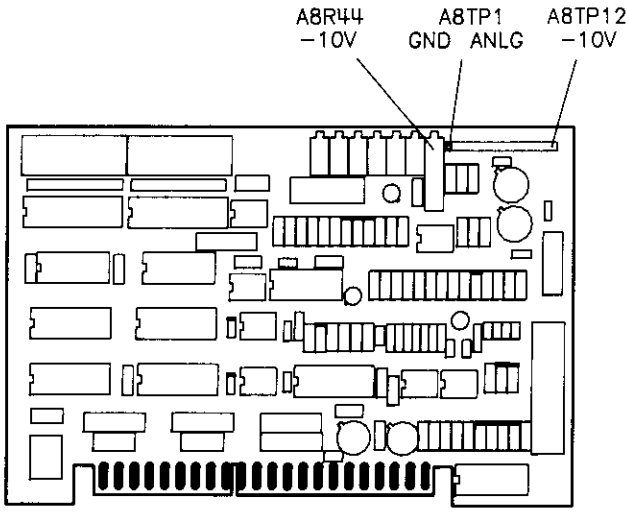


Figure 5-1. −10V Reference Adjustment Location

PROCEDURE

1. Connect the DVM HI to A8TP12 (−10V) with DVM LO to A8TP1 (GND ANLG).
2. Adjust A8R44 (−10V) for a DVM reading of −10 ± 0.001 VDC. Refer to Figure 5-1 for −10 volt reference adjustment location.

5-2. Sweep Control Adjustments

DESCRIPTION

With the tuning voltage (VTUNE) set to +10V (CW frequency of 26.5 GHz), the tuning voltage buffer is set for unity gain, and the DAC CAL adjustment is set to equalize the bandswitch comparator DAC and tuning voltage buffer inputs to the variable gain amplifier (DAC CAL is set for 0V at A6TP4). The −10V OFFSET adjustment is then set to offset the variable gain amplifier output by −10V. The gain of the variable gain amplifier is then calibrated at the low end of each frequency band. The HP 83595A is then swept across its full frequency range and SP is adjusted to set the bandswitch points.

EQUIPMENT

Digital Voltmeter	HP 3456A
Oscilloscope	HP 1741A
1:1 Probe	HP 10008B
Sweep Oscillator Mainframe	HP 8350

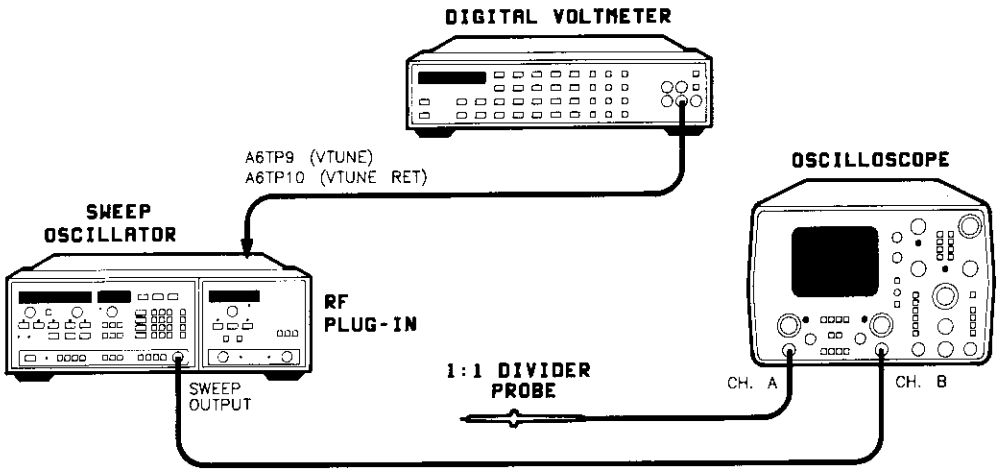


Figure 5-2. Sweep Control Adjustments Test Setup

5-2. Sweep Control Adjustments (Cont'd)

PROCEDURE

1. Ensure that A3S1 switch position 1 is in the OPEN (up) position. Refer to Table 3-3 in the Operation Section of this manual for configuration information.

2. Set up the equipment as shown in Figure 5-2 with the DVM HI connected to A6TP9 (V TUNE) and DVM LO connected to A6TP10 (V TUNE RET). See Figure 5-3 for test point location. Do not connect the oscilloscope probe yet. Allow the instrument to warm up for 1 hour.

3. On the sweep oscillator/RF plug-in:

   Press **[INSTR PRESET]**

   Press **[CW] [2] [6] [.] [5] [GHz]**

   Adjust the sweep oscillator FREQ VERNIER for a DVM reading of 10 ±0.001 VDC.

NOTE: The following voltage measurement procedures on the A6 sweep control board are made with DVM LO connected to A8TP1 (which is electrically the same as motherboard ground).

4. Connect DVM HI to A6TP5 and adjust A6R16 (TV GAIN) for a DVM reading of −10 ±0.001 VDC. Refer to Figure 5-3 for sweep control adjustment locations.

5. Connect DVM HI to A6TP4 and adjust A6R21 (DAC CAL) for a DVM reading of 0 ±0.001 VDC.

6. Connect DVM HI to A6TP8 (BV TUNE) and adjust A6R34 for a DVM reading of −10 ±0.001 VDC.

7. On the sweep oscillator/RF plug-in:

   Press **[CW] [2] [0] [GHz]**

8. Connect DVM HI to A6TP5 and adjust the sweep oscillator FREQ VERNIER control for a DVM reading of −7.54624 ±0.00005 VDC.

9. Connect DVM HI to A6TP8 and adjust A6R24 (B3) for a DVM reading of 0 ±0.001 VDC.

5-2. Sweep Control Adjustments (Cont'd)

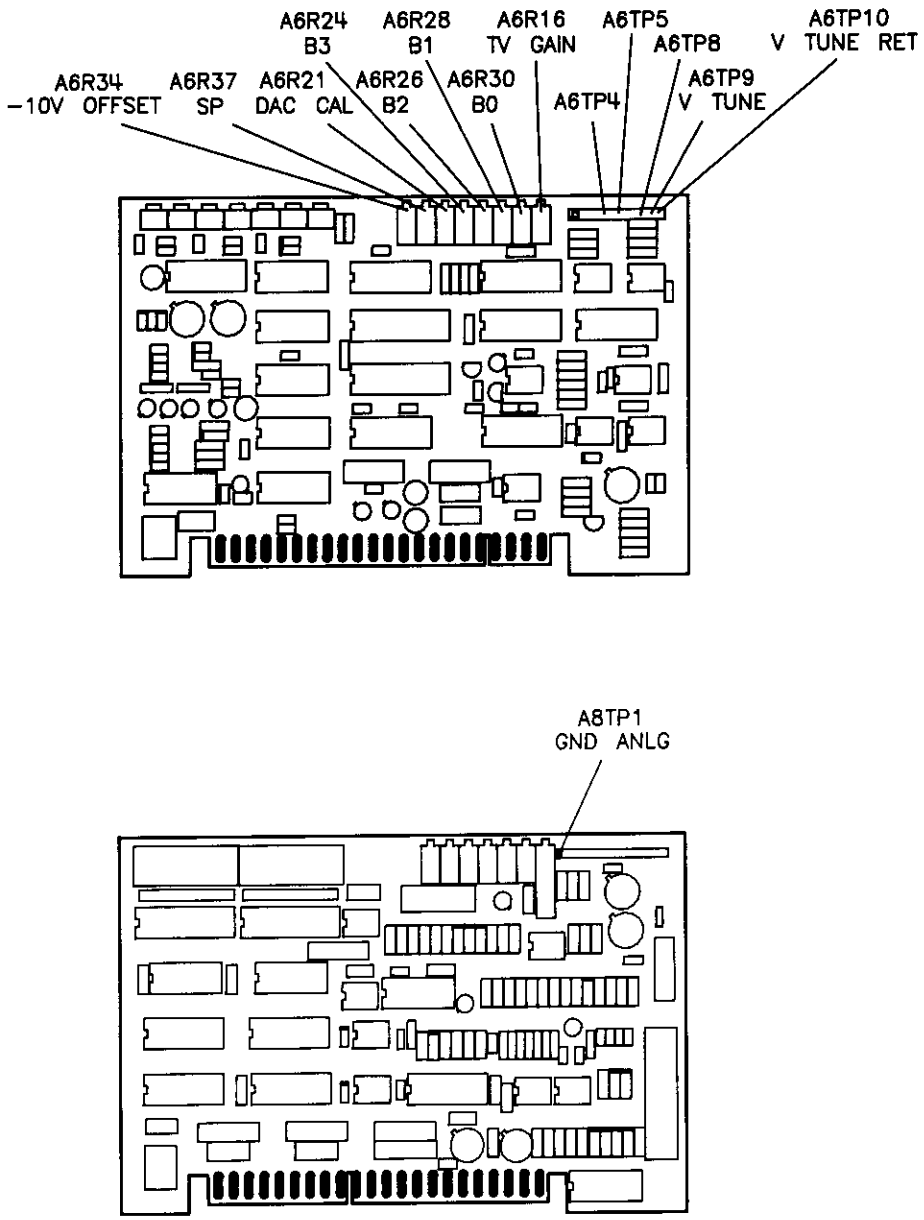


Figure 5-3. Sweep Control Adjustment Locations

5-2. Sweep Control Adjustments (Cont'd)

10. On the sweep oscillator/RF plug-in:

    Press **[CW] [1] [3] [.] [5] [GHz]**

11. Connect DVM HI to A6TP5 and adjust the sweep oscillator FREQ VERNIER control for a DVM reading of −5.09249 ±0.00005 VDC.

12. Connect DVM HI to A6TP8 and adjust A6R24 (B3) for a DVM reading of 0 ± 0.001 VDC.

13. Repeat steps 7 through 12 until the voltage at A6TP8 is optimized at 20 GHz and at 13.5 GHz. (A6R24 is the adjustment for bands 3 and 4.)

14. On the sweep oscillator/RF plug-in

    Press **[CW] [7] [GHz]**

15. Connect DVM HI to A6TP5 and adjust the sweep oscillator FREQ VERNIER control for a DVM reading of −2.63873 ±0.00005 VDC.

16. Connect DVM HI to A6TP8 and adjust A6R26 (B2) for a DVM reading of 0 ±0.001 VDC.

17. On the sweep oscillator/RF plug-in:

    Press **[CW] [2] [.] [4] [MHz]**

18. Connect DVM HI to A6TP5 and adjust the sweep oscillator FREQ VERNIER control for a DVM reading of −0.90223 ±0.00005 VDC.

19. Connect DVM HI to A6TP8 and adjust A6R28 (B1) for a DVM reading of 0 ±0.001 VDC.

20. On the sweep oscillator/RF plug-in:

    Press **[CW] [1] [0] [MHz]**

21. Connect DVM HI to A6TP5 and adjust the sweep oscillator FREQ VERNIER control for a DVM reading of 0 ±0.00005 VDC.

22. Connect DVM HI to A6TP8 and adjust A6R30 (B0) for a DVM reading of 0 ±0.001 VDC.

23. On the sweep oscillator/RF plug-in:

    Press **[INSTR PRESET]**

24. Set the oscilloscope settings as follows:

    Select A vs. B mode
    Set CHAN A for 0.5V/DIV, DC coupled

    Connect the oscilloscope probe to A6TP8.

25. Adjust the oscilloscope vertical position control to set the top of the first full 0 to −10 volt sweep ramp on the centerline as shown in Figure 5-4.

5-2. Sweep Control Adjustments (Cont'd)

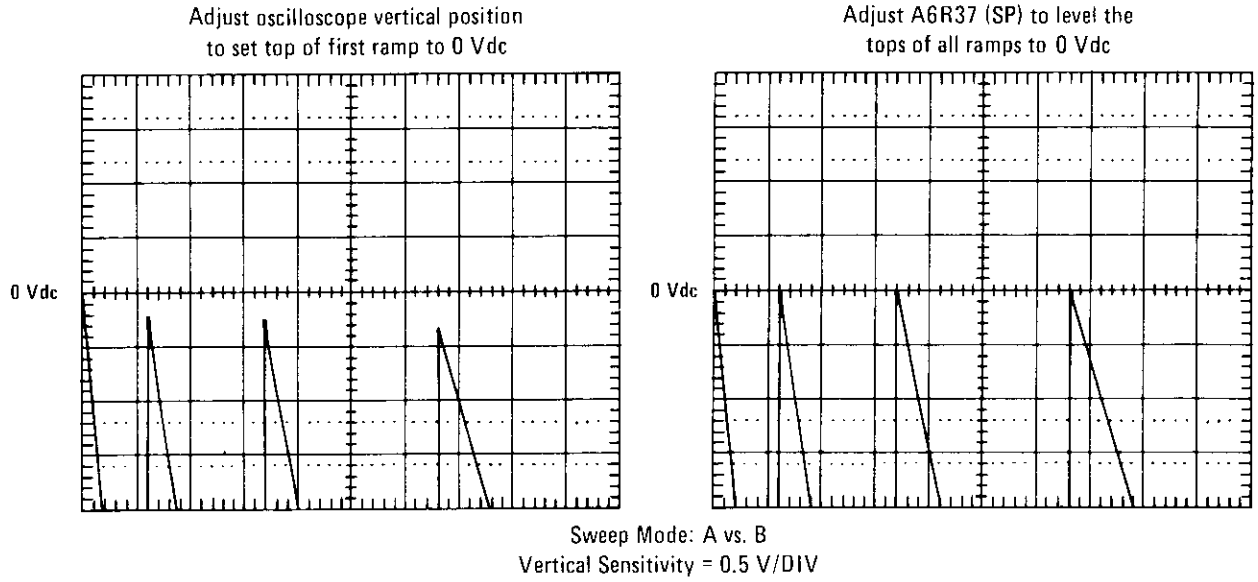


Figure 5-4. Sweep Control Adjustment Waveforms

26. Adjust A6R37 (SP) to bring the tops of the remaining 0 to −10 volt sweep ramps to the center graticule as shown in Figure 5-4.

27. If A3S1 switch position 1 was modified in step 1 of this procedure, reset it to the closed (down) position. Refer to Table 3-3 in the Operation Section of this manual for switch configuration information.

5-3. YO and SYTM DAC Calibration

DESCRIPTION

The HP 8350 is set for a CW frequency of 26.5 GHz and then fine tuned for a tuning voltage (VTUNE) of +10V. The hex data write feature of the HP 8350 is used to load each DAC with either all ones or all zeros. With both the scaled voltage tune and offset DACs loaded with all zeros, the YO collector output on the A8 assembly is monitored and the +20V tracking amplifier ZRO adjustment is set. Each DAC is then loaded with all ones and the respective offset or gain adjustment is set. The A7 SYTM driver is adjusted the same way. Finally the HP 8350 is then set into the swept CW mode, and the delay compensation circuits on both A7 and A8 are adjusted for a 0V output.

EQUIPMENT

Digital Voltmeter ..... HP 3456A
Sweep Oscillator Mainframe ..... HP 8350

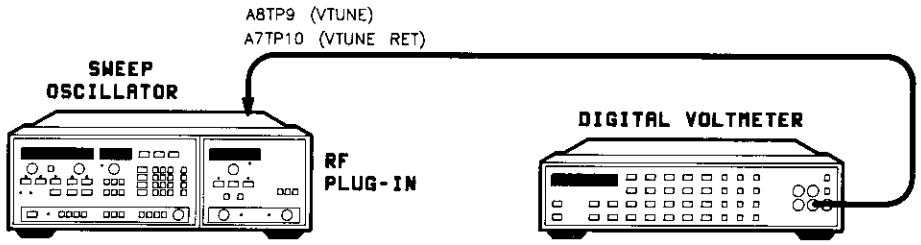


Figure 5-5. YO and YTM DAC Calibration Test Setup

PROCEDURE

1. Connect the equipment as shown in Figure 5-5 with DVM HI connected to A6TP9 (VTUNE) and DVM LO connected to A6TP10 (VTUNE RET). Refer to Figure 5-6 for test point and adjustment locations. Allow the RF plug-in to warm up for 1 hour.
2. On the sweep oscillator/RF plug-in:

   Press **[INSTR PRESET]**

   Press **[CW] [2] [6] [.] [5] [GHz]**

5-3. YO and SYTM DAC Calibration (Cont'd)

3. Set the sweep oscillator FREQ VERNIER for a DVM reading of 10 ±0.001 VDC.
4. Connect the DVM HI to A8TP6 (YO COLLECTOR) with DVM LO connected to A7TP8 (+20V FREQ REF).

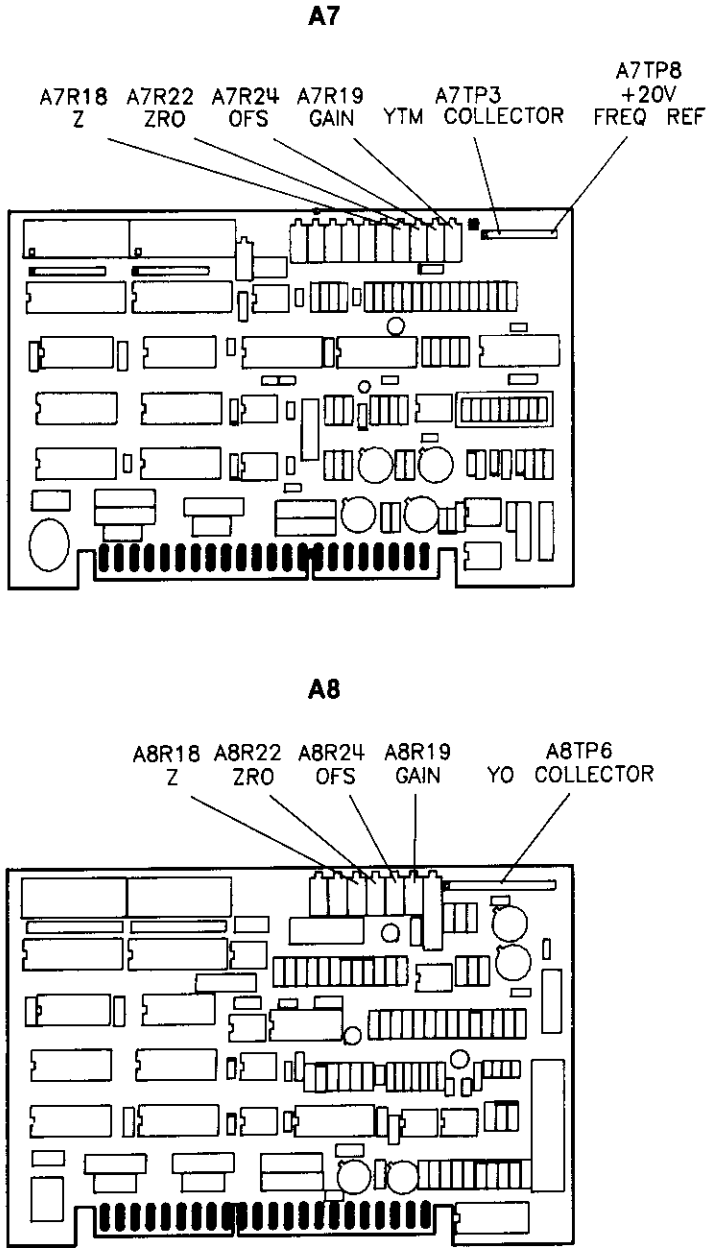


Figure 5-6. YO and SYTM DAC Calibration Adjustment Locations

5-3. YO and SYTM DAC Calibration (Cont'd)

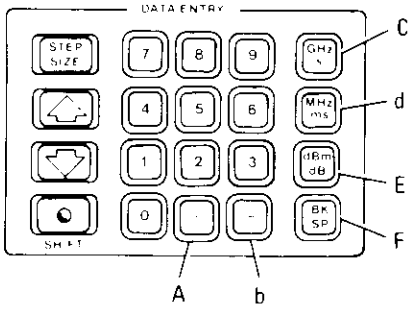


Figure 5-7. Front Panel Hexadecimal Entry Keys

5. Use the hex data write feature to write all zeros to both DACs on the A8 YO driver:

   [SHIFT] [0] [0] Enters hex data command
   [2] [GHz] [8] [0] Address location 2C80
   [M2] Hex data write
   [0] [0] Enters hex data 00
   [▲] [0] [0] Increment address to 2C81 and write 00
   [▲] [0] [0] Increment address to 2C82 and write 00
   [▲] [0] [0] Increment address to 2C83 and write 00

6. Adjust A8R22 (ZRO) for a DVM reading of −7.000 ±0.001 VDC.

7. Use the hex data write feature to write zeros to the scaled voltage tune DAC and ones to the offset DAC as follows:

   [▼] [▼] [▼] Decrement address to 2C80
   [0] [BKSP) Enters hex data 0F
   [▲] [0] [F] Increment address to 2C81 and write 0F
   [▲] [0] [F] Increment address to 2C82 and write 0F
   [▲] [0] [F] Increment address to 2C83 and write 0F

8. Adjust A8R24 (OFS) for a DVM reading of −20.000 ±0.001 VDC.

9. Use the hex data write feature to write ones to the scaled voltage tune DAC and zeros to the offset DAC as follows:

   [▼] [▼] [▼] Decrement address to 2C80
   [F] [0] Enters hex data F0
   [▲] [F] [0] Increment address to 2C81 and write F0
   [▲] [F] [0] Increment address to 2C82 and write F0
   [▲] [F] [0] Increment address to 2C83 and write F0

5-3. YO and YTM DAC Calibration (Cont'd)

10. Adjust A8R19 (GAIN) for a DVM reading of −26.500 ±0.001 VDC.

11. Use the hex data write feature to write all zeros to both DACs on the A7 YTM driver as follows:

    [▲] [▲] [▲] [▲] [▲] Increment address to 2C88
    [0] [0] Enters hex data 00
    [▲] [0] [0] Increment address to 2C89 and write 00
    [▲] [0] [0] Increment address to 2C8A and write 00
    [▲] [0] [0] Increment address to 2C8B and write 00

12. Connect DVM HI to A7TP3 (YTM COLLECTOR) with DVM LO still at A7TP8 (+20V FREQ REF). Adjust A7R22 (ZRO) for a DVM reading of −3.000 ± 0.001 VDC.

13. Use the hex data write feature to write zeros to the scaled voltage tune DAC and ones to the offset DAC as follows:

    [▼] [▼] [▼] Decrement address to 2C88
    [0] [BKSP] Enters hex data 0F
    [▲] [0] [F] Increment address to 2C89 and write 0F
    [▲] [0] [F] Increment address to 2C8A and write 0F
    [▲] [0] [F] Increment Address to 2C8B and write 0F

14. Adjust A7R24 (OFS) for a DVM reading of −19.500 ± 0.001 VDC.

15. Use the hex data write feature to write ones to the scaled voltage tune DAC and zeros to the offset DAC as follows:

    [▼] [▼] [▼] Decrement address to 2C88
    [BKSP] [0] Enter hex data F0
    [▲] [F] [0] Increment address to 2C89 and write F0
    [▲] [F] [0] Increment address to 2C8A and write F0
    [▲] [F] [0] Increment address to 2C8B and write F0

16. Adjust A7R19 (GAIN) for a DVM reading of −9.500 ± 0.001 VDC.

17. On the sweep oscillator/RF plug-in:

    Press **[INSTR PRESET] [SHIFT] [CW]**

18. Connect DVM HI to A7TP4 with reference to A8TP1 (GND ANLG).

19. Adjust A7R18 (Z) for a DVM reading of 0.000 ± 0.001 VDC.

20. Connect DVM HI to A8TP9 with reference to A8TP1 (GND ANLG).

21. Adjust A8R18 (Z) for a DVM reading of 0.000 ± 0.001 VDC.

5-4. Frequency Accuracy

DESCRIPTION

The HP 83595A CW frequency is set first to the low end and then to the high end of band 2. When the output frequency matches the front panel frequency display, the calibration switches on A8 are set for the appropriate correction factor. A8S1 affects the lower portion of the band and A8S2 affects the high section of the band.

EQUIPMENT

Frequency Counter ..... HP 5343A
10 dB Attenuator ..... HP 8491B Option 010
Sweep Oscillator Mainframe ..... HP 8350

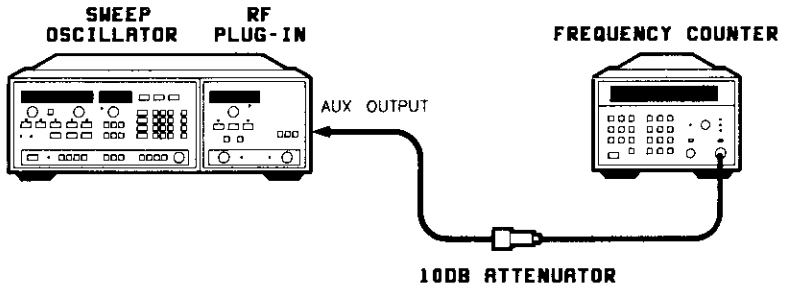


Figure 5-8. Preliminary Frequency Accuracy Test Setup

PROCEDURE

1. Connect the equipment as shown in Figure 5-8 with the frequency counter connected to the HP 83595A rear panel AUX OUTPUT connector through the 10 dB attenuator. Allow the equipment to warm up for 1 hour.
2. Adjust the HP 83595A FREQ CAL control to the center of its mechanical range.
3. On the sweep oscillator/RF plug-in:

   Press **[INSTR PRESET] [CW] [6] [.] [9] [GHz] [SAVEn] [1]**

   Press **[CW] [1] [3] [.] [5] [GHz] [SAVEn] [2]**

5-4. Preliminary Frequency Accuracy (Cont'd)

4. On the frequency counter:

   Press **[SET] [.] [2] [ENTER]**

   This sets the frequency counter in a mode which displays twice the input frequency. This step is necessary to compensate for the frequency of the rear panel AUX OUTPUT which is the YO fundamental frequency, approximately half of the sweep oscillator output frequency in band 2.

Low End Frequency Calibration

5. On the sweep oscillator/RF plug-in:

   Press **[RECALLn] [1]**

   The sweep oscillator FREQUENCY display should show 6.900 GHz.

6. Press **[SHIFT] [9] [0]** to select the low end frequency calibration mode.

7. Adjust the RF plug-in POWER control, if necessary, to display 6.900 ± 0.003 GHz on the frequency counter.

8. Set switch A8S1 for the hexadecimal value displayed in the HP 83595A POWER display (See Table 8-4 in the service section). Refer to Figure 5-9 for the location of the frequency calibration switches. Refer to Figure 5-10 for an illustration of the calibration switch configuration.

9. On the sweep oscillator/RF plug-in:

   Press **[INSTR PRESET] [RECALLn] [1]**. Verify that the frequency counter reads 6.900 ± 0.010 GHz.

High End Frequency Calibration

10. On the sweep oscillator/RF plug-in:

    Press **[RECALLn] [2]**. The sweep oscillator FREQUENCY display should show 13.500 GHz.

    Press **[SHIFT] [9] [1]** to select the high end frequency calibration mode.

11. Adjust the RF plug-in control if necessary to display 13.500 ± 0.003 GHz on the frequency counter.

12. Set switch A8S2 for the value displayed in the RF plug-in POWER display in the same manner as that described in step 8.

13. On the sweep oscillator/RF plug-in:

    Press **[INSTR PRESET] [RECALLn] [2]**. Verify that the frequency counter reads 13.500 ± 0.010 GHz.

    Press **[RECALLn 1]**

14. Manually adjust the sweep oscillator FREQUENCY control across band 2 (6.9 to 13.5 GHz) and check for frequency counter readings to ensure that they correspond to the displayed sweep oscillator FREQUENCY display reading within ± 5 MHz. If necessary repeat steps 5 through 13.

5-4. Preliminary Frequency Accuracy (Cont'd)

15. On the frequency counter:

    Press **[SET] [.] [4] [ENTER]**

16. On sweep oscillator/RF plug-in:

    Press **[2] [6] [.] [5] [GHz]**

17. Verify that the frequency counter indicates 26.5 GHz. If necessary, repeat steps 5 through 16.

18. On the sweep oscillator/RF plug-in:

    Press **[INSTR PRESET]**

    Press **[CW] [5] [0] [MHz]**

    While observing the frequency counter display, adjust the FREQ CAL control for 50 MHz.

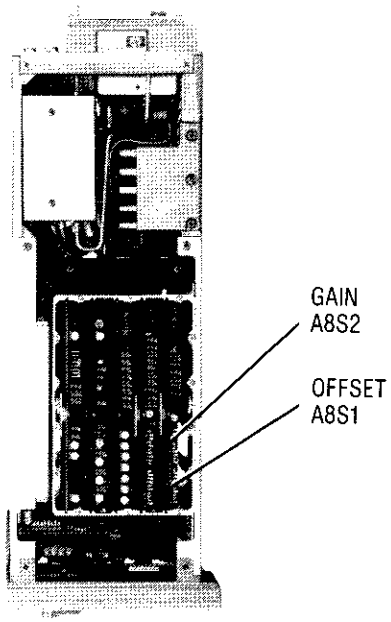


Figure 5-9. Frequency Calibration Switch Location

5-4. Preliminary Frequency Accuracy (Cont'd)

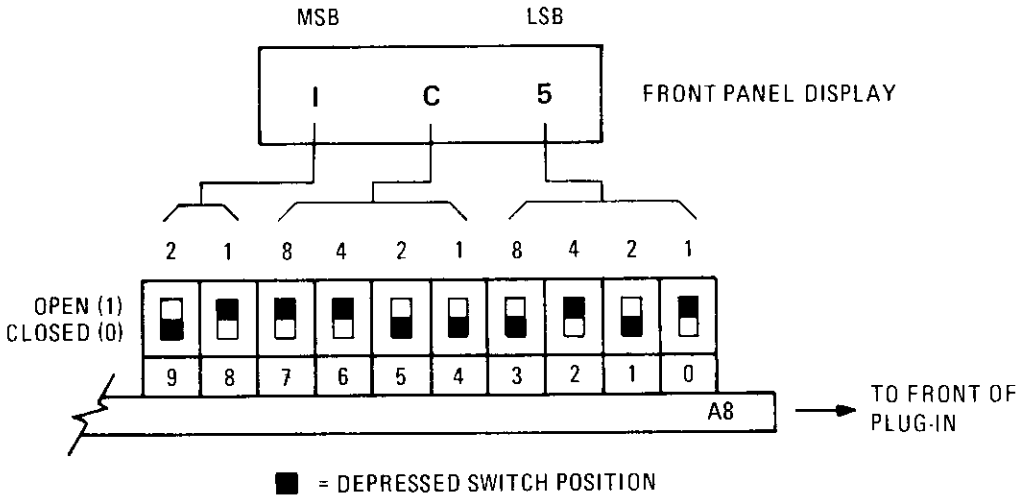


Figure 5-10. A8S1 and A8S2 Frequency Calibration Switch Configuration

5-5. YO Retrace Compensation

DESCRIPTION

During sweep retrace and each bandswitch, the YO frequency is forced to the start frequency of the next band by the retrace compensation circuit. This circuit is adjusted to maximize the YO frequency settling time before sweeping the next band. A spectrum analyzer is set to the YO frequency for the start of the next band. The width of the spectrum analyzer pip corresponds to how long the YO has settled at the correct start frequency.

EQUIPMENT

Sweep Oscillator Mainframe	HP 8350
Spectrum Analyzer	HP 8566B
Oscilloscope	HP 1741A

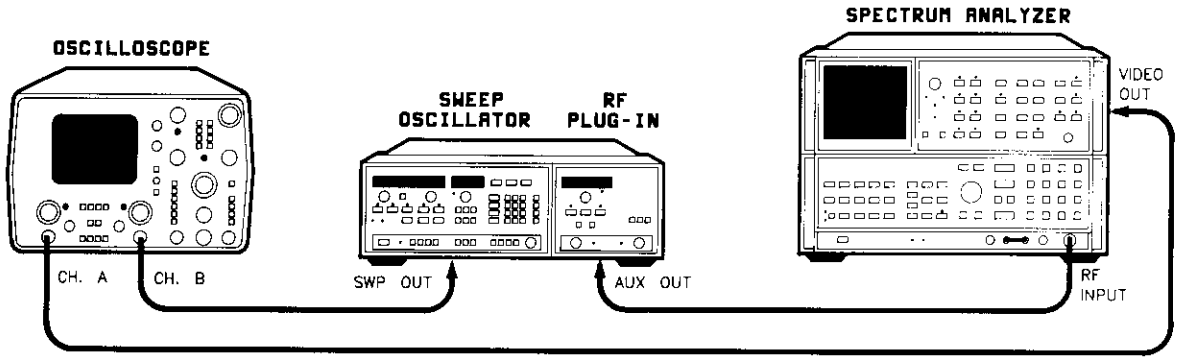


Figure 5-11. YO Retrace Compensation Test Setup

PROCEDURE

NOTE: This procedure requires that A3S1 is set to the factory-set position. Refer to Table 3-3 in the Operation Section of this manual for switch configuration information.

1. Connect the equipment as shown in Figure 5-11.

5-5. YO Retrace Compensation (Cont'd)

2. On the sweep oscillator/RF plug-in:

   Press **[INSTR PRESET]**

   Press **[RF BLANK]** to on.

   Allow the equipment to warm up for 1 hour.

3. Set the oscilloscope controls as follows:

   Set channel B to 2V/DIV, DC coupled
   Set horiz. sweep for 5 msec/DIV.
   Set delayed sweep for 0.5 msec/DIV.
   Set display to CHOP
   Set trigger to B
   Set sweep mode to MAIN

4. Adjust the vertical sensitivity of Channel A on the oscilloscope to bring the trace to center screen.

5. Adjust the spectrum analyzer center frequency to 3.5 GHz.

6. Use the delayed sweep vernier to set the delayed part of the trace on the bandswitch point between bands 1 and 2 as shown in Figure 5-12.

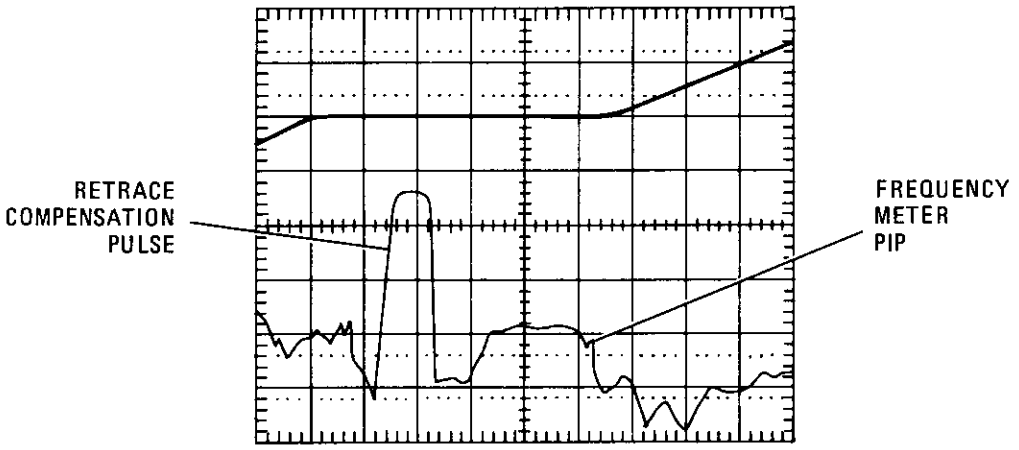


Figure 5-12. YO Retrace Compensation Pulse

7. Set the oscilloscope for delayed sweep. Adjust the spectrum analyzer center frequency to set the frequency pip near center screen.

8. Start with A8R55 (RTC COMP) fully clockwise and adjust it for the widest and flattest pip while moving the spectrum analyzer center frequency to track the bandswitch frequency. A well adjusted retrace compensation pulse is shown in Figure 5-12.

5-5. YO Retrace Compensation (Cont'd)

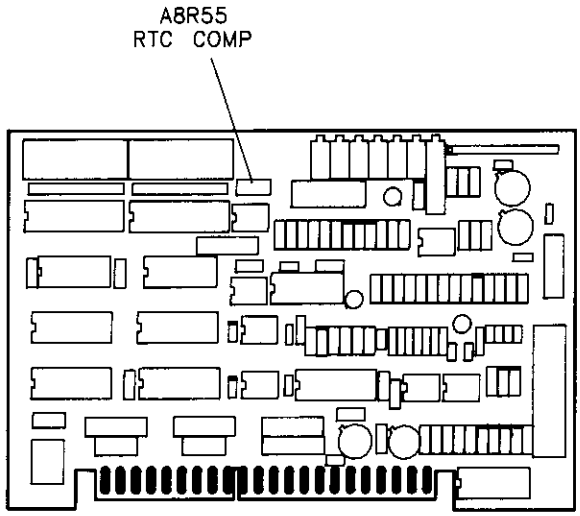


Figure 5-13. YO Retrace Compensation Adjustment Location

9. Select main sweep on the oscilloscope and adjust the delayed sweep vernier to move the delayed portion of the sweep to the bandswitch point between bands 2 and 3.

10. Adjust the spectrum analyzer center frequency to 4.49 GHz.

11. On the oscilloscope, go to delayed sweep and adjust the spectrum analyzer center frequency to set the frequency pip near center screen. If the previous band 1 to band 2 adjustment was made properly, this bandswitch point will look the same. If it does not, repeat steps 4 through 10 for the best compromise.

5-6. YO Delay Compensation

DESCRIPTION

This circuit compensates for the delay in the RF sweep output that occurs at fast sweep speeds. A spectrum analyzer is used to generate a frequency-dependent marker (pip) which is aligned with a tuning ramp-dependent marker (pip) generated from the HP 8350 sweep oscillator mainframe. Sweep time is decreased and delay in the YO is observed as the difference between the two marker pips.

Delay compensation adjustments are made while observing the shift between marker pips at a sweep time of 10 milliseconds (worst case for single-band sweeps). At sweep times greater than 100 msec, delay should not exceed +15 MHz (the difference betwen CW and swept frequency accuracies).

EQUIPMENT

Sweep Oscillator Mainframe	HP 8350
Digital Voltmeter	HP 3456A
Oscilloscope	HP 1741A
Spectrum Analyzer	HP 8566B

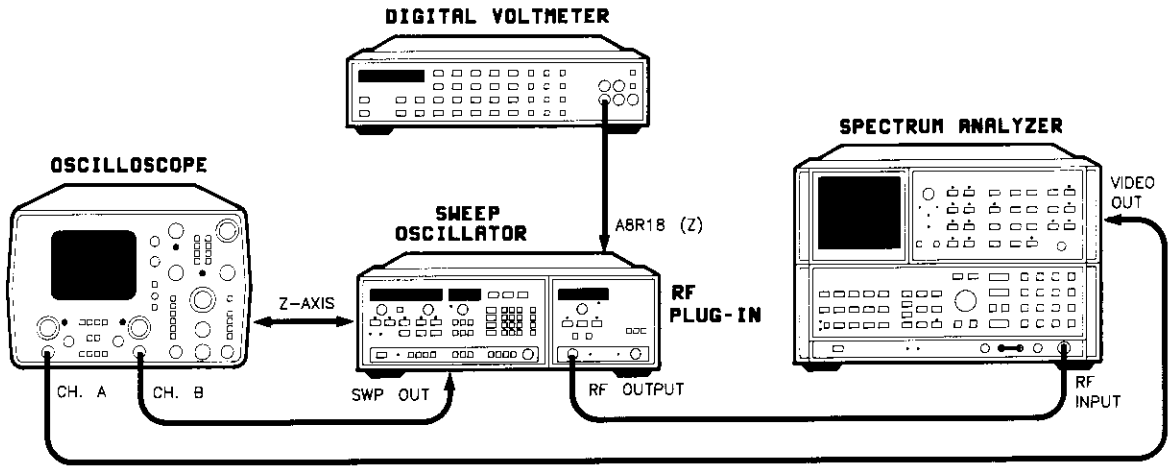


Figure 5-14. YO Delay Compensation Test Setup

PROCEDURE

NOTE: This procedure requires that A3S1 is set to the factory-set position. Refer to Table 3-3 in the Operation Section of this manual for switch configuration information.

1. Connect the equipment as shown is Figure 5-14. Allow the equipment to warm up for 1 hour.

5-6. YO Delay Compensation (Cont'd)

2. On the sweep oscillator/RF plug-in:

   Press **[CW]**

3. Measure and note the voltage at A8TP9.

4. On the sweep oscillator/RF plug-in:

   Press **[CF] [ΔF] [0] [MHz]**

5. Adjust A8R18 (Z) for a DVM reading equal to the voltage noted in step 3. Remove the DVM test leads.

6. On the sweep oscillator/RF plug-in:

   Press **[INSTR PRESET]**

   Press **[START FREQ] [6] [.] [9] [GHz]**

   Press **[STOP FREQ] [1] [3] [.] [5] [GHz]**

   Press **[SWEEP TIME] [1] [0] [ms]**

   Press **[SAVEn] [2]**

   Press **[SWEEP TIME] [2] [0] [0] [ms]**

   Press **[SAVEn] [1]**

7. On the spectrum analyzer:

   Press **[INSTR PRESET]**

   Press **[CENTER FREQUENCY] [7] [.] [2] [GHz]**

   Press **[FREQUENCY SPAN] [0] [Hz]**

   Press **[SINGLE]** sweep

8. Set the oscilloscope as follows:

   Select A vs. B mode

   Set channel A to 0.5V/DIV

   Set channel B to 0.1V/DIV

9. On the oscilloscope, position the pip to center screen with the horizontal position control. Press oscilloscope MAG X 10. Reposition the beginning of the pip at center line of screen with the horizontal position control.

10. On the sweep oscillator/RF plug-in:

    Press **[RECALL] [2]**

11. Adjust A8R12 (LO) to set the peak of the signal at the center of the oscilloscope screen.

5-6. YO Delay Compensation (Cont'd)

12. On the sweep oscillator/RF plug-in:

    Press **[RECALLn] [1]**

13. On the spectrum analyzer:

    Press **[CENTER FREQUENCY] [1] [3] [.] [2] [GHz]**

14. Set the oscilloscope channel B switch to 2V/DIV.

15. Adjust the horizontal position control so the beginning of the pip is at the center line of the screen.

16. On the spectrum analyzer:

    Press **[CENTER FREQUENCY]**

    Adjust the frequency using the rotary knob so that the peak of the pip is at the center line of the oscilloscope screen

17. On the sweep oscillator/RF plug-in:

    Press **[RECALLn] [2]**

18. Adjust A8R10 (HI) to set the peak of the pip at the center line of the oscilloscope screen.

19. On the sweep oscillator/RF plug-in:

    Press **[RECALLn] [1]**

    Repeat steps 9 through 18 until no further adjustment of A8R10 (HI) and A8R12 (LO) is necessary.

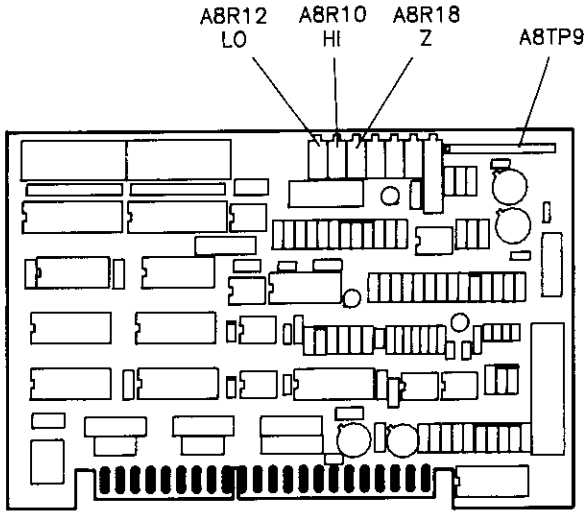


Figure 5-15. YO Delay Compensation Adjustment Location

5-7. Slow Sweep SYTM to YO Tracking

DESCRIPTION

To obtain optimum output power, the switched yig tuned multiplier (SYTM) passband should track the output of the yig oscillator (YO). The RF plug-in is set to sweep bands 2 and 3 (7 to 26.5 GHz), and the automatic leveling control (ALC) loop is opened by selecting the External (EXT) ALC MODE. The step recovery diode (SRD) bias for the SYTM is preset and will be fine tuned in the following procedure. The output power is peaked for each calibration mode, and the appropriate calibration constant is entered into the calibration switches. A7S1 stores the OFFSET constant, and A7S2 stores the GAIN constant.

EQUIPMENT

Scalar Network Analyzer	HP 8757A
Detector	HP 85025B
10 dB Attenuator	HP 8493C Option 010
Sweep Oscillator Mainframe	HP 8350
Adapter 3.5 (f) to 3.5 (f)	HP Part No. 1250-1749

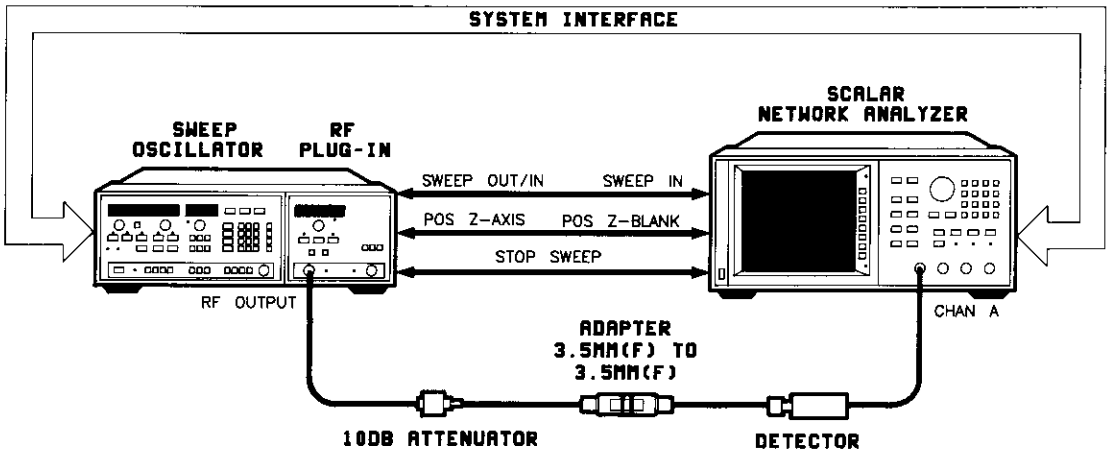


Figure 5-16. Slow Sweep SYTM to YO Tracking Test Setup

5-7. Slow Sweep SYTM to YO Tracking (Cont'd)

PROCEDURE

NOTE: This procedure requires that A3S1 is set to the factory-set position. Refer to Table 3-3 in the Operation Section of this manual.

NOTE: During this adjustment, a localized drop in power may occur. This drop in power is due to the SRD being over biased and is called squegging. If squegging occurs in band 2, adjust A6R68 and R73 to eliminate it and to maximize power across the band. If squegging occurs in band 3, adjust A6R69 and A6R74.

1. Connect the equipment as shown in Figure 5-16. Allow the equipment to warm up for 1 hour.
2. On the sweep oscillator/RF plug-in:

   Press **[INSTR PRESET]**

   Press **[START] [7] [GHz]**

   Press **[EXT]**.

   Press **[SAVEn] [3]**

   The unleveled lamp should be lit.
3. Preset A6R78 (T) 1/4 turn from the full clockwise position.
4. Turn channel 2 off on the scalar network analyzer and select 5 dB/DIV display resolution. Center the display by adjusting the reference position.
5. On the sweep oscillator/RF plug-in:

   Press **[SHIFT] [9] [2]** to enable the SYTM OFFSET DAC subroutine.

   Using the RF plug-in POWER control, peak the power in the beginning of band 2.
6. Press **[SHIFT] [9] [3]** to enable the SYTM GAIN DAC subroutine. Using the RF plug-in POWER control, peak the power at the end of band 3. Maximum peaking occurs when the power at the high end of band 3 has been optimized without the power in other bands dropping out.
7. Iterate between steps 5 and 6. SHIFT 92 and 93 are interactive so the adjustments must be alternated until the best comprimise is found.
8. On the sweep oscillator/RF plug-in:

   Press **[SHIFT] [9] [2]**. Set A7S1 to the hex code on the plug-in display (Figure 5-19).

   Press **[SHIFT] [9] [3]**. Set A7S2 to the hex code on the plug-in display (Figure 5-19).
9. Press **[INSTR PRESET]** so that the new calibration data will be entered from the current switch settings.
10. Turn channel 2 off on the scalar network analyzer and select 5 dB/DIV display resolution. Center the display by adjusting the reference position.

5-7. Slow Sweep SYTM to YO Tracking (Cont'd)

11. Press **[RECALLn] [3]**

    Press **[STOP] [7] [GHz]**

    [SWEEP TIME] [4] [0] [0] [ms]

    Press **[INT]** ALC MODE

12. Press **[POWER LEVEL]** and adjust rotary knob to increase the power until the UNLEVELED LED begins to light.

13. Adjust A7R51 (B1 OFS) until the UNLEVELED LED is no longer lit.

14. Iterate between steps 12 and 13 until maximum leveled power in band 1 is achieved.

5-7. Slow Sweep SYTM to YO Tracking (Cont'd)

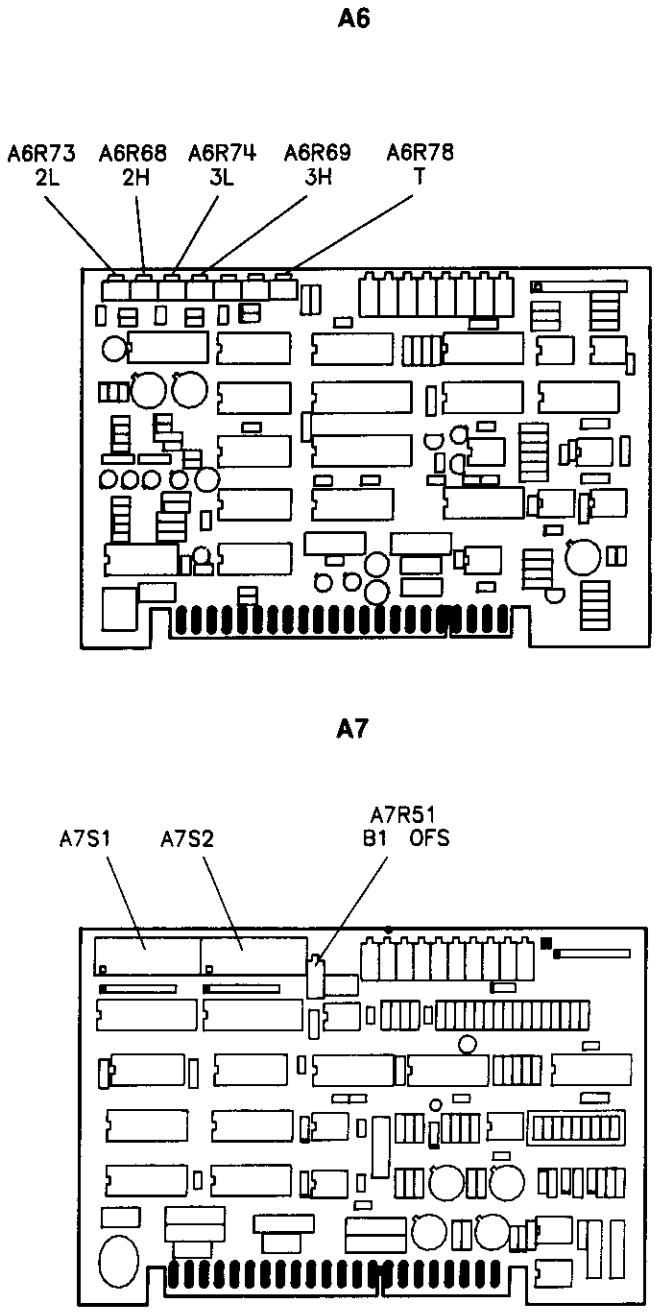


Figure 5-17. Slow Sweep SYTM To YO Tracking Adjustment Locations

5-7. Slow Sweep SYTM to YO Tracking (Cont'd)

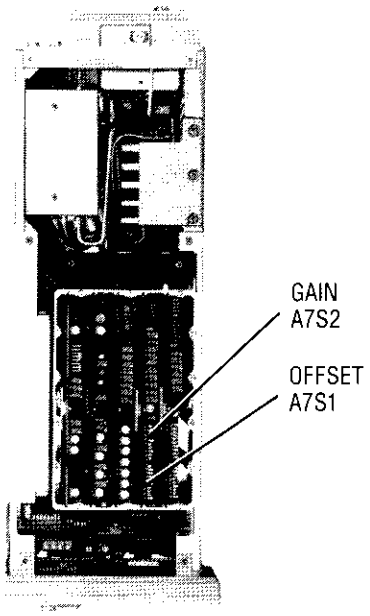


Figure 5-18. SYTM to YO Tracking Calibration Switch Location

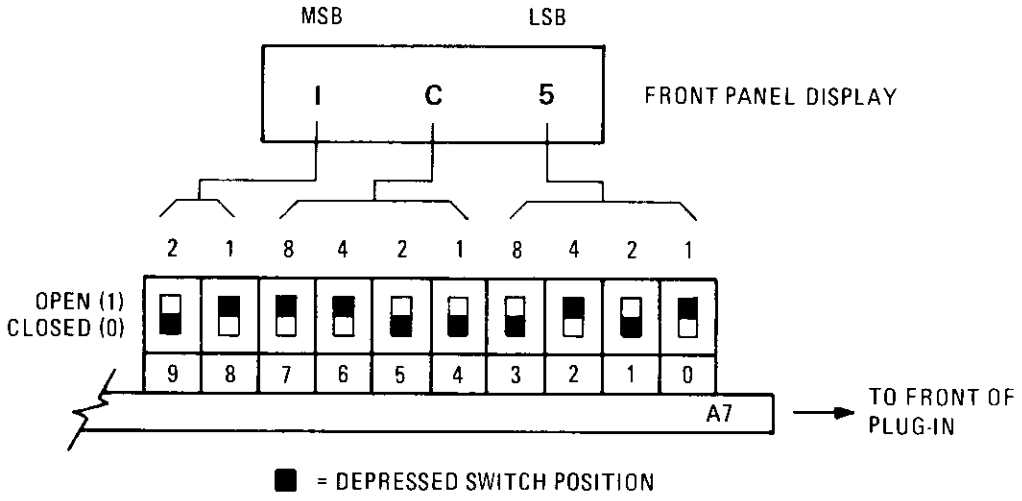


Figure 5-19. SYTM to YO Tracking Calibration Switch Configuration

5-8. SRD BIAS

DESCRIPTION

The high power SRD bias is set by peaking the HP 8757A displayed trace with A6R68 (2H) and A6R73 (2L0) in band 2, A6R69 (3H) and A6R74 (3L) in band 3.

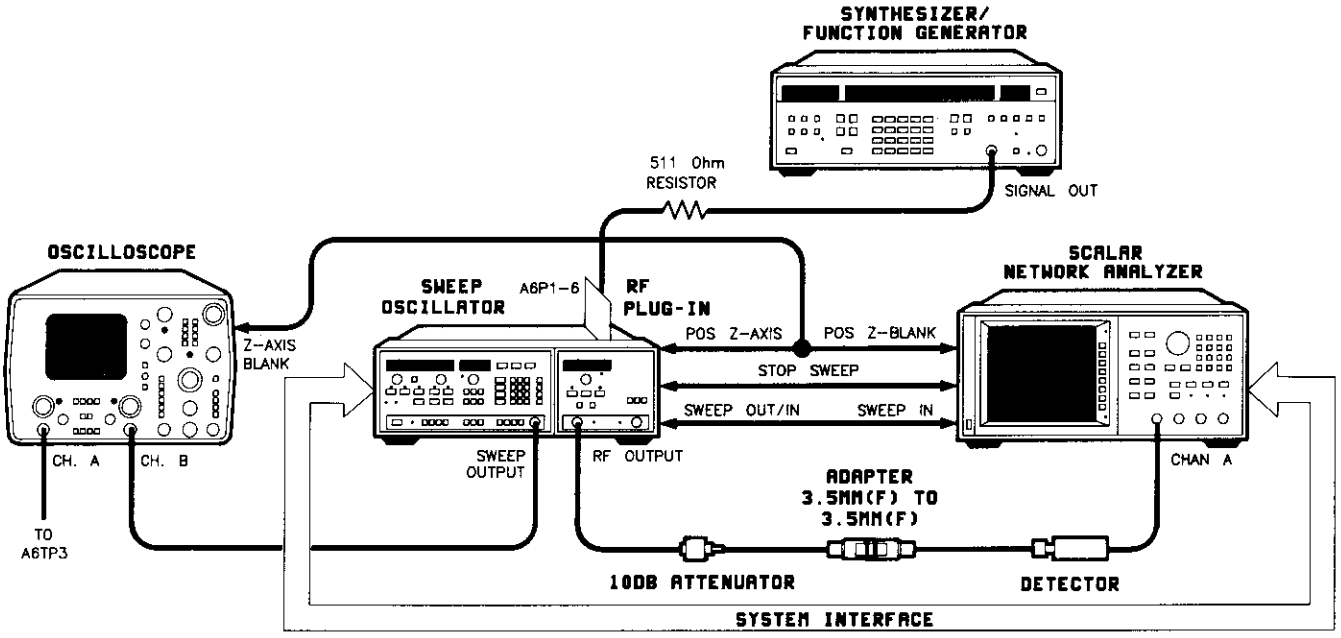
The low and mid-power SRD bias is adjusted by inserting a voltage through a 511 ohm current limiting resistor to directly bias the modulator/splitter. With the HP 83595A at maximum RF output, the power supply voltage is increased (minimum voltage 0.5 VDC, maximum voltage 5.0 VDC) to set the RF output power just above the HP 8757A noise floor. Then A6R63 (3HL) is adjusted until minimum slope is obtained on the oscilloscope display. The voltage from the power supply is decreased until the lowest part of the trace is 10 dB above the noise floor. Then A6R12 (C) is adjusted to peak the power in bands 2 and 3. The power supply is then removed.

A low-pass filter is inserted before the detected HP 8757A input. A comparison between the normalized and low pass inputs are made to determine the SYTM fundamental feedthru.

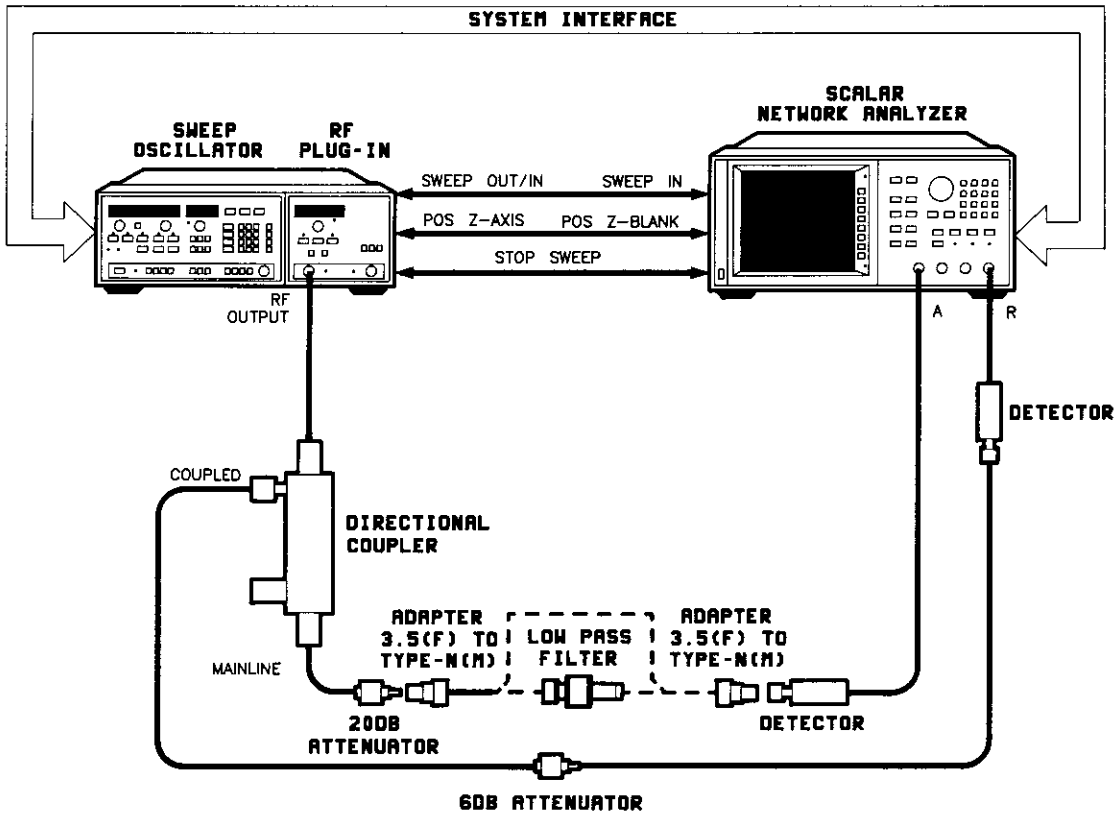
EQUIPMENT

Sweep Oscillator Mainframe	HP 8350
Scalar Network Analyzer	HP 8757A
Function Generator	HP 3325A
Detector (2)	HP 85025B
6 dB Attenuator	HP 8493C Option 006
10 dB Attenuator	HP 8493C Option 010
20 dB Attenuator	HP 8493C Option 020
Directional Coupler	HP Part No. 0955-0125
Extender Board	HP Part No. 08350-60031
511 Ohm Resistor	HP Part No. 0757-0416
Low-pass Filter	HP 11684
Adapter 3.5 (m) to N (f)	HP Part No. 1250-1743
Adapter 3.5 (f) to N (m)	HP Part No. 1250-1744
Adapter 3.5 (f) to N (f)	HP Part No. 1250-1745
Adapter 3.5 (f) to 3.5 (f)	HP Part No. 1250-1749
Adapter 3.5 (m) to N (f)	HP Part No. 1250-1750

5-8. SRD BIAS (Cont'd)



a) Low and Mid-Power Test Setup



b) YTM Fundamental Feedthru Test Setup

Figure 5-20. SRD Bias Adjustment Test Setups

5-8. SRD DIAS (Cont'd)

PROCEDURE

NOTE: Turn HP 8350 LINE power OFF when removing or installing PC boards.

NOTE: This procedure requires that A3S1 is set to the factory-set position. Refer to Table 3-3 in the Operation Section of this manual.

High Power SRD Bias

1. Connect the equipment as shown in Figure 5-20(a) with the HP 83595A A6 sweep control board on an extender. Do not connect the function generator. With the LINE power OFF, remove the HP 83595A A4 ALC board. Connect the scalar network analyzer MODULATOR DRIVE output to the RF plug-in rear panel PULSE IN connector.
2. Allow the equipment to warm up for 1 hour.
3. On the sweep oscillator/RF plug-in:

   Press **[INSTR PRESET] [START] [6] [.] [9] [GHz]**

   Press **[STOP] [1] [3] [.] [5] [GHz]**

   Press **[SWEEP TIME] [4] [0] [0] [ms]**

   Press **[EXT]** ALC MODE

   Press **[⌐¬MOD]** to off
4. Set the scalar network analyzer display resolution for 5 dB/DIV and center the display.
5. Set up a zero volt reference on the oscilloscope.

NOTE: Before beginning each adjustment, preset the potentiometer to the point where one side of the trace on the oscilloscope display is below zero volts. Adjustment locations labeled 2L and 3L set the left side of the displayed trace. Adjustment locations labeled 2H and 3H set the right side of the displayed trace. Do not preset more than one potentiometer at one time.

6. Observe the scalar network analyzer display, adjust A6R73 (2L) to peak the power of the low end of band 2 without the power squegging. Then adjust A6R68 (2H) to peak the rest of the band. Iterate between (2L) and (2H) to peak the power across the band without any squegging.
7. On the sweep oscillator/RF plug-in:

   Press **[START] [1] [3] [.] [4] [GHz]**

   Press **[STOP] [2] [0] [GHz]**

   Adjust A6R74 (3L) for the low end of band 3 and A6R69 (3H) for the rest of the band to peak the power without squegging.

5-8. SRD DIAS (Cont'd)

8. On the sweep oscillator/RF plug-in:

   Press **[START] [1] [9] [.] [9] [GHz]**

   Press **[STOP] [2] [6] [.] [5] [GHz]**

   Adjust A6R75 (4L) for the low end of band 4 and A6R70 (4H) for the rest of the band to peak the power without squegging.

9. Check the SYTM to YO tracking to ensure it has not changed. If retracking is necessary, repeat the steps above to eliminate any squegging that may have occured.

Low and Mid Power SRD Bias

CAUTION

The voltage connected to A6P1-6 is to bias the modulator/splitter directly. If the A6 P1-7 (+10VDC) is shorted to A6P1-6, the modulator/splitter will be damaged.

10. Set up the equipment as shown in Figure 5-20(a) with a 511 ohm resistor connected to A6P1-6 (reference to ground). Remove the RF plug-in A4 ALC board. Connect the scalar network analyzer MODULATOR DRIVE output to the RF plug-in rear panel PULSE IN connector.

11. Allow the equipment to warm up for one hour.

12. On the sweep oscillator/RF plug-in:

    Press **[INSTR PRESET]**

    Press **[⌐MOD]** to off

    Press **[START] [7] [.] [0] [GHz]**

    Press **[SWEEP TIME] [2] [0] [0] [ms]**

    Press **[POWER LEVEL] [2] [0] [dB]**

13. Set the scalar network analyzer display resolution for 10 dB/DIV and adjust the display to the top graticule.

14. Set the oscilloscope as follows:

    Select A vs. B mode

    Set channel A to .5V/DIV, DC coupled

    Set channel B to 1V/DIV, DC coupled

15. Set the function generator voltage to .5 VDC. Increase the voltage until the highest power point is 10 dB above the noise floor (DO NOT EXCEED 5 VDC).

16. Monitor A6TP3 with the oscilloscope and adjust A6R63 (3HL) until minimum slope (flat display) is obtained.
17. Decrease the function generator voltage until the power at the lowest point between 6.9 and 26.5 GHz is 10 dB above the noise floor.
18. Set A6R12 (C) to a centered position and then adjust to peak the power between 6.9 and 26.5 GHz. Using the voltage source, keep the RF power at or near 10 dB above the noise floor, then repeak A6R12 (C). If the power of the sweep drops at any frequency, maximum peaking has been exceeded.
19. Repeat step 16 to verify baseline flatness, readjust A6R63 as needed.

Threshold

NOTE: For this adjustment to be accurate, the attenuator must be in the 0.0 dB step (Opt 002 only).

20. On the sweep oscillator/RF plug-in:

    Press **[INSTR PRESET]**

    Press **[⌐MOD]** to off

    Press **[POWER LEVEL] [-] [5] [dB]**

21. Observe the scalar network analyzer with a 1 dB/DIV reference. Preset A6R78 (T) clockwise, then adjust counter-clockwise until squegging and /or oscillations are eliminated.
22. Increase power slowly to maximum specified power out. If squegging or oscillations reoccur, readjust A6R78 (T) in small increments. If excessive adjustment of A6R78 (T) is required, the SRD bias may be misadjusted.

SYTM Fundamental Feedthrough

23. Set the equipment as shown in Figure 5-20(b) without the low-pass filter, and with the RF plug-in A4 ALC board installed.
24. Allow the equipment to warm up for one hour.
25. On the sweep oscillator/RF plug-in:

    Press **[INSTR PRESET] [START] [8] [GHz]**

26. On the scalar network analyzer:

    Press **[MEAS]**, then select **[A/R]**

    Press **[SCALE]**, then select **[AUTO SCALE] [10] [dB]**.

    Press **[DISPLAY]**, then select **[MEAS→MEM] [MEAS-MEM]**

    The trace on the scalar network analyzer should be flat, showing that system errors have been removed.

5-8. SRD DIAS (Cont'd)

27. Install the low-pass filter at the location shown in Figure 5-20(b).

28. The SYTM fundamental feedthru is now displayed on the scalar network analyzer.

    Press **[CURSOR]**

29. Use the cursor to indicate how many dB the trace is below the reference position established in step 26. If the any portion of the trace is less than 25 dB below the reference between 8 GHz and 26.5 GHz, repeat paragraph 5-8.

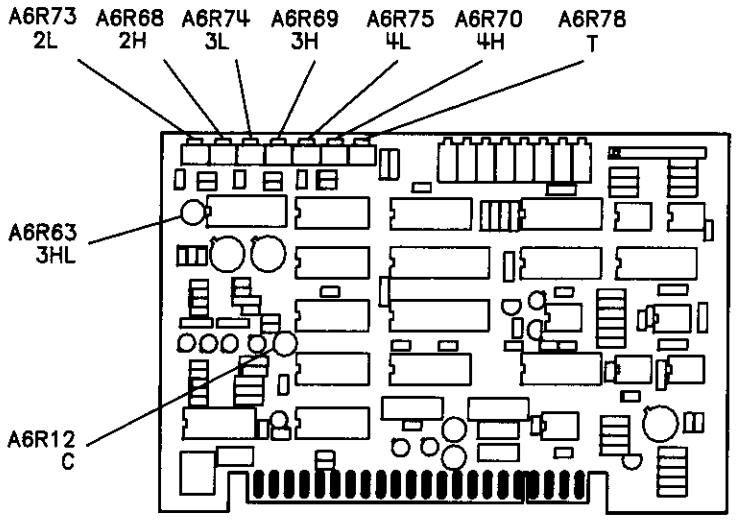


Figure 5-21. SRD Bias Adjustment Locations

5-9. SYTM Delay Compensation

DESCRIPTION

The SYTM delay compensation circuit is adjusted to optimize SYTM to YO tracking over varying sweep rates. Adjustments are provided for sequential sweeps (multiband) and single band sweeps.

EQUIPMENT

Sweep Oscillator Mainframe	HP 8350
10 dB Attenuator	HP 8493C Option 010
Oscilloscope	HP 1741A
Detector	HP 8473C

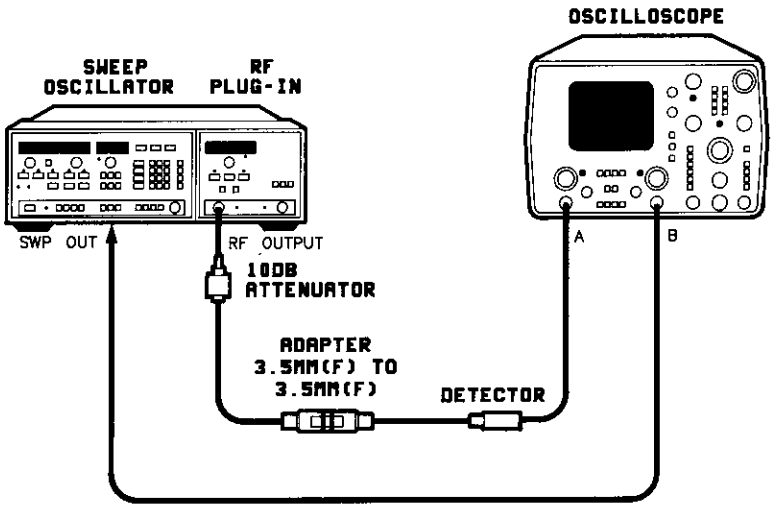


Figure 5-22. SYTM Delay Compensation Adjustment Test Setup

PROCEDURE

NOTE: This procedure requires that A3S1 is set to the factory-set postion. Refer to Table 3-3 in the Operation Section of this manual for switch configuration information.

1. Connect the equipment as shown in Figure 5-22. Do not connect the BNC cable between the HP 8350 rear panel POS Z BLANK and the Z AXIS input connector on the oscilloscope rear panel. Preset A7R45 (SEQ TC) fully counter-clockwise. Refer to Figure 5-23 for adjustment locations. Allow the equipment to warm up for 1 hour.

5-9. SYTM Delay Compensation (Cont'd)

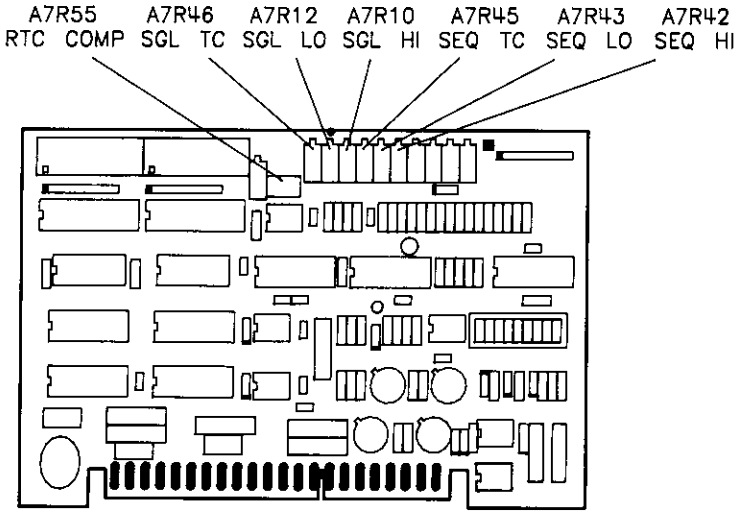


Figure 5-23. SYTM Delay Compensation Adjustment Locations

2. Set the oscilloscope controls as follows:

   Set channel A to .2 Volts/DIV, DC coupled
   Set channel B to 1 Volt/DIV, DC coupled
   Select A vs.B mode

3. On the sweep oscillator/RF plug-in:

   Press **[INSTR PRESET] [⌐MOD] [EXT]** ALC MODE **[SAVEn] [1]**

   Press **[TIME] [0] [.] [5] [s] [SAVEn] [2]**

4. Press **[RECALLn] [1]**

   Adjust A7R45 (SEQ TC) for the highest power with the best defined (brightest) bandswitch point between band 2 and band 3. By dimming the oscilloscope intensity, the brightest bandswitch point can become more apparent.

5. Connect a BNC cable from the HP 8350 rear panel POS Z BLANK connector to the scalar network analyzer rear panel POS Z BLANK connector.

6. Adjust A7R43 (SEQ LO) for maximum power at the beginning of band 2.

7. Adjust A7R42 (SEQ HI) for maximum power at the end of band 3.

8. On the sweep oscillator/RF plug-in, iterate between **[RECALLn] [1]** and **[RECALLn] [2]** while readjusting A7R42 (SEQ HI) and A7R43 (SEQ LO) as necessary to minimize the power level changes.

9. On the sweep oscillator/RF plug-in:

   Press **[START] [7] [.] [1] [GHz]**

   Press **[SWEEP TIME] [2] [5] [ms]**

5-9. SYTM Delay Compensation (Cont'd)

10. Adjust A7R55 (RTC COMP) for maximum power in band 2.

11. Vary the HP 8350 START FREQUENCY control from 10 MHz to 13 GHz to check for power variations. Readjust A7R42 (SEQ HI), A7R43 (SEQ LO), and A7R55 (RTC COMP) as necessary to minimize any drop in power (particularly near 26.5 GHz). The worst case drop should not exceed 0.5 dB as the start frequency is varied (the scale resolution on the oscilloscope display is approximately 2 dB/DIV). If this step cannot be met, repeat the Slow Speed YTM to YO Tracking Adjustments.

12. On the sweep oscillator/RF plug-in:

    Press **[INSTR PRESET] [EXT]** ALC MODE.

13. Repeatedly press **[SINGLE SWEEP TRIGGER]** while watching the displayed power level. Readjust A7R42 (SEQ HI) and A7R43 (SEQ LO) as necessary to minimize the power level difference between a 25 msec single sweep and a 25 msec internal sweep.

14. On the sweep oscillator/RF plug-in:

    Press **[INSTR PRESET] [START] [6] [.] [9] [GHz]**

    Press **[STOP] [1] [3] [.] [5] [GHz] [EXT]** ALC MODE.

15. Preset A7R46 (SGL TC) fully counter-clockwise.

16. While continuously changing the SWEEP TIME control for a sweep speed from 25 msec to 100 msec, adjust A7R12 (SGL LO) to maximize power at the low end of band 2. In the same manner, adjust A7R10 (SGL HI) to maximize the power at the high end of band 2. Then adjust A7R46 (SGL TC) to maximize the power at the very start of the band.

17. On the sweep oscillator/RF plug-in:

    Press **[START] [1] [3] [.] [4] [GHz]**

    Press **[STOP] [2] [0] [GHz]**

    Vary the sweep speed as in step 16 and note any drop in power. If the change is greater than 0.5 dB, make slight adjustments to A7R10 (SGL HI) and A7R12 (SGL LO). If it is necessary to adjust A7R10 (SGL HI) and A7R12 (SGL LO), repeat step 16 and 17 until the power variation while adjusting sweep time is less than 0.5 dB.

5-10. Band Overlap

DESCRIPTION

The HP 83595A is swept across each bandswitch point. A frequency meter is set to the bandswitch frequency, and the gain of the variable gain amplifier on the A6 sweep control assembly is adjusted for a smooth frequency transition between bands.

EQUIPMENT

Sweep Oscillator Mainframe	HP 8350
Oscilloscope	HP 1741A
Spectrum Analyzer	HP 8566B

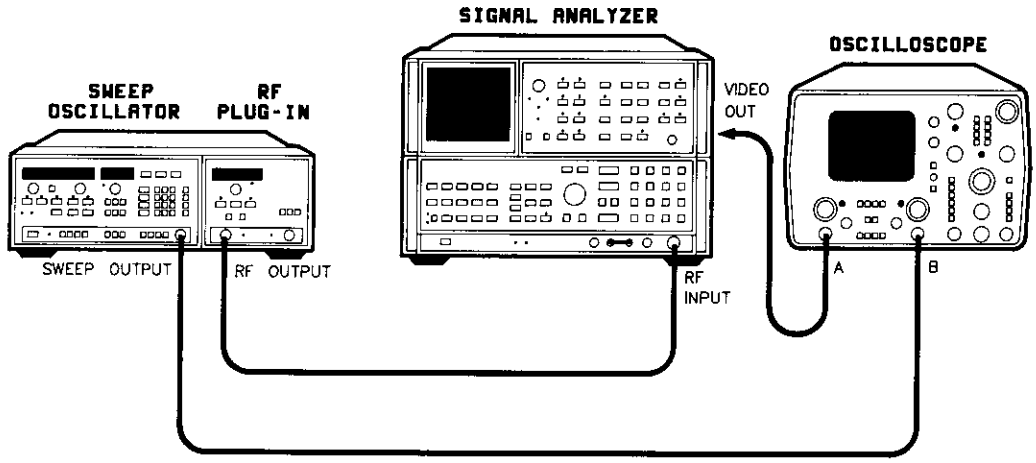


Figure 5-24. Band Overlap Adjustment Test Setup

PROCEDURE

NOTE: This procedure requires that A3S1 be set to the factory-set position. Refer to the operation section of this manual for switch configuration information.

1. Connect the equipment as shown in Figure 5-24. Allow the equipment to warm up for 1 hour.
2. On the sweep oscillator/RF plug-in:

   Press **[INSTR PRESET]**

   Press **[CF] [2] [.] [3] [5] [GHz] [△F] [1] [5] [0] [MHz]**
3. Set the oscilloscope for A versus B display mode to display amplitude versus frequency. Center the display on screen.

5-10. Band Overlap (Cont'd)

4. On the spectrum analyzer:

   Press **[CENTER FREQUENCY] [2] [.] [3] [5] [GHz]**.

5. Center the bandswitch point on the display using the HP 8350 FREQUENCY control.

6. Adjust the spectrum analyzer center frequency to put the left half of the pip on the left side of the switch point.

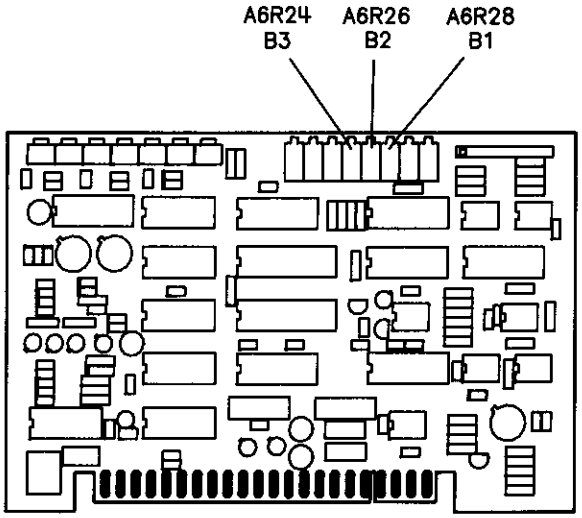


Figure 5-25. Band Overlap Adjustment Locations

7. Adjust A6R28 (B1) to bring the right side pip over to the switch point so that the left half of this pip mates with the right half of the other as shown in Figure 5-26. Refer to Figure 5-25 for the adjustment location. The pip should be undisturbed as it moves through the bandswitch point.

5-10. Band Overlap (Cont'd)

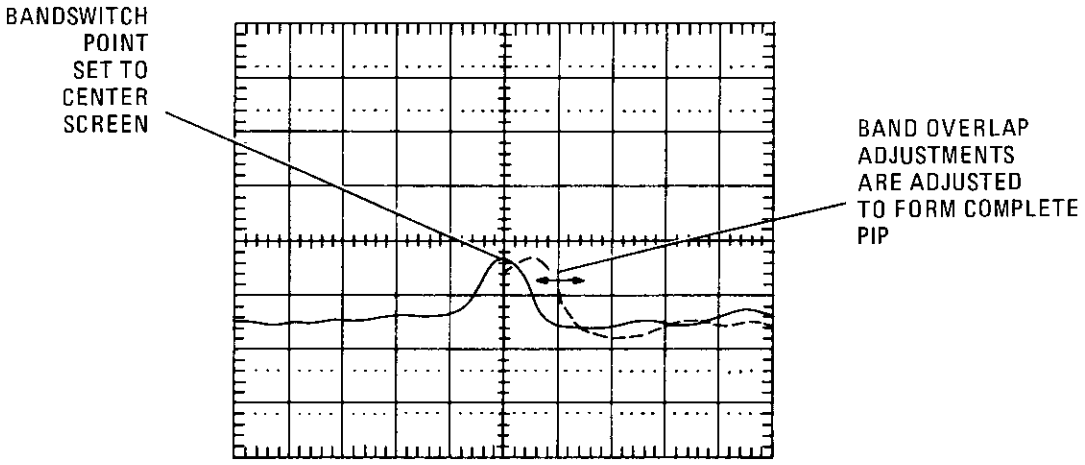


Figure 5-26. Band Overlap Adjustment Waveform

8. On the spectrum analyzer:

   Press **[CENTER FREQUENCY] [7] [.] [0] [GHz]**

9. On the sweep oscillator/RF plug-in:

   Press **[CF] [6] [.] [9] [5] [GHz]**

10. Repeat steps 5 through 7 but, this time, adjust A6R26 (B2) in step 7.

11. On the spectrum analyzer:

    Press **[CENTER FREQUENCY] [1] [3] [.] [4] [5] [GHz]**

12. On the sweep oscillator/RF plug-in:

    Press **[CF] [1] [3] [.] [4] [5] [GHz]**

13. Repeat steps 5 through 7 but, this time, adjust A6R24 (B3) in step 7.

14. On the spectrum analyzer:

    Press **[CENTER FREQUENCY] [1] [9] [.] [9] [5] [GHz]**

15. On the sweep oscillator/RF plug-in:

    Press **[CF] [1] [9] [.] [9] [5] [GHz]**

16. Repeat steps 5 through 7 but, this time, adjust A6R24 (B3) in step 7.

17. Repeat steps 11 through 16 to obtain a compromise between bands 3 and 4.

5-11. Frequency Reference 1V/GHz Output

DESCRIPTION

The frequency reference rear panel output is adjusted for 1V/GHz output. Example: 1 GHz = 1 Volt; 2 GHz = 2 Volts, etc.

EQUIPMENT

Digital Voltmeter ..... HP 3456A
Sweep Oscillator Mainframe ..... HP 8350

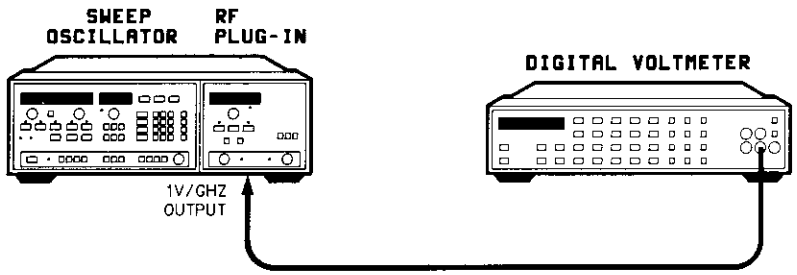


Figure 5-27. Frequency Reference 1 V/GHz Output Test Setup

PROCEDURE

NOTE: Frequency accuracy must be adjusted accurately (Paragraph 5-4) before adjusting Frequency Reference 1V/GHz Output.

NOTE: Ensure that A2S1 is set for 1V/GHz output before performing this adjustment. Refer to Table 3-3 in the Operation Section of this manual for switch configuration information.

1. Connect the equipment as shown in Figure 5-27 with the DVM connected to the rear panel 1V/GHz frequency reference connector, J4. Allow the equipment to warm up for 1 hour.

Bands 1 through 3

2. Adjust A2R4 (OFFSET) to the center of its mechanical range. Refer to Figure 5-28 for the adjustment location.
3. On the sweep oscillator/RF plug-in:

   Press **[CW] [8] [GHz]**

5-11. Frequency Reference 1V/GHz Output (Cont'd)

4. Adjust A2R1 (GAIN) for a DVM reading of 8.000 ±0.005 VDC.
5. On the sweep oscillator/RF plug-in:

   Press **[CW] [1] [5] [GHz]**
6. Adjust A2R4 (OFFSET) for a DVM reading of 15.000 ±0.005 VDC.
7. Repeat steps 2 through 6 until the indicated voltages are obtained.

Band 0

8. Adjust A2R6 (BAND 0 OFFSET) to the center of its mechanical range.
9. On the sweep oscillator/RF plug-in:

   Press **[CW] [1] [0] [MHz]**
10. Adjust A2R6 (BAND 0 OFFSET) for a DVM reading of 0.010 ±0.005 VDC.
11. On the sweep oscillator/RF plug-in:

    Press **[CW] [2] [GHz]**
12. Adjust A2R23 (BAND 0 GAIN) for a DVM reading of 2.000 ±0.005 VDC.
13. Repeat steps 8 through 12 until the indicated voltages are obtained.

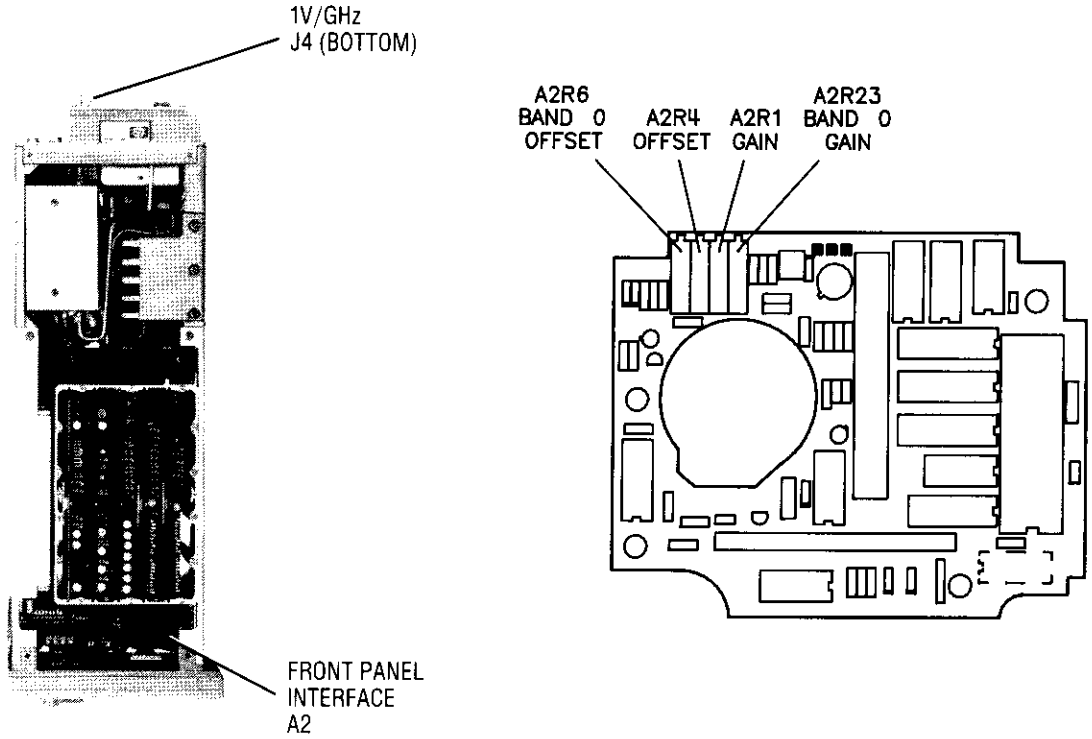


Figure 5-28. Frequency Reference Adjustment Locations

5-12. ALC Adjustment

NOTE: Complete adjustment of the leveling loop requires several procedures to be performed in the order prescribed, from Paragraph 5-12 through 5-16. Deviation from this routine may cause improper leveling and/or power variation problems.

DESCRIPTION

Adjustments compensate for DC offsets in the detected RF path and the main ALC amplifier. Power is roughly calibrated and low band flatness is optimized.

EQUIPMENT

Sweep Oscillator Mainframe	HP 8350
Digital Voltmeter	HP 3456A
Power Meter	HP 436A
Power Sensor	HP 8485A
Scalar Network Analyzer	HP 8757A
Detector	HP 85025B
Extender Board	HP 08350-60031
10 dB Attenuator	HP 8493C Option 010
Adapter 3.5 (f) to Type-N (m)	HP Part No. 1250-1749

5-12. ALC Adjustment (Cont'd)

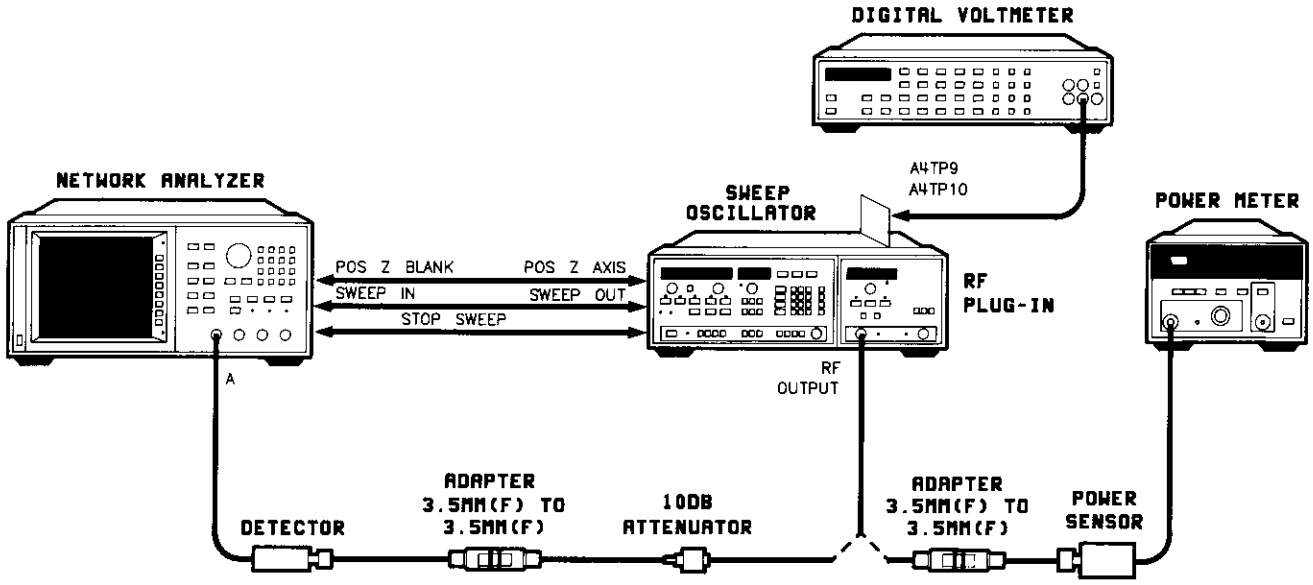


Figure 5-29. ALC Adjustment Test Setup

PROCEDURE

NOTE: Turn AC power OFF when removing or installing PC boards.

NOTE: This procedure assumes that A3S1 is set to the factory-set position. Refer to Table 3-3 in the Operation Section of this manual for switch configuration information.

1. Connect the equipment as shown in Figure 5-29. With AC power off, remove A5 FM driver board. Place A4 assembly on an extender board. Press **[INSTR PRESET] [CW]**. Sweep the full range of the plug-in at any leveled power. Preset the following adjustments as indicated:

A4R81 (OFS 1)	Midrange
A4R82 (OFS 2)	Midrange
A4R78 (OFS 3)	Midrange
A4R15 (GAIN)	Midrange
A4R7 (0 HI)	Fully CW
A4R8 (1 HI)	Fully CW
A4R14 (BIAS)	Midrange
A4R1 (SLP)	Midrange

5-12. ALC Adjustment (Cont'd)

2. Float the ground on the digital voltmeter and measure the voltage between A4TP9 and A4TP10. Refer to Figure 5-30 for adjustment locations. Adjust A4R81 (OFS 1) for 0.000 ±0.001 VDC.

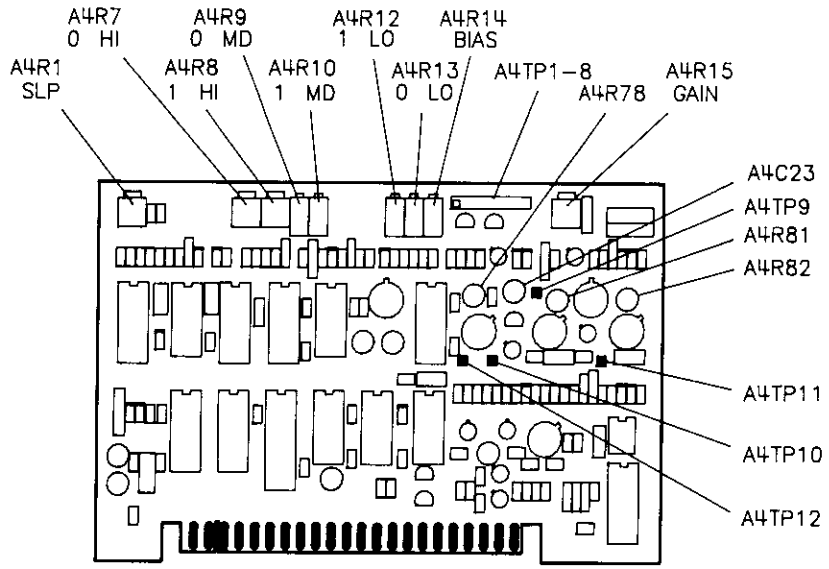


Figure 5-30. ALC Adjustment Locations

3. Attach a jumper from A4TP11 to ground. Connect DVM HI to A4TP4 (reference to ground) and adjust A4R82 (OFS 2) for a DVM reading of 0.000 ±0.001 VDC. Remove the jumper.

4. Connect the DVM between A4TP12 and A4TP9 (floating ground). Adjust A4R78 (OFS 3) for a DVM reading of 0.000 ±0.001 VDC.

5. On the sweep oscillator/RF plug-in:

   Press **[CW] [5] [0] [MHz]**

   Press **[RF]** power to off.

   Connect DVM HI to A4TP7 (ground to P1 pin 42) and adjust A4R14 (BIAS) for a DVM reading of 0.000 ±0.001 VDC.

   Press **[RF]** power to on.

6. Set the sweep oscillator line power to off. Remove the A4 assembly from the extender board and reinsert the A4 assembly directly into the instrument. Set the sweep oscillator line power to ON.

   Press **[CW] [5] [0] [MHz]**

   Connect the power meter to the plug-in RF output.

5-12. ALC Adjustment (Cont'd)

7. Press **[POWER LEVEL] [-] [5] [dBm]**

   Adjust A4R13 (0 LO) for an RF output power of −5 ±0.1 dBm.

8. Press **[POWER LEVEL] [7] [dBm]**

   Adjust A4R9 (0 MD) for an RF output power of +7 ±0.1 dBm.

9. Iterate between steps 7 and 8 until both low and midpower ranges are calibrated and no readjustment is necessary.

10. Press **[POWER LEVEL] [1] [0] [dBm]**

    Adjust A4R7 (0 HI) for an RF output power at the HP 83595A connector of +10 ±0.1 dBm.

11. Disconnect the power meter and monitor the RF output with the HP 8757A.

12. On the sweep oscillator/RF plug-in:

    Press **[INSTR PRESET]** to sweep the full range of the plug-in.

    Press **[POWER LEVEL] [-] [3] [dBm]**

    Press **[RF BLANK]**

    Press **[SAVEn] [1]**

13. Select 1 dB/DIV display resolution on the scalar network analyzer.

14. Adjust A4R1 (SLP) for best overall flatness from 10 MHz to 2.4 GHz as observed on the scalar network analyzer.

15. Adjust A4R12 (1 LO) for best continuity at the bandswitch point at 2.4 GHz.

16. On the sweep oscillator/RF plug-in:

    Press **[POWER LEVEL] [7] [dBm]**

    Press **[SAVEn] [2]**

    Adjust A4R10 (1 MD) for best continuity at the bandswitch point.

17. On the sweep oscillator/RF plug-in:

    Press **[POWER LEVEL] [1] [0] [dBm]**

    Press **[SAVEn] [3]**

    Adjust A4R8 (1 HI) for best trace continuity at the bandswitch point.

18. Iterate between steps 15, 16, and 17 using RECALL 1, 2, and 3 until trace continuity at all three power settings is achieved.

19. With the AC power off, reinstall the A5 FM driver board assembly.

5-13. Power Calibration

NOTE: Complete adjustment of the leveling loop for power meter leveling requires several procedures to be performed in the order prescribed from Paragraph 5-12 through 5-16. Deviation from this routine may cause improper leveling and/or power variation problems.

DESCRIPTION

Power is calibrated on a power meter at three points over the leveled power range: −5, +3, and +10 dBm.

EQUIPMENT

Scalar Network Analyzer	HP 8757A
Detector	HP 85025B
Power Meter	HP 436A
Power Sensor	HP 8485A
Sweep Oscillator Mainframe	HP 8350
Adapter 3.5 (f) to 3.5 (f)	HP Part No. 1250-1749

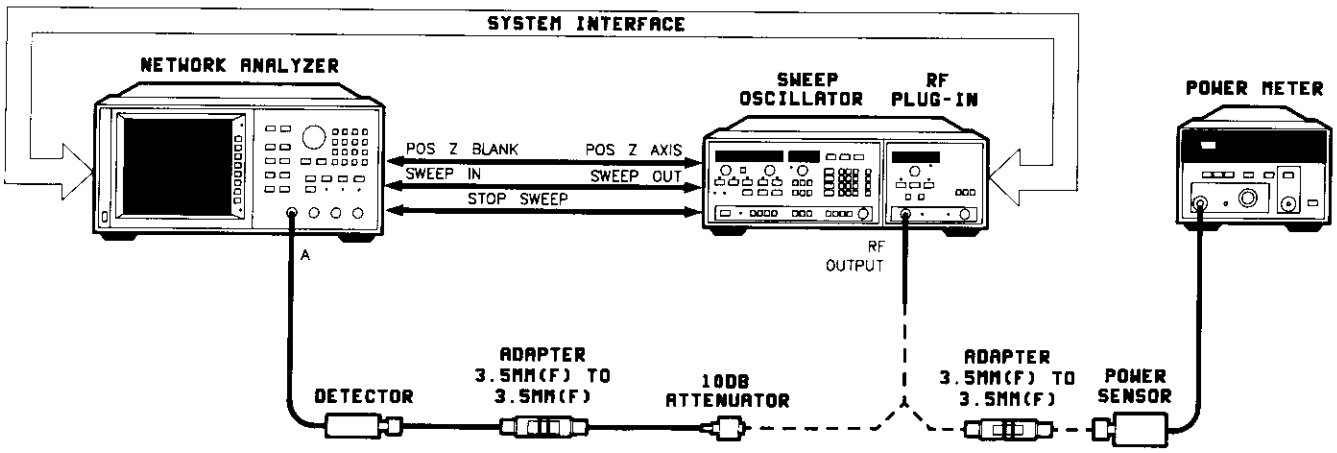


Figure 5-31. Power Calibration Test Setup

5-13. Power Calibration (Cont'd)

PROCEDURE

NOTE: This procedure assumes that A3S1 is set to the factory-set position. Refer to Table 3-3 in the Operation Section of this manual for switch configuration information. If the following steps result in A4R13 and A4R9 being adjusted near the end of their mechanical range, connect DVM LO to A4TP12 (floating ground) and DVM HI to A4TP9. Adjust A4R78 for −0.2mV ± 0.01mV.

Before proceeding with the power calibration, the instrument MUST be warmed up for 30 minutes minimum with the cover on in order to stabilize the power.

1. Connect the equipment as shown in Figure 5-31 with the power meter connected to the RF output. Allow 30 minutes for warm-up.
2. On the sweep oscillator/RF plug-in:

   Press **[INSTR PRESET]**

   Press **[⌐¬MOD] [CW] [5] [0] [MHz]**
3. Set the plug-in for a front panel display of −5 dBm and press **[SAVEn] [1]**.
4. Press **[CW] [2] [.] [2] [GHz]** and **[SAVEn] [2]**.
5. Set the plug-in for a front panel display of +3 dBm and press **[SAVEn] [5]**.
6. Press **[CW] [5] [0] [MHz]** and **[SAVEn] [4]**.
7. Set the plug-in for a front panel display of +10 dBm and press **[SAVE] [7]**.
8. Press **[CW] [2] [.] [2]** and **[SAVEn] [8]**.
9. Adjust A4R1 (SLP) to get the same but opposite difference between (50 MHz and 2.2 GHz at −5 dBm) and (50 Mhz and 2.2 GHz at +10 dBm). See Figure 5-32.

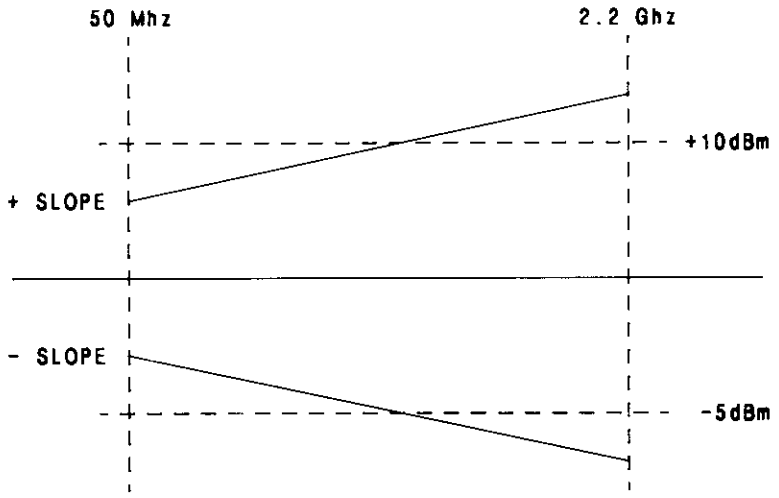


Figure 5-32. 0 Slope Adjustment

5-13. Power Calibration (Cont'd)

10. Adjust A4R13 (0 LO) for equal but opposite deviations from −5 dBm at 50 MHz and 2.2 GHz using registors 1 and 2.
11. Adjust A4R9 (0 MD) for equal but opposite deviations from +3 dBm at 50 MHz and 2.2 GHz using registors 4 and 5.
12. Adjust A4R7 (0 HI) for equal but opposite deviations from +10 dBm at 50 MHz and 2.2 GHz using registors 7 and 8.
13. Connect the scalar network analyzer to the RF plug-in output.
14. On the sweep oscillator/RF plug-in:

    Press **[INSTR PRESET]**

    Press **[START] [2] [.] [3] [GHz] [STOP] [7] [GHz]**

    Observing the scalar network analyzer, locate the frequency which is the mid-point of band 1 power variation, and set CW to that frequency.
15. Connect the power meter to the RF plug-in output connector.
16. Set the plug-in for a front panel display of −5 dBm and adjust A4R12 (1 LO) for a power meter reading of −5 dBm.
17. Set the HP 83595A for a front panel display of +3 dBm and adjust A4R10 (1MD) for a power meter reading of +3 dBm.
18. Set the HP 83595A for a front panel display of +10 dBm and adjust A4R8 (1HI) for a power meter reading of +10 dBm.
19. Repeat steps 2 through 18 until no further adjustment is necessary.

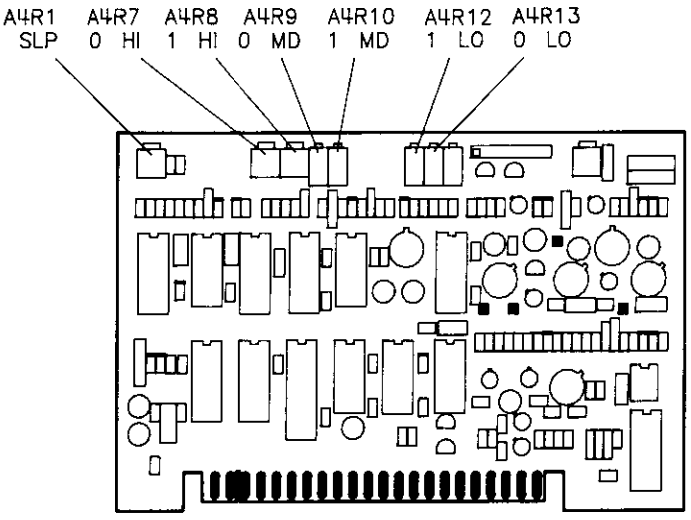


Figure 5-33. Power Calibration Adjustment Locations

5-14. Internal Leveled Flatness

NOTE: Complete adjustment of the leveling loop requires several procedures to be performed in the order prescribed, from Adjustments 5-12 through 5-16. Deviation from this routine may cause improper leveling and/or flatness problems.

DESCRIPTION

Four parallel circuits on the A5 assembly provide adjustments for ALC flatness. BP1 through BP4 and SL1 through SL4 determine the shape of the flatness compensation signal.

EQUIPMENT

Sweep Oscillator Mainframe	HP 8350
Scalar Network Analyzer	HP 8757A
Detector	HP 85025B
10 dB Attenuator	HP 8493C Option 010
Adapter 3.5 (f) to 3.5 (f)	HP Part No. 1250-1749

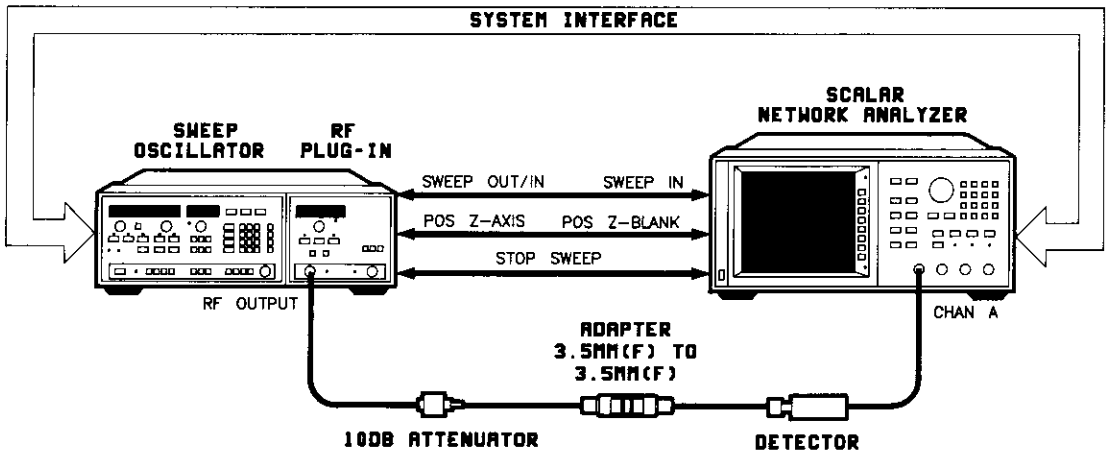


Figure 5-34. Internal Leveled Flatness Adjustment Test Setup

5-14. Internal Leveled Flatness (Cont'd)

PROCEDURE

1. Connect the equipment as shown in Figure 5-34. Allow 30 minutes for warm-up.
2. On the scalar network analyzer:

   Press **[PRESET]**. Select **[CHANNEL 2 OFF]**.

   Press **[SYSTEM]**. Select **[MODE DC]**.

   Select **[CAL] [DC DET ZERO] [MANUAL]**. Before completing the detector zero, turn the plug-in's RF output power off.

   Select **[CONT]**.
3. On the sweep oscillator/RF plug-in:

   Press **[RF]** to on

   After the scalar network analyzer preset, the oscillator should be in full sweep range, 10.0 MHz to 26.5 GHz and the sweep time should be 0.2 seconds.

Preset the Adjustments

4. Set A5R34, A5R36, A5R38, and A5R40 (BP1 – BP4) fully CW. Set A5R41 through A5R44 (SL1 –SL4) to mid-range. Refer to Figure 5-35.

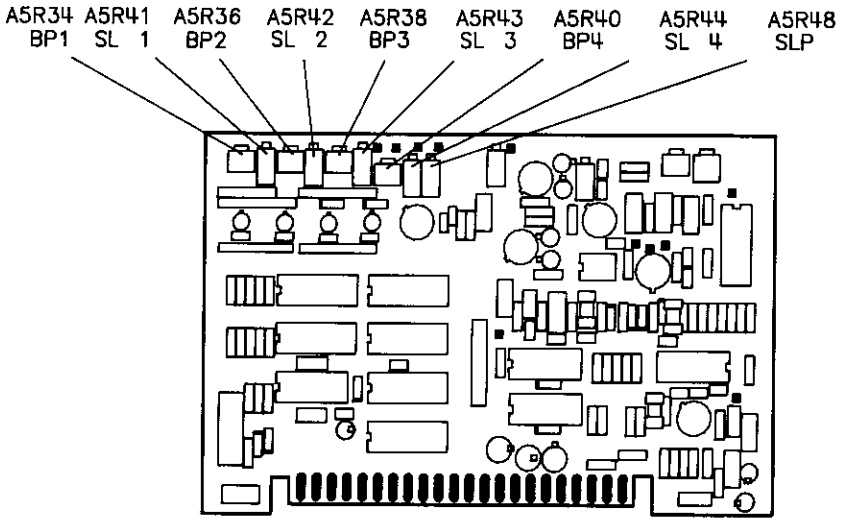


Figure 5-35. Internal Leveled Flatness Adjustment Location

5-14. Internal Leveled Flatness (Cont'd)

5. On the scalar network analyzer:
   Press **[SCALE] [1] [dB]**.

   Press **[REF]**, then select **[REF LEVEL]** and use the rotary knob to center the trace on the display. Adjust **[REF POSN]** to center the reference line. Refer to Figure 5-36.

6. On the sweep oscillator/RF plug-in:

   Adjust the overall slope adjust, A5R48 (SLP), for the flattest display, as shown on the scalar network analyzer. Refer to Figure 5-37.

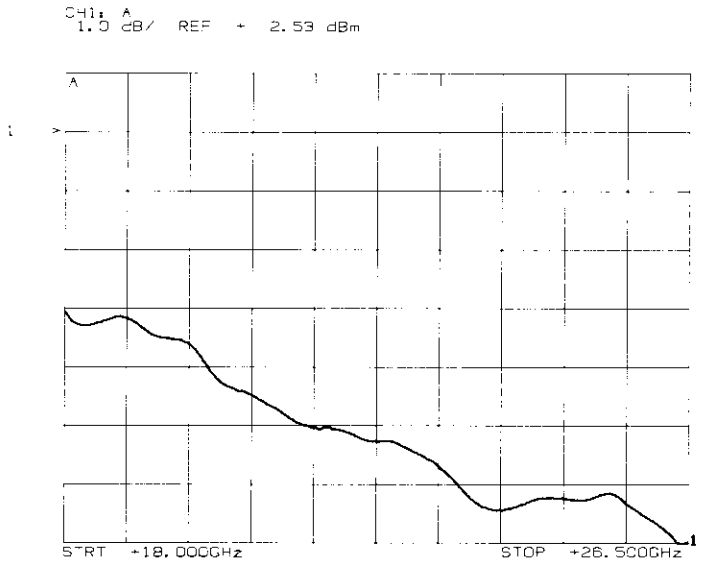


Figure 5-36. Trace Before Adjustments

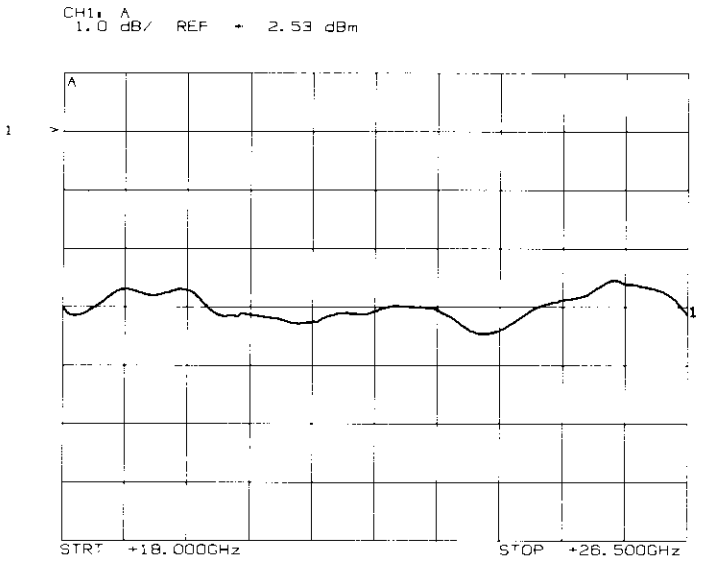


Figure 5-37. Trace After Main Slope Adjustment

5-14. Internal Leveled Flatness (Cont'd)

7. The adjustments affect the displayed output from left to right, with A5R34 (BP1) and A5R41 (SL1) having the greatest affect. The breakpoint and slope adjustments are done in pairs. A5R34 (BP1) and A5R41 (SL1) will be adjusted before continuing to A5R36 (BP2) and A5R42 (SL2) and so on.

8. Identify the breakpoint, refer to Figure 5-38. Adjust A5R34 (BP1) so that the adjustment point lies on the breakpoint (as closely as possible).

   Use the SCALE function of the scalar network analyzer to increase the displayed resolution if needed.

   Adjust A5R41 (SL1) to rotate the slope and bring it closer to a flatter display, refer to Figure 5-39. Iterate between A5R34 (BP1) and A5R41 (SL1) for the flattest display.

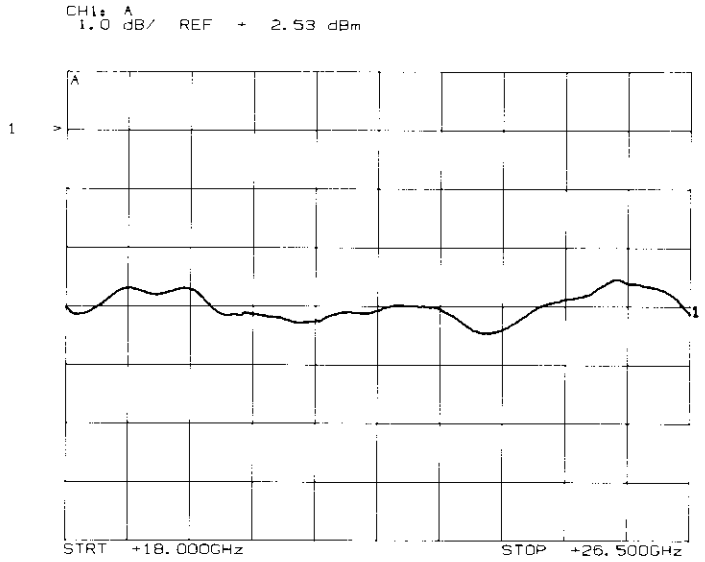


Figure 5-38. Identifying Breakpoint

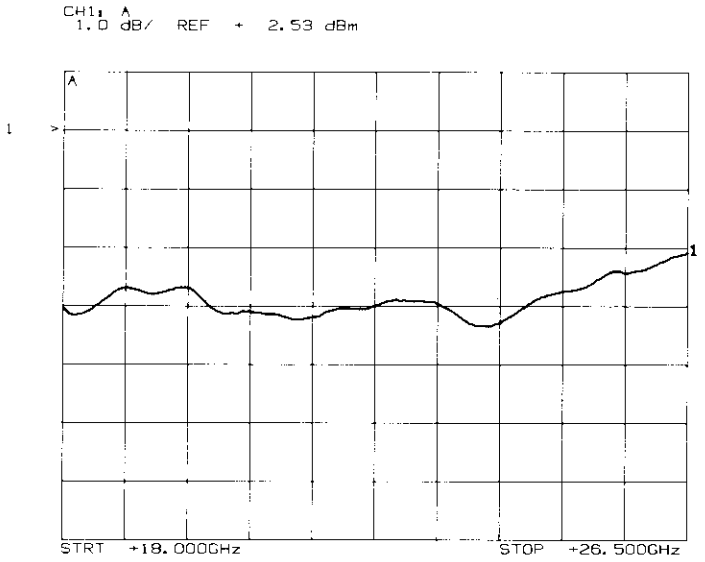


Figure 5-39. Trace After First Breakpoint and Slope Adjusted

5-14. Internal Leveled Flatness (Cont'd)

9. Repeat step 8 for the following adjustment pairs:

   A5R36 (BP2) and A5R42 (SL2)

   A5R38 (BP3) and A5R43 (SL3)

   A5R40 (BP4) and A5R44 (SL4)

   The final properly adjusted trace should be similar to Figure 5-40. If the trace is not adjusted properly, return to the preset conditions of the potentiometers. Do not attempt to begin readjustment from the middle of the procedure.

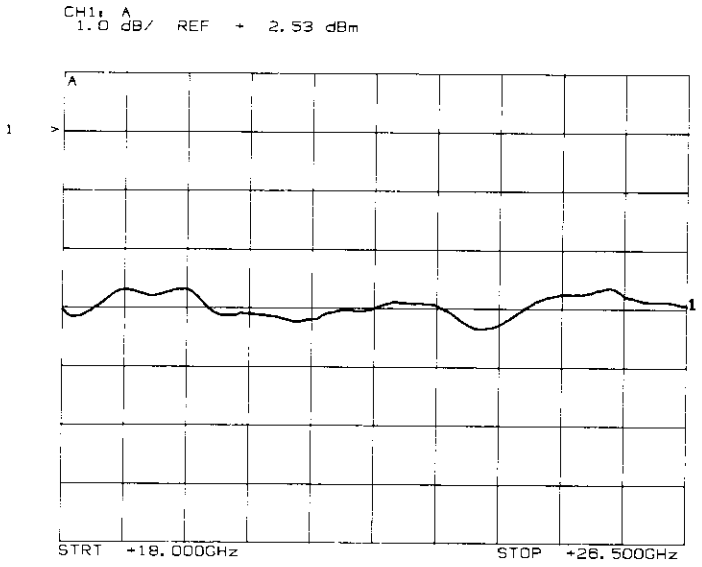


Figure 5-40. Properly Adjusted Power

5-15. Squarewave Symmetry Adjustment

NOTE: Complete adjustment of the ALC leveling loop requires several procedures to be performed in the order prescribed from paragraphs 5-12 and 5-16. Deviation from this routine may cause improper leveling and/or power variation problems.

Turn AC power OFF when removing or installing PC boards.

This procedure assumes that A3S1 is set to the factory-set position. Refer to Table 3-3 in the Operation Section of this manual.

DESCRIPTION

A4C23 (SYM 1) and A4R99 (SYM 2) minimize overshoot of the squarewave. A4R92 adjusts the duty cycle of the squarewave in bands 1-3.

EQUIPMENT

Sweep Oscillator Mainframe	HP 8350
Oscilloscope	HP 1741A
Crystal Detector	HP 8473C
Attenuator	HP 8493C Option 010
Adapter 3.5 (f) to 3.5 (f)	HP Part No. 1250-1749

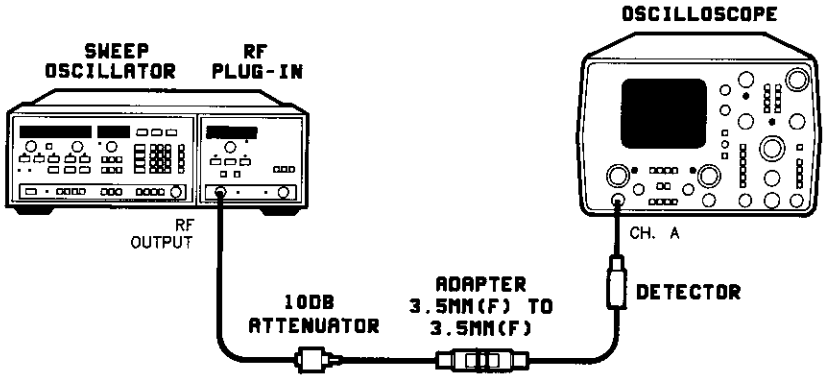


Figure 5-41. Squarewave Symmetry Adjustment Test Setup

PROCEDURE

1. Connect the equipment as shown in Figure 5-42, with A4 on an extender board. Allow one hour for warm-up.

5-15. Squarewave Symmetry Adjustment (Cont'd)

2. On the sweep oscillator/RF plug-in:

   Press **[INSTR PRESET] [CW] [⌐¬MOD]**

   Press **[POWER LEVEL] [0] [dBm]**

NOTE: Ensure that you do not overdrive the detector as this will distort the squarewave.

3. Set the oscilloscope controls as follows:

   Select MAIN SWEEP with 10us/DIV time

   Set channel A to .005V/DIV

   Set channel B to 1V/DIV.

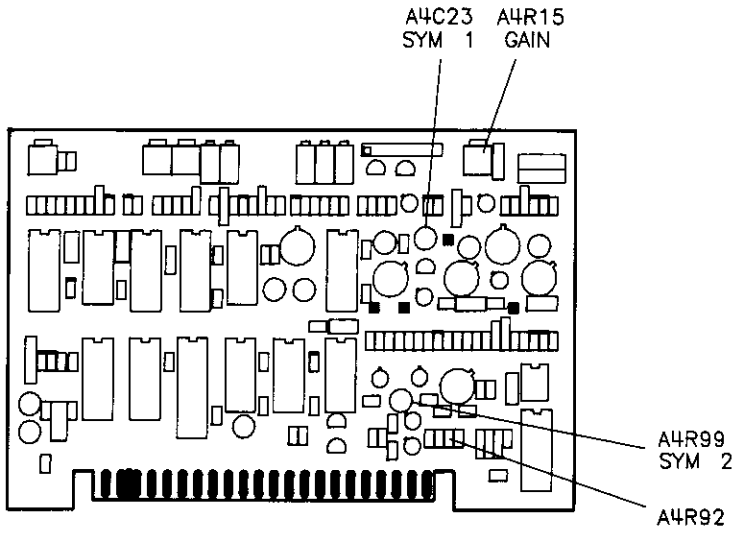


Figure 5-42. Squarewave Symmetry Adjustment Locations

4. Press **[CW] [1] [.] [5] [GHz]**

   Alternately adjust A4C23 (SYM 1) and A4R99 (SYM 2) for the waveform shown in Figure 5-43.

5. Press **[CW] [5] [GHz]**

   Check that the squarewave resembles that shown in Figure 5-43. If not, adjust A4C23 and A4R99 for best squarewave while alternately checking the squarewave at 1.5 GHz.

6. Repeat step 5 for 10, 15, and 26.5 GHz. Optimize the shape of the squarewave over the entire range of the plug-in. Pay particular attention to the changes between band 0 and bands 1, 2, 3, and 4. Naturally, there will be slight variations at each end of the plug-in's range.

5-15. SquareWave Symmetry Adjustment (Cont'd)

7. With the A4 board on an extender, there may be a slight "pip" on the detected signal. This will disappear when the board is mounted in the plug-in.

8. If you are unable to obtain the correct waveshape, you may need to adjust the value of A4R92. Replace A4R92 with a potentiometer having a mid-range value the same as that of A4R92. Vary its resistance until 50% duty cycle is obtained. Remove the potentiometer and measure its value. Replace with fixed resistor closest to the measured value.

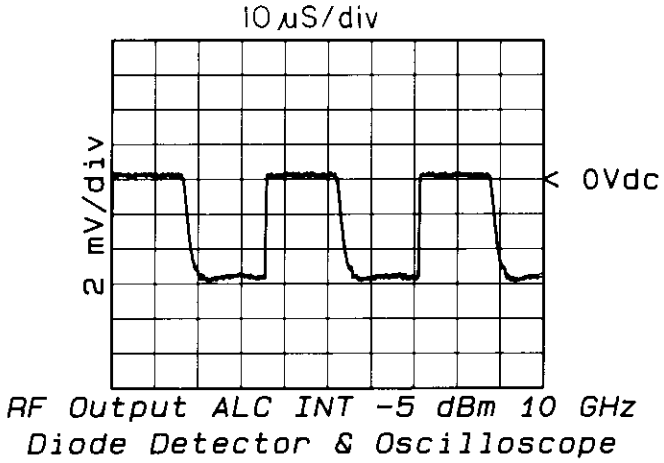


Figure 5-43. Optimum Squarewave

5-16. ALC Gain Adjustment

NOTE: Complete adjustment of the leveling loop requires several procedures to be performed in the order prescribed, from Adjustments 5-12 through 5-16. Deviation from this routine may cause improper leveling and/or flatness problems.

DESCRIPTION

A4R15 (GAIN) at the inverting input of A4U9, adjusts the gain of the main ALC amplifier. A4R15 (GAIN) is adjusted for maximum possible gain without producing ALC loop oscillations.

EQUIPMENT

Sweep Oscillator Mainframe	HP 8350
Oscilloscope	HP 1741A
Crystal Detector	HP 8473C
Function Generator	HP 3325A
Adapter 3.5 (f) to 3.5 (f)	HP Part No. 1250-1749
10 dB Attenuator	HP 8493C Option 010
50 Ohm Feedthru Termination	HP 10100C

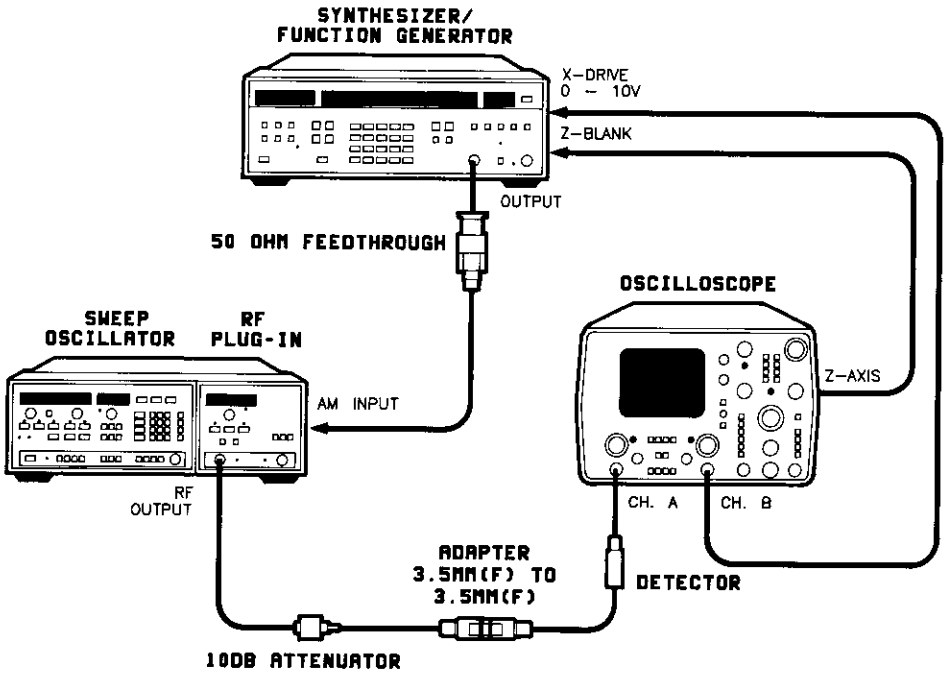


Figure 5-44. ALC Gain Adjustment Test Setup

5-16. ALC Gain Adjustment (Cont'd)

PROCEDURE

1. Connect equipment as shown in Figure 5-44. Allow 30 minutes for warm-up.
2. On the sweep oscillator/RF plug-in:

   Press **[INSTR PRESET] [CW]**.

   Press **[POWER LEVEL] [-] [2] [dBm]**.
3. Set the oscilloscope controls as follows:

   Select A vs.B mode to display a frequency versus amplitude plot.

   Set channel A for 0.05V/DIV, AC coupled

   Set channel B for 1 V/DIV, AC coupled

   Adjust horizontal position and Channel A vertical position controls for a stable display at mid-screen.
4. Set the function generator as follows:

START FREQUENCY	100 Hz
STOP FREQUENCY	300 kHz
START CONTINUE	ON
FUNCTION	SINE
AMPLITUDE	1V peak-to-peak
OFFSET	0
TIME	150 msec

5. Adjust the far left side of the modulated signal for 2 divisions peak- to-peak by using the CAL on the CHANNEL A knob. See Figure 5-45.

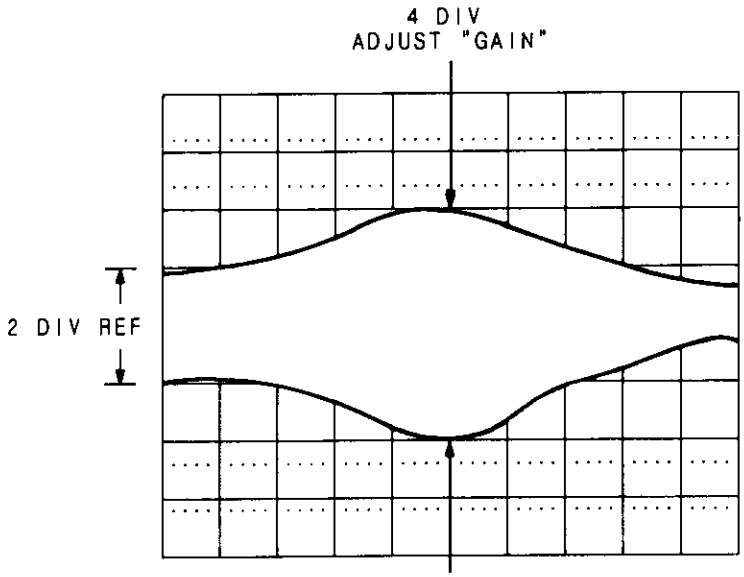


Figure 5-45. ALC Gain Adjusted Correctly (Worst Case)

5-16. ALC Gain Adjustment (Cont'd)

6. While monitoring Channel A, manually sweep the entire RF plug-in frequency range and adjust A4R15 (GAIN) for 4 divisions of peaking at the RF plug-in frequency where the highest gain peaking occurs. See Figure 5-45. Refer to Figure 5-46 for adjustment locations.

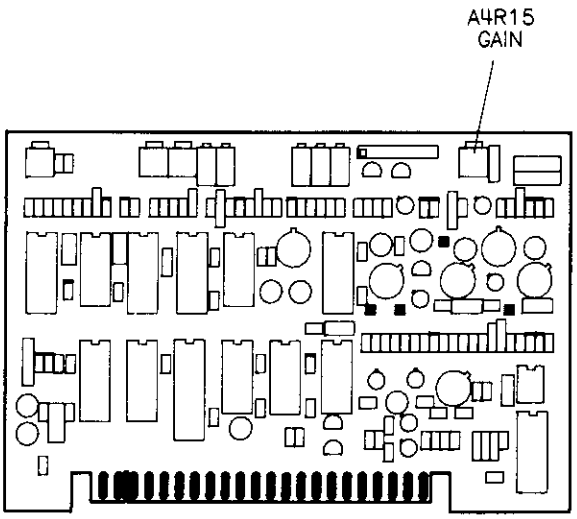


Figure 5-46. ALC Gain Adjustment Location

5-17. Power Sweep

DESCRIPTION

A 10 dB/sweep POWER SWEEP mode is selected and the resultant is displayed on the 8757A scalar network analyzer. Output of the power sweep circuit is adjusted for the correct sweep.

EQUIPMENT

Sweep Oscillator Mainframe	HP 8350
Scalar Network Analyzer	HP 8757A
Detector	HP 85025B
10 dB Attenuator	HP 8493C Option 010
Adapter 3.5 (f) to 3.5 (f)	HP Part No. 1250-1749

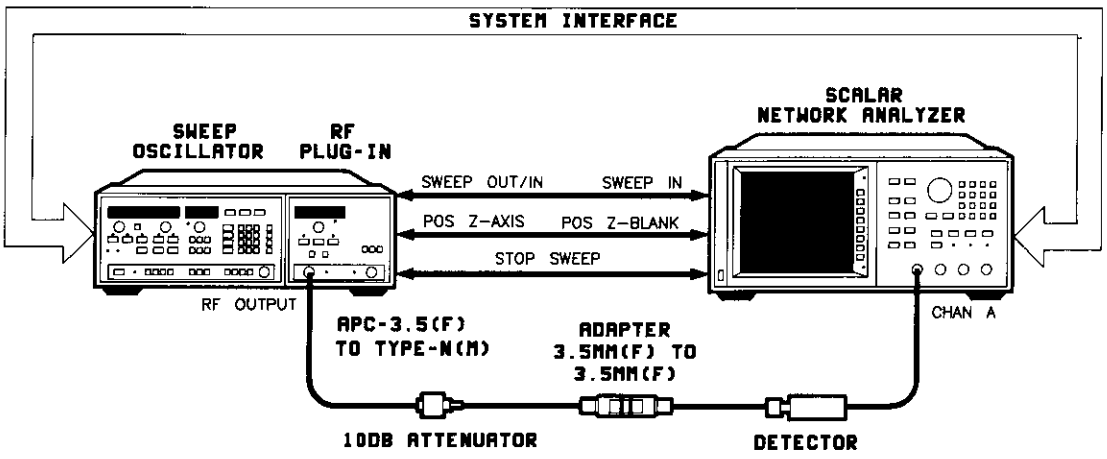


Figure 5-47. Power Sweep Adjustment Test Setup

PROCEDURE

1. Connect the equipment as shown in Figure 5-47. Allow 30 minutes for warm-up.

5-17. Power Sweep (Cont'd)

2. On the scalar network analyzer:

   Press **[PRESET]**. Select **[CHANNEL 2 OFF]**.

   Press **[SYSTEM]**. Select **[MODE DC]**.

   Select **[CAL] [DC DET ZERO] [MANUAL]**. Before completing the detector zero, turn the plug-in's RF output power off.

   Select **[CONT]**.

   Press **[REF]**, then select **[REF POSN]**. Adjust the trace with the rotary knob to the bottom horizontal graticule.

3. On the sweep oscillator/RF plug-in:

   Press **[SHIFT] [CW] [POWER LEVEL] [0] [dB]**.

4. On the scalar network analyzer:

   Press **[SCALE] [5] [dB]**

   Press **[REF]**, then select **[REF LEVEL]**.

   Adjust the trace with the rotary knob to one division below the center horizontal graticule.

5. On the sweep oscillator/RF plug-in:

   Press **[POWER SWEEP] [1] [0] [dB]**.

6. While observing the scalar network analyzer display of the POWER SWEEP output, adjust A5R50 (PWSP) (See Figure 5-48 for adjustment location) for 10 dB/sweep (two major divisions). Refer to Figure 5-49 for properly adjusted power sweep.

5-17. Power Sweep (Cont'd)

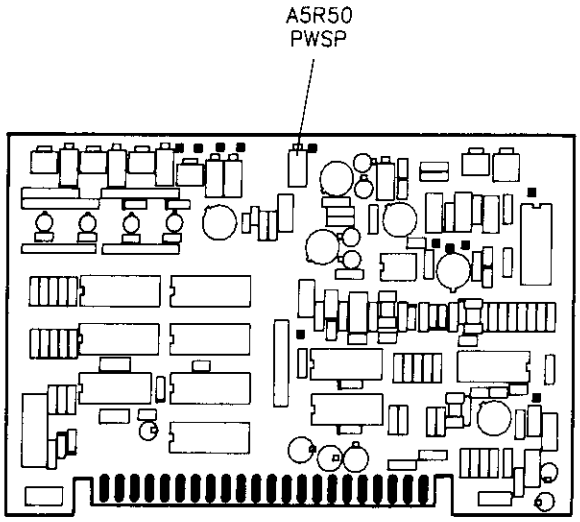


Figure 5-48. Power Sweep Adjustment Location

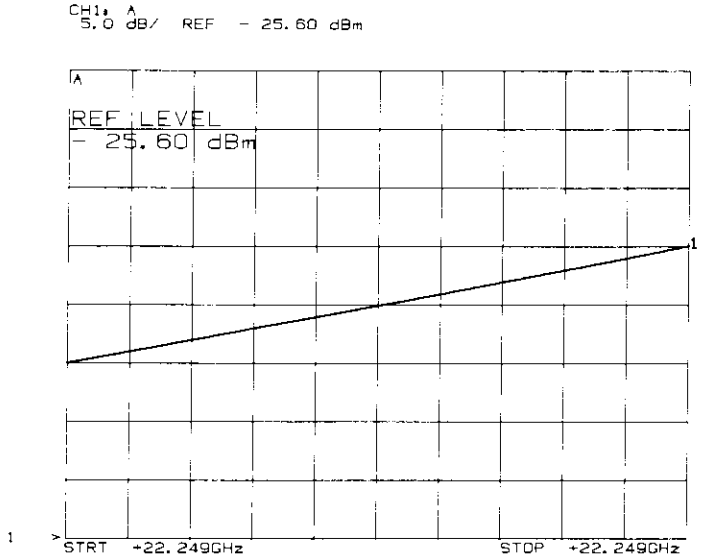


Figure 5-49. Power Sweep After Adjustment

5-18. FM Driver

DESCRIPTION

The FM driver high frequency offset is adjusted for a zero volt drive with no FM applied. A delay-line discriminator is used to detect and display FM on an oscilloscope. Adjustments are made for best overall frequency response from 100 Hz to 10 MHz. Compliance to a specification of ±3 dB is checked between 100 Hz and 2 MHz.

EQUIPMENT

Sweep Oscillator Mainframe	HP 8350
Digital Voltmeter	HP 3456A
Oscilloscope	HP 1741A
Function Generator	HP 3325A
Delay Line Descriminator	Refer to Figure 1-3 (General Information)
Frequency Counter	HP 5343A
50 Ohm Feedthru Termination	HP 10100C

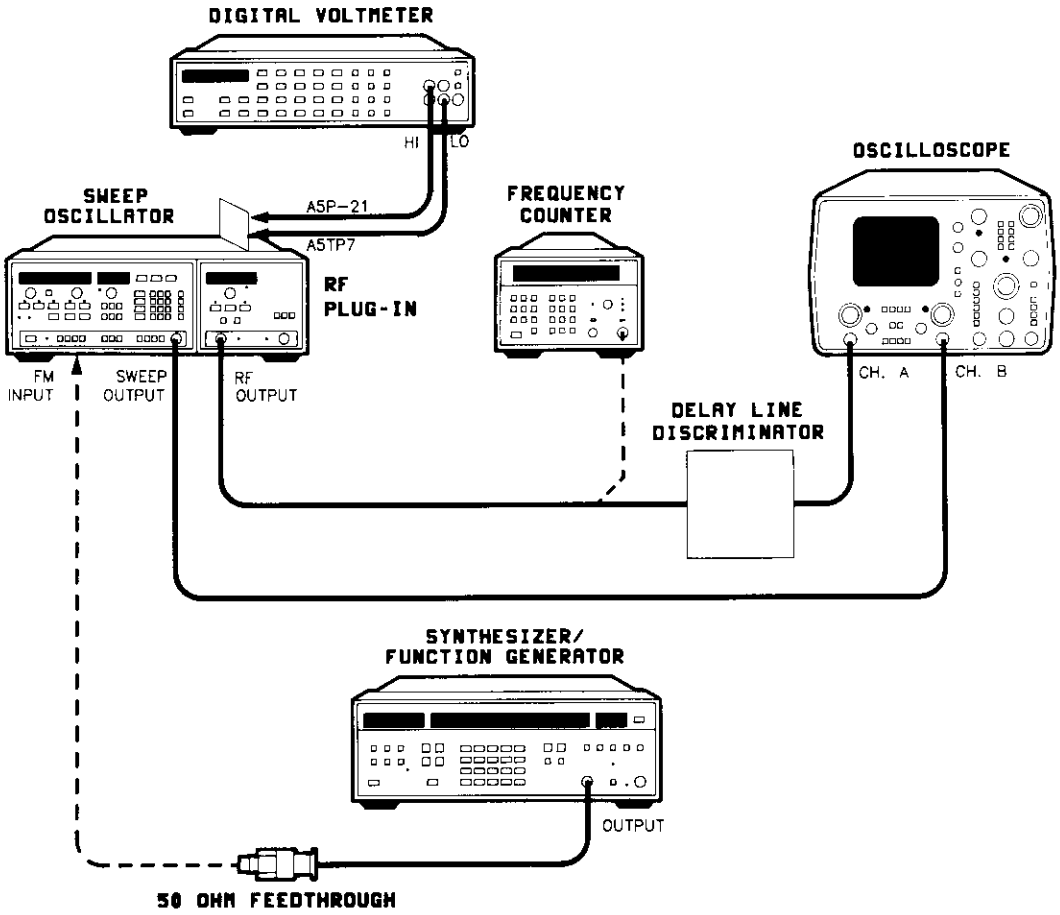


Figure 5-50. FM Adjustment Test Setup

5-18. FM Driver (Cont'd)

PROCEDURE

CAUTION

Turn off AC power when removing or installing PC boards.

1. The equipment in Figure 5-50 will be configured in the following procedure. In the interim, allow 30 minutes for warm-up for each instrument.

FM Offset

2. Turn the HP 8350 AC power off and place the RF plug-in A5 FM driver assembly on extender board.
3. Turn the HP 8350 AC power on and connect DVM HI to A5 board connector pin 21 and DVM LO to A5TP7 (Ground). Adjust A5R19 (FM OFFSET) for 0.00 ± 0.0001V. Refer to Figure 5-51.
4. Turn the HP 8350 AC power off and disconnect the DVM from test points. Remove the extender board, and reinstall the A5 FM driver board in the instrument.
5. On the sweep oscillator/RF plug-in:

   Turn AC power on.

   Press **[SHIFT] [CW] [1] [0] [GHz]**

   Press **[VERNIER]** to on

   Press **[INT]** ALC MODE

   Press **[RF BLANK]** to on

   Press **[CW] [FILTER]** to off

   Set the RF output power to any leveled power.

6. Set the oscilloscope as follows:

MODE	A vs.B
CHAN A	
INPUT	50 Ω
VOLTS/DIV	0.005
CHAN B	
INPUT	DC
VOLTS/DIV	1

5-18. FM Driver (Cont'd)

7. Set the function generator as follows:

FREQUENCY	10 MHz
FUNCTION	SINE
AMPLITUDE	Adjust the amplitude for a 100 mV peak-to-peak display on the oscilloscope screen.

Flatness

8. Connect the frequency counter to the RF plug-in RF output. Apply +1V DC to the rear panel FM INPUT with the function generator. A shift in frequency of approximately −20 MHz should occur on the frequency counter. This displays a correct FM sensitivity. If a frequency shift of −6 MHz is indicated, reset switch 5 on A3S1 to 0. Refer to Table 3-3 in the Operation Section of this manual for switch configuration information.

9. Connect the equipment as shown in Figure 5-50 with the delay line descriminator connected to the RF output and the function generator connected to the rear panel FM INPUT connector.

10. Set ground reference on the oscilloscope to center line. Adjust the sweep oscillator CW FREQUENCY and CW VERNIER for a waveform at the center of the oscilloscope CRT.

11. Adjust Channel A CAL (sensitivity) for a trace 4 divisions peak-to-peak, centered on the screen. (This sets up a 100% amplitude reference.)

12. Sweep the function generator frequency from 100 Hz to 100 kHz. Select resistor A5R31 (See Figure 5-51) so the amplitude at 100 Hz and at 100 kHz are the same ±0.2 divisions on the screen.

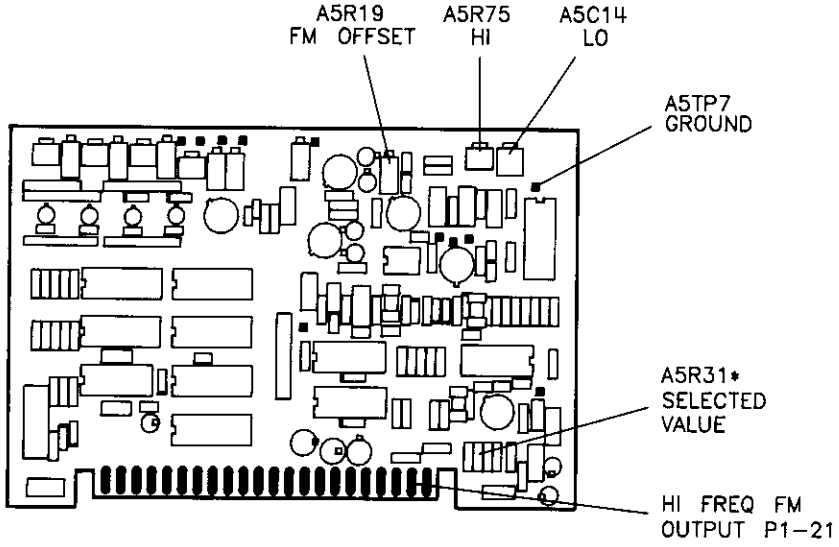


Figure 5-51. FM Driver Adjustment Location

5-18. FM Driver (Cont'd)

13. Sweep the function generator frequency from 100 Hz to 10 MHz. Iterate between adjustments A5C14 (LO) and A5R75 (HI) to obtain the most constant overall response from 100 Hz to 10 MHz.

14. Check that the ±3 dB flatness specification is met between 100 Hz and 2 MHz as follows. Sweep the function generator frequency between 100 Hz and 2 MHz. On the oscilloscope, note the maximum point (+3.0 dB) can be up to 5.6 divisions, and the minimum point (−3.0 dB) which can be down to 2.8 divisions. Refer to Figure 5-52.

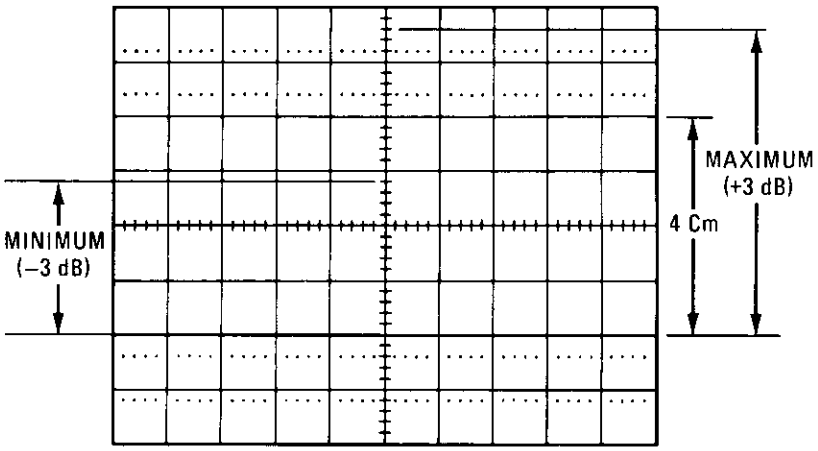


Figure 5-52. Flatness Response

15. If the flatness response in step 14 is not met, repeat steps 12 and 13 and make compromise adjustments in the 100 Hz to 2 MHz range to meet the flatness requirements.

Section 6. Replaceable Parts

INTRODUCTION

This section contains information for ordering parts. Table 6-1 lists the assemblies that are available for exchange or are under two-year warranty. Table 6-2 lists abbreviations used in the parts list and the names and addresses that correspond to the manufacturer's code numbers. Table 6-3 lists all replaceable parts in reference designator order.

TWO-YEAR WARRANTY AND RESTORED EXCHANGE PARTS

A two-year warranty applies to both an original component and to one that is purchased as a replacement part either new or restored through the support life of the instrument. The restored exchange parts program allows a defective component to be exchanged for a factory-restored part that provides a substantial reduction in replacement cost. In addition, if the original component is covered by a two-year warranty, the exchanged component will also have a two-year warranty from the date of purchase. Table 6-1 identifies the components within the instrument that have a two-year warranty as well as those that are available as restored exchange parts.

ABBREVIATIONS

Table 6-2 contains three major sections:

- Reference Designations explain the designators used in the parts list.
- Abbreviations define all abbreviations used in the descriptions of replaceable parts.
- Manufacturer's Code List references the name and address of a typical manufacturer with the code number provided in the parts list.

REPLACEABLE PARTS LIST

Table 6-3 is the list of replaceable parts and is organized as follows:

- Electrical assemblies and their components in alpha-numerical order by reference designation and option.
- Chassis-mounted parts in alpha-numerical order by reference designation and option.
- Miscellaneous parts.

The information given for each part consists of the following:

a. The Hewlett-Packard part number.

b. Part number check digit (CD).

c. The total quantity (Qty) in the instrument.

d. The description of the part.

e. A typical manufacturer of the part in a five-digit code.

f. The manufacturer's number for the part.

The total quantity for each part is given only once — at the first appearance of the part number in the list.

NOTE: Total quantities for optional assemblies are totaled by assembly and not integrated into the standard list.

ILLUSTRATIONS

Figures 6-1 (1 through 4) and 6-2 (1 through 3), Replaceable Parts, provide the location of front and back panel and exterior frame replaceable mechanical parts. These parts are numbered for reference and are listed in a table below each figure.

ORDERING INFORMATION

To order a part listed in the Replaceable Parts List, quote the Hewlett-Packard part number with its check digit (CD), indicate the quantity, and address the order to the nearest Hewlett-Packard office. The check digit will ensure accurate and timely processing of your order.

To order a part that is not listed in the Replaceable Parts List, include the instrument model number, instrument serial number, description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

SPARE PARTS KIT

Stocking spare parts for an instrument is often done to ensure quick return to service after a malfunction occurs. Hewlett-Packard has a "Spare Parts Kit" available for this purpose. The kit consists of selected replaceable assemblies and components for this instrument. The contents of the kit and the "Recommended Spares" list for this instrument may be obtained on request and the "Spares Parts Kit" may be ordered through your nearest Hewlett-Packard office.

Table 6-1. Two Year Warranty and Restored Exchange Parts

Reference Designation	Description	Two-Year Warranty	Restored Exchange Part
A12	Switched YTM	Yes	Yes
A13	YO 2.3 to 7.0 GHz	Yes	Yes
A14	2 to 7 GHz Power Amp	Yes	Yes
A16	Mod/Splitter	Yes	Yes
A17	0.01 to 2.4 GHz Amp	Yes	Yes
A18	Modulator Mixer	Yes	Yes
DC1	Detector	Yes	No

Table 6-2. Reference Designations, Abbreviations, and Manufacturer's Code List (1 of 3)

REFERENCE DESIGNATIONS

A . . . . . Assembly
AT . . . . . Attenuator, Isolator, Limiter, Termination
B . . . . . Fan, Motor
C . . . . . Capacitor
CP . . . . . Coupler
CR . . . . . Diode, Diode Thyristor, Step Recovery Diode (SCR), Varactor
DC . . . . . Directional Coupler
DS . . . . . Annunciator, Lamp, Light Emitting Diode (LED), Signaling Device (Audible or Visible)
E . . . . Miscellaneous Electrical Part
F . . . . . Fuse
FL . . . . . Filter
H . . . . . Hardware
J . . . . . Electrical Connector (Stationary Portion), Jack
K . . . . . Relay
L . . . . . Coil, Inductor
M . . . . . Meter
MP . . . . . Miscellaneous Mechanical Part
P . . . . . Electrical Connector (Movable Portion), Plug
Q . . . . . Silicon Controlled Rectifier (SCR), Transistor, Triode Thyristor
R . . . . . Resistor
RT . . . . . Thermistor
S . . . . . Switch
T . . . . . Transformer
TB . . . . . Terminal Board
TP . . . . . Test Point
U . . . . . Integrated Circuit, Microcircuit
V . . . . . Electron Tube
VR . . . . . Breakdown Diode (Zener), Voltage Regulator
W . . . . . Cable, Transmission Path, Wire
X . . . . . Socket
Y . . . . . Crystal Unit (Piezoelectric, Quartz)
Z . . . . . Tuned Cavity, Tuned Circuit

ABBREVIATIONS

A

A . . . . . Across Flats, Acrylic, Air (Dry Method), Ampere
ADJ . . . . . Adjust, Adjustment
AL . . . . . Aluminum
ALC . . . . . Alcohol, Automatic Level Control
AMP . . . . . Amperage
AMPL . . . . . Amplifier
ANDZ . . . . . Anodized
ANLG . . . . . Analog
ASSY . . . . . Assembly
ASTBL . . . . . Astable
ATTEN . . . . . Attenuation, Attenuator
AWG . . . . . American Wire Gauge

B

BCKT . . . . . Bracket
BD . . . . . Board, Bundle
BE . . . . . Baume, Beryllium
BFR . . . . . Before, Buffer
BLK . . . . . Black, Blank, Block
BNC . . . . . Type of Connector
BSC . . . . . Basic
BVR . . . . . Reverse, Breakdown Voltage

C

C . . . . . Capacitance, Capacitor, Center Tapped, Centistoke, Ceramic, Cermet, Circular Mil Foot, Closed Cup, Cold, Compression
CBL . . . . . Cable
CER . . . . . Ceramic
CH . . . . . Center Hole
CHAM . . . . . Chamfer
CHAN . . . . . Channel
COAX . . . . . Coaxial
COM . . . . . Commercial, Common
CONN . . . . . Connect, Connection, Connector
CONT . . . . . Contact, Continuous, Control, Controller
CONV . . . . . Converter
CP . . . . . Cadmium Plate, Candle Power, Centipoise, Conductive Plastic, Cone Point
CRP . . . . . Crepe, Crimp
CTR . . . . . Center
CURRNT . . . . . Current

D

D . . . . . Deep, Depletion, Depth, Diameter, Direct Current
D/A . . . . . Digital-to-Analog
DAP . . . . . Diallyl Phthalate
DB . . . . . Decibel, Double Break
DC . . . . . Direct Current, Double Contact
DBL . . . . . Double
DCDR . . . . . Decoder
DEG . . . . . Degree
DIA . . . . . Diameter
DIFF . . . . . Differential
DIP . . . . . Dual In-Line Package
DO . . . . Package Type Designation
DRVR . . . . . Driver

E

E . . . . . Enamel (Insulation, Enhancement, Extension)
E-MODE . . . . . Enhancement Mode
EPROM . . . . . Eraseable Programmable Read Only Memory
EXCL . . . . . Excluding, Exclusive
EXT . . . . . Extended, Extension, External, Extinguish

F

F . . . . . Fahrenheit, Farad, Female, Film, (Resistor), Fixed, Flange, Flint, Flourine, Frequency
FDTHRU . . . . . Feed Through
FEM . . . . . Female
FF . . . . . Flange, Female Connection; Flip Flop
FL . . . . . Flash, Flat, Fluid
FLEX . . . . . Flexible
FLG . . . . . Flange
FLTR . . . . . Filter, Floater
FT . . . . . Current Gain Bandwidth
FM . . . . . Flange, Male Connection; Foam, Frequency Modulation Product (Transition Frequency); Feet, Foot
FXD . . . . . Fixed

G

GEN . . . . . General, Generator
GHZ . . . . . Gigahertz
GP . . . . . General Purpose Group
GL . . . . . Glass
GRN . . . . . Green
GRV . . . . . Grooved

Table 6-2. Reference Designations, Abbreviations, and Manufacturer's Code List (2 of 3)

H

H . . . . . Henry, Hermaphrodite, High, Hole Diameter, Hot, Hub Inside Diameter, Hydrogen
HD . . . . . Hand, Hard, Head, Heavy Duty
HEX . . . . . Hexadecimal, Hexagon, Hexagonal
HGT . . . . . Height

I

IC . . . . . Collector Current, Integrated Circuit
ID . . . . . Identification, Inside Diameter
IF . . . . . Forward Current, Intermediate Frequency
IMPD . . . . . Impedance
IN . . . . . Inch, Indium
INP . . . . . Input
INS . . . . . Insert, Inside, Insulation, Insulator
INT . . . . . Integral, Intensity, Internal
INTL . . . . . Internal, International
INV . . . . . Invert, Inverter

J

JFET . . . . . Effect Transistor

K

K . . . . . Kelvin, Key, Kilo, Potassium
KB . . . . . Knob

L

LED . . . . . Light Emitting Diode
LG . . . . . Length, Long
LIN . . . . . Linear, Linear Taper, Linearity
LK . . . . . Link, Lock
LKG . . . . . Leakage, Locking
LKWR . . . . . Lockwasher
LS . . . . . Loudspeaker, Low Power Schottky, Series Inductance
LUM . . . . . Luminous

M

M . . . . . Male, Maximum, Mega, Mil, Milli, Mode, Momentary, Mounting Hole Centers, Mounting Hole Diameter
MA . . . . . Milliampere
MACH . . . . . Machined
MAX . . . . . Maximum
MCD . . . . . Millacandela
MICPROC . . . . . Microprocessor
MIN . . . . . Miniature, Minimum, Minor, Minute
MLD . . . . . Mold, Molded
MM . . . . . Magnetized Material (Restricted Articles Code), Millimeter
MO . . . . . Metal Oxide, Milliounce, Molybdenum
MOD . . . . . Model, Modified Modular, Modulated, Modulator
MOM . . . . . Momentary, Motherboard
MTG . . . . . Mounting
MTLC . . . . . Metallic
MTR . . . . . Meter
MULTIPLXR . . . . . Multiplexer
MULTR . . . . . Multiplier
MUW . . . . . Music Wire
MW . . . . . Milliwatt

N

N-CHAN . . . . . N-Channel Metal Oxide Semiconductor
NB . . . . . Niobium
NCH . . . . . Notched
NEG . . . . . Negative
NH . . . . . Nanohenry
NM . . . . . Nanometer, Nonmetallic
NO . . . . . Normally Open, Number
NPN . . . . . Negative Positive Negative (Transistor)
NS . . . . . Nanosecond, Non-Shorting, Nose
NYL . . . . . Nylon (Polyamide)

O

OCTL . . . . . Octal
OD . . . . . Olive Drab, Outside Diameter
OP . . . . . Operational
OPT . . . . . Optical, Option, Optional
OXD . . . . . Oxide

P

PAN-HD . . . . . Pan Head
PC . . . . . Picocoulomb, Piece, Printed Circuit
P.C. . . . . Printed Circuit
PCB . . . . . Printed Circuit Board
PD . . . . . Pad, Palladium, Pitch Diameter, Power Dissipation
PF . . . . . Picofarad; Pipe, Female Connection; Power Factor
PKG . . . . . Package
PL . . . . . Phase Lock, Plain, Plate, Plug
PL-MTG . . . . . Plate Mounting
PLSTC . . . . . Plastic
PN . . . . . Part Number
PNP . . . . . Positive Negative Positive (Transistor)
POLYC . . . . . Polycarbonate
POLYE . . . . . Polyester
POLYI . . . . . Polyimide
POS . . . . . Position, Positive
POZI . . . . . Pozidrive Recess
PRCN . . . . . Precision
PRIM . . . . . Primary
PRL . . . . . Parallel
PRP . . . . . Purple, Purpose
P/S . . . . . Power Supply
PT . . . . . Part, Pint, Platinum, Point, Pulse Time
PVC . . . . . Polyvinyl Chloride
PW . . . . . Power Wirewound, Pulse Width

Q

QUAD . . . . . Set of Four

R

RBN . . . . . Ribbon
RCVR . . . . . Receiver
RECT . . . . Rectangle, Rectangular, Rectifier
RES . . . . . Research, Resistance, Resistor, Resolution
RET . . . . . Retaining
RF . . . . . Radio Frequency
RFI . . . . . Radio Frequency Interference
RFLTR . . . . . Regulator
RKR . . . . . Rocker
RND . . . . . Round
RPG . . . . . Rotary Pulse Generator
RR . . . . . Rear
RVT . . . . . Rivet, Riveted

S

SCR . . . . . Screw, Scrub, Silicon Controlled Rectifier
SEC . . . . . Secondary
SER . . . . . Serial, Series
SGL . . . . . Single
SHFT . . . . . Shaft
SHLDR . . . . . Shoulder
SI . . . . . Silicon, Square Inch
SIG . . . . . Signal, Significant
SIP . . . . . Single In-Line Package
SKT . . . . . Skirt, Socket
SLDR . . . . . Solder
SM . . . . . Samarium, Seam, Small, Square Meter, Sub Modular, Subminiature
SMB . . . . . Subminiature, B Type (Snap-On Connector)

Table 6-2. Reference Designations, Abbreviations , and Manufacturer's Code List (3 of 3)

SNP . . . . . Snap
SPCL . . . . . Special
SQ . . . . . Square
SST . . . . . Stainless Steel
STDF . . . . . Standoff
SZ . . . . . Size

T

T . . . . . Tab Width, Taper, Teeth, Temperature, Tera, Tesla, Thermoplastic (Insulation), Thickness, Time, Timed, Tooth, Turns Ratio, Typical
TA . . . . . Ambient Temperature, Tantalum
TC . . . . . Thermoplastic
TFE . . . . . Polytetrafluro - ethylene, Teflon
THD . . . . . Thread, Threaded
THK . . . . . Thick
TO . . . . . Package Type
TPL . . . . . Triple
TRIG . . . . . Trigger, Triggerable, Triggering, Trigonometry
TRMR . . . . . Trimmer
TRN . . . . . Turn, Turns
TTL . . . . . Tan Translucent, Transistor, Transistor Logic

U

UCD . . . . . Microcandela
UNCT . . . . . Undercut
UF . . . . . Microfarad

V

V . . . . . Vanadium, Variable, Violet, Volt, Voltage
VA . . . . . Volt Ampere
VDC . . . . . Volts, Direct Current
VID . . . . . Video

W

W . . . . . Watt, Wattage, White,
WB . . . . . Wide Band Wide, Width, Wire
WD . . . . . Width, Wood

X

XSTR . . . . . Transistor

Y

YIG . . . . . Yytrium-iron-garnet
YTM . . . . . YIG Tuned Multiplier

Z

ZN-P . . . . . Zinc Plate
ZNR . . . . . Zener

MANUFACTURER'S CODE LIST

Mfr Code	Manufacturer Name	Address		Zip Code
00000	Any Satisfactory Supplier			
00779	AMP Inc	Harrisburg	PA	17111
01121	Allen-Bradley Co Inc	El Paso	TX	79935
01295	Texas Instruments Inc	Dallas	TX	75265
01417	Chrysler Corp Defense Opn Div	Detroit	MI	48203
01287	Coates & Clark Inc	New York	NY	10022
03888	K D I Pyrofilm Corp	Whippany	NJ	07981
04713	Motorola Inc Semi-Cond Prod	Phoenix	AX	85008
06665	Precision Monolithics Inc	Santa Clara	CA	95050
07263	Fairchild Corp	Mountain View	CA	94042
11236	CTS Corp Berne Div	Berne	IN	46711
13606	Sprague Electric Semicon Div	Concord	NH	03301
15818	Teledyne Semiconductor	Mountain View	CA	94043
17856	Siliconix Inc	Santa Clara	CA	95054
18324	Signetics Corp	Sunnyvale	CA	94086
19701	Mepco/Centralab Inc	West Palm Beach	FL	33407
24355	Analog Devices Inc	Norwood	MA	02062
24546	Corning Electronics	Santa Clara	CA	95050
25088	Siemens Corp	Iselin	NJ	08830
27014	National Semiconductor Corp	Santa Clara	CA	95052
28480	Hewlett-Packard Co Corporate HQ	Palo Alto	CA	94304
3L585	RCA Corp Solid State Div	Somerville	NJ	
34371	Harris Corp	Melbourne	FL	32901
34649	Intel Corp	Santa Clara	CA	95054
56289	Sprague Electric Co	North Adams	MA	01247
72136	Electro Motive Corp	Florence	SC	06226
73138	Beckman Industrial Corp	Fullerton	CA	92632
9N171	Unitrode Corp	Lexington	MA	02173
91506	Augat Inc	Mansfield	MA	02048
91637	Dale Electronics Inc	El Paso	TX	79936

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	**83592-60008**	**9**	**1**	**BOARD ASSEMBLY-FRONT PANEL (DOES NOT INCLUDE RPG)**	**28480**	**83592-60008**
A1C1	0160-4084	8	26	CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A1C2	0180-2811	7	1	CAPACITOR-FXD 10UF±20% 35VDC TA	28480	0180-2811
A1C3	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A1C4	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A1C5	0180-0552	9	1	CAPACITOR-FXD 220UF±20% 10VDC TA	28480	0180-0552
A1DS2	1990-0487	7	2	LED-LAMP LUM-INT=2MCD BVR=5V	28480	HLMP-1401
A1DS3	1990-0487	7		LED-LAMP LUM-INT=2MCD BVR=5V	28480	HLMP-1401
A1DS4	1990-0670	0	5	LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0670
A1DS5	1990-0670	0		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0670
A1DS6	1990-0486	6	1	LED-LAMP LUM-INT=2MCD IF=25MA-MAX BVR=5V	28480	HLMP-1301
A1DS14	1990-0670	0		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0670
A1DS15	1990-0670	0		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0670
A1DS16	1990-0670	0		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0670
A1DS17	1990-0699	3	3	LED-LIGHT BAR MODULE LUM-INT=7MCD	28480	1LM1-2350
A1DS18	1990-0699	3		LED-LIGHT BAR MODULE LUM-INT=7MCD	28480	1LM1-2350
A1DS19	1990-0699	3		LED-LIGHT BAR MODULE LUM-INT=7MCD	28480	1LM1-2350
A1J1	1251-4827	1	1	CONNECTOR 50-PIN M POST TYPE	28480	1251-4827
A1MP1				NOT ASSIGNED		
A1MP3	0380-1233	9	3	SPACER-SPECIALTY .450 IN LG; .175 IN OD	00000	ORDER BY DESCRIPTION
A1MP4	2190-0067	4	2	WASHER-LK INTL T 1/4 IN .256-IN-ID	28480	2190-0067
A1MP5	2950-0006	3	2	NUT-HEX-DBL-CHAM 1/4-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
A1MP6	7121-1153	1	3	LABEL-INFORMATION .14-IN-WD .4-IN-LG	28480	7121-1153
A1MP7	3050-0381	0	2	WASHER-FL NM 1/4 IN .266 IN-ID	28480	3050-0381
A1R2	0698-3444	1	1	RESISTOR 316 1% .125W F TC=0±100	24546	CT4-1/8-T0-316R-F
A1R3	2100-4022	0	2	RESISTOR-VAR CONTROL CP 10K 10% LIN	28480	2100-4022
A1R4	2100-4022	0		RESISTOR-VAR CONTROL CP 10K 10% LIN	28480	2100-4022
A1R6	0698-8820	7	1	RESISTOR 4.64 1% .125W F TC=0±100	28480	0698-8820
A1R7	0757-0398	4	4	RESISTOR 75 1% .125W F TC=0±100	24546	CT4-1/8-T0-75R0-F
A1R8	0757-0398	4		RESISTOR 75 1% .125W F TC=0±100	24546	CT4-1/8-T0-75R0-F
A1R9	0757-0398	4		RESISTOR 75 1% .125W F TC=0±100	24546	CT4-1/8-T0-75R0-F
A1RPG1	0960-0683	1	1	ROTARY PULSE GENERATOR INPUT POWER; 5VDC	28480	0960-0683
A1S1	5060-9436	7	8	PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S2	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S3	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S4	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S5	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S12	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S13	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S14	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1U1	1810-0124	9	1	NETWORK-RES 16-DIP 200.0 OHM X 8	28480	1810-0124
A1U2	1990-0738	1	1	DISPLAY-NUM-SEG 5-CHAR .152-H RED	28480	1990-0738
A1U3	1810-0403	7	1	NETWORK-RESISTOR R1-R15: 330 OHM±2%	01121	316A331
A1XU2	1251-5928	5	1	CONNECTOR 15-PIN M POST TYPE	28480	1251-5928
A1XU9	1200-0901	7	3	SOCKET-STRP 8-CONT SIP DIP-SLDR	28480	1200-0901
A1XU10	1200-0901	7		SOCKET-STRP 8-CONT SIP DIP-SLDR	28480	1200-0901
A1XU11	1200-0901	7		SOCKET-STRP 8-CONT SIP DIP-SLDR	28480	1200-0901

See introduction to this section for ordering information.

*Indicates factory selected value.

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2	**83590-60122**	**6**	**1**	**BOARD ASSEMBLY-FRONT PANEL INTERFACE**	**28480**	**83590-60122**
A2C1	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A2C2	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A2C3	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A2C5	0160-0174	9	1	CAPACITOR-FXD .47UF +80-20% 50VDC CER	28480	0160-0174
A2C6	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A2C7	0160-3879	7	30	CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A2C8	0160-3875	3	1	CAPACITOR-FXD 22PF ±5% 200VDC CER 0±30	28480	0160-3875
A2C9	0160-4808	4	1	CAPACITOR-FXD 470PF ±5% 100VDC CER	28480	0160-4808
A2CR1	1901-0033	2	18	DIODE-GEN PRP 180V 200MA DO-35	9N171	1N645
A2CR2	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-35	9N171	1N645
A2CR3	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-35	9N171	1N645
A2CR6	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-35	9N171	1N645
A2CR7	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-35	9N171	1N645
A2J1	1251-5926	3	3	CONNECTOR 50-PIN M POST TYPE	28480	1251-5926
A2J3	1200-1204	5	1	SOCKET-IC 14-CONT DIP DIP-SLDR	01417	2-641609-2
A2K1	0490-0916	6	3	RELAY-REED 1A 500MA 100VDC 5VDC-COIL	28480	0490-0916
A2L1	9100-1618	1	1	INDUCTOR RF-CH-MLD 5.6UH 10%	28480	9100-1618
A2MP1				NOT ASSIGNED		
A2MP2	0380-0773	0	4	SPACER-RVT-ON .5-IN-LG .152-IN-ID	28480	0380-0773
A2MP3	7121-2679	8	1	LABEL-INFORMATION .14-IN-WD .4-IN-LG	28480	7121-2679
A2P1	1251-5491	7	2	CONNECTOR 25-PIN F POST TYPE	28480	1251-5491
A2Q1	1854-0474	4	2	TRANSISTOR NPN SI PD=310MW FT=100MHZ	04713	2N5551
A2Q2	1853-0316	1	3	TRANSISTOR-DUAL PNP PD=500MW	28480	1853-0316
A2Q3	1854-0474	4		TRANSISTOR NPN SI PD=310MW FT=100MHZ	04713	2N5551
A2Q4	1854-0477	7	3	TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
A2R1	2100-3103	6	1	RESISTOR-TRMR 10K 10% C SIDE-ADJ 17-TRN	73138	89PR10K
A2R2	0698-7268	5	2	RESISTOR 21.5K 1% .05W F TC=0±100	24546	C3-1/8-T0-2152-F
A2R3	0698-3268	7	1	RESISTOR 11.5K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1152-F
A2R4	2100-3109	2	1	RESISTOR-TRMR 2K 10% C SIDE-ADJ 17-TRN	73138	89PR2K
A2R5	0757-0465	6	5	RESISTOR 100K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1003-F
A2R6	2100-3054	6	2	RESISTOR-TRMR 50K 10% C SIDE-ADJ 17-TRN	73138	89PR50K
A2R7	0698-7257	2	3	RESISTOR 7.5K 1% .05W F TC=0±100	24546	C3-1/8-T0-7501-F
A2R8	0757-0463	4	1	RESISTOR 82.5K 1% .125W F TC=0±100	24546	CT4-1/8-T0-8252-F
A2R9	0698-7251	6	3	RESISTOR 4.22K 1% .05W F TC=0±100	24546	C3-1/8-T0-4221-F
A2R10	0698-6320	8	1	RESISTOR 5K .1% .125W F TC=0±25	03888	PME55-1/8-T9-5001-B
A2R11	0698-6630	3	1	RESISTOR 20K .1% .125W F TC=0±25	28480	0698-6630
A2R12	0698-3153	9	3	RESISTOR 3.83K 1% .125W F TC=0±100	24546	CT4-1/8-T0-3831-F
A2R13	0698-3431	6	1	RESISTOR 23.7 1% .125W F TC=0±100	03888	PME55-1/8-T0-23R7-F
A2R14	0757-0438	3	7	RESISTOR 5.11K 1% .125W F TC=0±100	24546	CT4-1/8-T0-5111-F
A2R15	0698-3156	2	4	RESISTOR 14.7K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1472-F
A2R17	0757-0465	6		RESISTOR 100K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1003-F
A2R18	0698-3159	5	4	RESISTOR 26.1K 1% .125W F TC=0±100	24546	CT4-1/8-T0-2612-F
A2R20	0757-0442	9	26	RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A2R21	0757-0465	6		RESISTOR 100K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1003-F
A2R22	0757-0465	6		RESISTOR 100K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1003-F
A2R23	2100-3054	6		RESISTOR-TRMR 50K 10% C SIDE-ADJ 17-TRN	73138	89PR50K
A2R24	0698-7260	7	19	RESISTOR 10K 1% .05W F TC=0±100	24546	C3-1/8-T0-1002-F
A2R25	0698-7260	7		RESISTOR 10K 1% .05W F TC=0±100	24546	C3-1/8-T0-1002-F
A2R26	0698-7229	8	3	RESISTOR 511 1% .05W F TC=0±100	24546	C3-1/8-TO-511R-F
A2R27	0698-7260	7		RESISTOR 10K 1% .05W F TC=0±100	24546	C3-1/8-T0-1002-F
A2R29	0698-5437	6	1	RESISTOR 12K .1% .125W F TC=0±50	28480	0698-5437
A2SW1	3101-2751	1	1	SWITCH-RKR DIP-RKR-ASSY 2-1A .015A 24VDC	28480	3101-2751
A2TP1	0360-0535	0	19	TERMINAL-TEST POINT .330IN ABOVE	28480	0360-0535
A2TP2	0360-0535	0		TERMINAL-TEST POINT .330IN ABOVE	28480	0360-0535
A2TP3	0360-0535	0		TERMINAL-TEST POINT .330IN ABOVE	28480	0360-0535
A2U1	1826-0092	3	3	IC OP AMP GP DUAL TO-99 PKG	28480	1826-0092
A2U2	1858-0047	5	2	TRANSISTOR ARRAY 16-PIN PLSTC DIP	13606	ULN-2003A
A2U3	1858-0047	5		TRANSISTOR ARRAY 16-PIN PLSTC DIP	13606	ULN-2003A
A2U4	1820-1416	5	5	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A2U5	1820-1730	6	5	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A2U6	1820-2150	6	1	IC MICPROC-ACCESS NMOS	34649	D8279-5
A2U7	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A2U8	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A2U9	1826-1186	8	6	ANALOG SWITCH 4 SPST 16 -CERDIP	06665	SW-06GQ
A2U10	1858-0069	1	1	TRANSISTOR ARRAY 18-PIN PLSTC DIP	13606	ULN-2803A
A2U12	1826-0205	0	1	IC TIMER TTL	18324	NE556N
A2U13	1820-1199	1	2	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A2VR1	1902-0041	4	2	DIODE-ZNR 5.11V 5% DO-35 PD=.4W	07263	1N751A
A2W2	8159-0005	0	10	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005

See introduction to this section for ordering information.

*Indicates factory selected value.

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3	**83525-60080**	**6**	**1**	**BOARD ASSEMBLY-DIGITAL INTERFACE**	**28480**	**83525-60080**
A3C1	0160-0127	2	5	CAPACITOR-FXD 1UF ±20% 50VDC CER	28480	0160-0127
A3C2	0160-0127	2		CAPACITOR-FXD 1UF ±20% 50VDC CER	28480	0160-0127
A3C3	0160-0127	2		CAPACITOR-FXD 1UF ±20% 50VDC CER	28480	0160-0127
A3C4	0160-0127	2		CAPACITOR-FXD 1UF ±20% 50VDC CER	28480	0160-0127
A3C5	0160-3537	4	1	CAPACITOR-FXD 680PF ±5% 100VDC MICA	28480	0160-3537
A3C6	0180-0500	7	1	CAPACITOR-FXD 47UF±20% 20VDC TA	28480	0180-0500
A3J1	1251-5926	3		CONNECTOR 50-PIN M POST TYPE	28480	1251-5926
A3MP1				NOT ASSIGNED		
A3MP2	5040-6852	3	1	BD EXTR ORANGE	28480	5040-6852
A3MP3	5000-9043	6	5	PIN	28480	5000-9043
A3MP4	7021-4611	2	4	LBL IN MADE USA	28480	7121-4611
A3R1	0757-0428	1	1	RESISTOR 1.62K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1621-F
A3R2	0698-3153	9		RESISTOR 3.83K 1% .125W F TC=0±100	24546	CT4-1/8-T0-3831-F
A3R3	0698-3153	9		RESISTOR 3.83K 1% .125W F TC=0±100	24546	CT4-1/8-T0-3831-F
A3R4	0698-7212	9	6	RESISTOR 100 1% .05W F TC=0±100	24546	C3-1/8-TO-100R-F
A3S1	3101-2243	6	1	SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-2243
A3U1	83595-60074	2	1	ROM REPLACEMENT KIT (U1 NOT SEPARATELY REPLACEABLE)	28480	83595-60074
A3U2	83595-60074	2		ROM REPLACEMENT KIT (U2 NOT SEPARATELY REPLACEABLE)	28480	83595-60074
A3U3	1826-0180	0	3	IC TIMER TTL MONO/ASTBL	18324	NE555N
A3U4	1820-2081	2	1	IC NMOS	04713	MC68A21P
A3U5	1820-3093	8	1	IC-8000-SERIES PROGRAMMABLE TIMER	28480	1820-3093
A3U6	1820-1202	7	2	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A3U7	1820-1197	9	3	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A3U8	1820-1416	5		IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A3U9	1820-1216	3	7	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A3U10	1820-1416	5		IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A3U11	1820-1416	5		IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A3U12	1810-0338	7	3	NETWORK-RES 16-DIP 100.0 OHM X 8	11236	761-3-R100
A3U13	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A3U14	1820-1491	6	1	IC BFR TTL LS NON-INV HEX 1-INP	01295	SN74LS367AN
A3U15	1820-1416	5		IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A3U16	1810-0338	7		NETWORK-RES 16-DIP 100.0 OHM X 8	11236	761-3-R100
A3U17	1820-2075	4	2	IC TRANSCEIVER TTL LS BUS OCTL	01295	SN74LS245N
A3U18	1820-2075	4		IC TRANSCEIVER TTL LS BUS OCTL	01295	SN74LS245N
A3U19	1810-0338	7		NETWORK-RES 16-DIP 100.0 OHM X 8	11236	761-3-R100
A3XU1	1200-0541	1	2	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A3XU2	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
	7121-4611	2	4	LBL IN MADE USA	28480	7121-4611

See introduction to this section for ordering information.

*Indicates factory selected value.

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4	**83592-60132**	**0**	**1**	**BOARD ASSEMBLY-ALC**	**28480**	**83592-60132**
A4C1	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A4C3	0180-2617	1	7	CAPACITOR-FXD 6.8UF±10% 35VDC TA	25088	D6R8GS1B35K
A4C4	0160-0945	2	2	CAPACITOR-FXD 910PF ±5% 100VDC MICA	28480	0160-0945
A4C6	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A4C7	0160-3874	2	6	CAPACITOR-FXD 10PF ±.5PF 200VDC CER	28480	0160-3874
A4C8	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A4C9	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A4C10	0180-2697	7	4	CAPACITOR-FXD 10UF±10% 25VDC TA	28480	0180-2697
A4C11	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A4C12	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A4C13	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A4C14	0160-0127	2		CAPACITOR-FXD 1UF ±20% 50VDC CER	28480	0160-0127
A4C15	0180-2697	7		CAPACITOR-FXD 10UF±10% 25VDC TA	28480	0180-2697
A4C16	0180-2697	7		CAPACITOR-FXD 10UF±10% 25VDC TA	28480	0180-2697
A4C17	0180-2697	7		CAPACITOR-FXD 10UF±10% 25VDC TA	28480	0180-2697
A4C18	0180-2661	5	1	CAPACITOR-FXD 1UF±10% 50VDC TA	25088	D1R0GS1A50K
A4C19	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A4C20	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A4C21	0160-0572	1	3	CAPACITOR-FXD 2200PF ±20% 100VDC CER	28480	0160-0572
A4C22	0160-3874	2		CAPACITOR-FXD 10PF ±.5PF 200VDC CER	28480	0160-3874
A4C23	0121-0448	8	1	CAPACITOR-V TRMR-CER 2.5-5PF 63V PC-MTG	28480	0121-0448
A4C25	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A4C26	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A4C27	0160-3878	6	12	CAPACITOR-FXD 1000PF ±20% 100VDC CER	28480	0160-3878
A4C28	0160-0572	1		CAPACITOR-FXD 2200PF ±20% 100VDC CER	28480	0160-0572
A4C29	0160-3873	1	2	CAPACITOR-FXD 4.7PF ±.5PF 200VDC CER	28480	0160-3873
A4C30	0160-3873	1		CAPACITOR-FXD 4.7PF ±.5PF 200VDC CER	28480	0160-3873
A4C31	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A4CR1	1901-1098	1	10	DIODE-SWITCHING 1N4150 50V 200MA 4NS	15818	1N4150
A4CR2	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	15818	1N4150
A4CR3	1901-0535	9	13	DIODE-SM SIG SCHOTTKY	28480	1901-0535
A4CR4	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	15818	1N4150
A4CR5	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	15818	1N4150
A4CR7	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A4CR8	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A4CR9	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A4CR10	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	15818	1N4150
A4CR11	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	15818	1N4150
A4J1	1258-0124	7	2	SHUNT-PROGRAMMABLE 1 DBL PIN SET; .100	28480	1258-0124
A4J2	1258-0124	7		SHUNT-PROGRAMMABLE 1 DBL PIN SET; .100	28480	1258-0124
A4L1	9140-0210	1	1	INDUCTOR RF-CH-MLD 100UH 5%	28480	9140-0210
A4MP1				NOT ASSIGNED		
A4MP2	5040-6848	7	1	BOARD EXTR YELLOW	28480	5040-6848
A4MP3	5000-9043	6		PIN	28480	5000-9043
A4MP4	1251-4932	9	4	CONNECTOR-SGL CONT SKT .021-IN-BSC-SZ	91506	LSG-1AG14-1
A4MP5	7121-1153	1		LBL IN 83592	28480	7121-1153
A4Q1	1853-0007	7	1	TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A4Q2	1854-0404	0	1	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0404
A4Q3	1854-0295	7	2	TRANSISTOR-DUAL NPN PD=400MW	28480	1854-0295
A4Q5	1855-0386	9	2	TRANSISTOR J-FET 2N4392 N-CHAN D-MODE	04713	2N4392
A4Q6	1855-0386	9		TRANSISTOR J-FET 2N4392 N-CHAN D-MODE	04713	2N4392
A4Q7	1855-0423	5	8	TRANSISTOR MOSFET N-CHAN E-MODE TO-237	17856	VN10KM
A4Q8	1855-0423	5		TRANSISTOR MOSFET N-CHAN E-MODE TO-237	17856	VN10KM
A4Q9	1854-0295	7		TRANSISTOR-DUAL NPN PD=400MW	28480	1854-0295
A4Q10	1853-0316	1		TRANSISTOR-DUAL PNP PD=500MW	28480	1853-0316
A4Q11	1853-0316	1		TRANSISTOR-DUAL PNP PD=500MW	28480	1853-0316
A4Q12	1855-0423	5		TRANSISTOR MOSFET N-CHAN E-MODE TO-237	17856	VN10KM
A4Q13	1855-0423	5		TRANSISTOR MOSFET N-CHAN E-MODE TO-237	17856	VN10KM
A4Q14	1853-0451	5	2	TRANSISTOR PNP 2N3799 SI TO-18 PD=360MW	01295	2N3799
A4Q15	1853-0451	5		TRANSISTOR PNP 2N3799 SI TO-18 PD=360MW	01295	2N3799
A4Q16	1855-0423	5		TRANSISTOR MOSFET N-CHAN E-MODE TO-237	17856	VN10KM
A4R1	2100-2633	5	1	RESISTOR-TRMR 1K 10% C SIDE-ADJ 1-TRN	73138	82PAR1K
A4R2	0698-7267	4	3	RESISTOR 19.6K 1% .05W F TC=0±100	24546	C3-1/8-T0-1962-F
A4R7	2100-2516	3	1	RESISTOR-TRMR 100K 10% C SIDE-ADJ 1-TRN	73138	82PAR100K
A4R8	2100-2515	2	1	RESISTOR-TRMR 200K 10% C SIDE-ADJ 1-TRN	73138	82PAR200K
A4R9	2100-0670	6	5	RESISTOR-TRMR 10K 10% C SIDE-ADJ 17-TRN	28480	2100-0670

See introduction to this section for ordering information.

*Indicates factory selected value.

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4R10	2100-0670	6		RESISTOR-TRMR 10K 10% C SIDE-ADJ 17-TRN	28480	2100-0670
A4R12	2100-3753	2	2	RESISTOR-TRMR 200K 10% C SIDE-ADJ 17-TRN	28480	2100-3753
A4R13	2100-0544	3	2	RESISTOR-TRMR 100K 10% C SIDE-ADJ 17-TRN	28480	2100-0544
A4R14	2100-0670	6		RESISTOR-TRMR 10K 10% C SIDE-ADJ 17-TRN	28480	2100-0670
A4R15	2100-2489	9	1	RESISTOR-TRMR 5K 10% C SIDE-ADJ 1-TRN	73138	82PAR5K
A4R16	0698-7253	8	3	RESISTOR 5.11K 1% .05W F TC=0±100	24546	C3-1/8-T0-5111-F
A4R17	0698-7253	8		RESISTOR 5.11K 1% .05W F TC=0±100	24546	C3-1/8-T0-5111-F
A4R18	0698-7257	2		RESISTOR 7.5K 1% .05W F TC=0±100	24546	C3-1/8-T0-7501-F
A4R19	0698-7263	0		RESISTOR 13.3K 1% .05W F TC=0±100	24546	C3-1/8-T0-1332-F
A4R20	0698-7258	3	1	RESISTOR 8.25K 1% .05W F TC=0±100	24546	C3-1/8-T0-8251-F
A4R21	0698-7261	8	3	RESISTOR 11K 1% .05W F TC=0±100	24546	C3-1/8-T0-1102-F
A4R22	0698-7262	9	2	RESISTOR 12.1K 1% .05W F TC=0±100	24546	C3-1/8-T0-1212-F
A4R23	0698-7276	5	1	RESISTOR 46.4K 1% .05W F TC=0±100	24546	C3-1/8-T0-4642-F
A4R24	0698-7261	8		RESISTOR 11K 1% .05W F TC=0±100	24546	C3-1/8-T0-1102-F
A4R25	0698-7261	8		RESISTOR 11K 1% .05W F TC=0±100	24546	C3-1/8-T0-1102-F
A4R26	0698-7260	7		RESISTOR 10K 1% .05W F TC=0±100	24546	C3-1/8-T0-1002-F
A4R27	0698-7231	2	1	RESISTOR 619 1% .05W F TC=0±100	24546	C3-1/8-TO-619R-F
A4R28	0698-7254	9	1	RESISTOR 5.62K 1% .05W F TC=0±100	24546	C3-1/8-T0-5621-F
A4R30	0837-0119	7	1	THERMISTOR TUB WITH AXL LEADS 5K-OHM	28480	0837-0119
A4R31	0698-7279	8		RESISTOR 61.9K 1% .05W F TC=0±100	24546	C3-1/8-T0-6192-F
A4R32	0698-7264	1	3	RESISTOR 14.7K 1% .05W F TC=0±100	24546	C3-1/8-T0-1472-F
A4R33	0698-7249	2	2	RESISTOR 3.48K 1% .05W F TC=0±100	24546	C3-1/8-T0-3481-F
A4R34	0698-3457	6	3	RESISTOR 316K 1% .125W F TC=0±100	28480	0698-3457
A4R35	0698-7260	7		RESISTOR 10K 1% .05W F TC=0±100	24546	C3-1/8-T0-1002-F
A4R36	0698-7260	7		RESISTOR 10K 1% .05W F TC=0±100	24546	C3-1/8-T0-1002-F
A4R38	0698-7243	6	7	RESISTOR 1.96K 1% .05W F TC=0±100	24546	C3-1/8-T0-1961-F
A4R39	0698-7282	3	1	RESISTOR 82.5K 1% .05W F TC=0±100	24546	C3-1/8-T0-8252-F
A4R40*	0698-7279	8	3	RESISTOR 61.9K 1% .05W F TC=0±100	24546	C3-1/8-T0-6192-F
A4R41*	0698-7279	8		RESISTOR 61.9K 1% .05W F TC=0±100	24546	C3-1/8-T0-6192-F
A4R42	0698-7256	1	3	RESISTOR 6.81K 1% .05W F TC=0±100	24546	C3-1/8-T0-6811-F
A4R43*	0698-7270	9	1	RESISTOR 26.1K 1% .05W F TC=0±100	24546	C3-1/8-T0-2612-F
A4R44	0698-7233	4	1	RESISTOR 750 1% .05W F TC=0±100	24546	C3-1/8-T0-750R-F
A4R45	0698-7243	6		RESISTOR 1.96K 1% .05W F TC=0±100	24546	C3-1/8-T0-1961-F
A4R46	0698-7234	5	4	RESISTOR 825 1% .05W F TC=0±100	24546	C3-1/8-T0-825R-F
A4R47	0837-0085	6	1	THERMISTOR ROD 680-OHM TC=+.7%/C-DEG	28480	0837-0085
A4R48	0698-7238	9	2	RESISTOR 1.21K 1% .05W F TC=0±100	24546	C3-1/8-T0-1211-F
A4R49	0698-7205	0	3	RESISTOR 51.1 1% .05W F TC=0±100	24546	C3-1/8-TO-51R1-F
A4R50	0757-0399	5	1	RESISTOR 82.5 1% .125W F TC=0±100	24546	CT4-1/8-T0-82R5-F
A4R51	0698-7236	7		RESISTOR 1K 1% .05W F TC=0±100	24546	C3-1/8-T0-1001-F
A4R52	0698-7229	8		RESISTOR 511 1% .05W F TC=0±100	24546	C3-1/8-TO-511R-F
A4R53	0698-7232	3	2	RESISTOR 681 1% .05W F TC=0±100	24546	C3-1/8-TO-681R-F
A4R54	0698-3151	7	2	RESISTOR 2.87K 1% .125W F TC=0±100	24546	CT4-1/8-TO-2871-F
A4R56	0698-7260	7		RESISTOR 10K 1% .05W F TC=0±100	24546	C3-1/8-T0-1002-F
A4R57	0698-7249	2		RESISTOR 3.48K 1% .05W F TC=0±100	24546	C3-1/8-T0-3481-F
A4R58	0698-7256	1		RESISTOR 6.81K 1% .05W F TC=0±100	24546	C3-1/8-T0-6811-F
A4R59	0698-7229	8		RESISTOR 511 1% .05W F TC=0±100	24546	C3-1/8-TO-511R-F
A4R60	0698-7247	0	1	RESISTOR 2.87K 1% .05W F TC=0±100	24546	C3-1/8-T0-2871-F
A4R61	0698-7219	6	2	RESISTOR 196 1% .05W F TC=0±100	24546	C3-1/8-TO-196R-F
A4R62	0698-7212	9		RESISTOR 100 1% .05W F TC=0±100	24546	C3-1/8-TO-100R-F
A4R63	0698-7243	6		RESISTOR 1.96K 1% .05W F TC=0±100	24546	C3-1/8-T0-1961-F
A4R64	0698-7256	1		RESISTOR 6.81K 1% .05W F TC=0±100	24546	C3-1/8-T0-6811-F
A4R68	0698-7222	1	1	RESISTOR 261 1% .05W F TC=0±100	24546	C3-1/8-TO-261R-F
A4R69	0698-7277	6	3	RESISTOR 51.1K 1% .05W F TC=0±100	24546	C3-1/8-T0-5112-F
A4R70	0698-7246	9	1	RESISTOR 2.61K 1% .05W F TC=0±100	24546	C3-1/8-T0-2611-F
A4R71	0698-7268	5		RESISTOR 21.5K 1% .05W F TC=0±100	24546	C3-1/8-T0-2152-F
A4R72	0698-7212	9		RESISTOR 100 1% .05W F TC=0±100	24546	C3-1/8-TO-100R-F
A4R73	0698-7212	9		RESISTOR 100 1% .05W F TC=0±100	24546	C3-1/8-TO-100R-F
A4R74	0698-7243	6		RESISTOR 1.96K 1% .05W F TC=0±100	24546	C3-1/8-T0-1961-F
A4R75	0698-7274	3	1	RESISTOR 38.3K 1% .05W F TC=0±100	24546	C3-1/8-T0-3832-F
A4R76	0698-7260	7		RESISTOR 10K 1% .05W F TC=0±100	24546	C3-1/8-T0-1002-F
A4R77	0698-7260	7		RESISTOR 10K 1% .05W F TC=0±100	24546	C3-1/8-T0-1002-F
A4R78	2100-1986	9	1	RESISTOR-TRMR 1K 10% C TOP-ADJ 1-TRN	73138	82PR1K
A4R79	0698-7260	7		RESISTOR 10K 1% .05W F TC=0±100	24546	C3-1/8-T0-1002-F
A4R80	0698-7205	0		RESISTOR 51.1 1% .05W F TC=0±100	24546	C3-1/8-TO-51R1-F
A4R81	2100-2030	6	5	RESISTOR-TRMR 20K 10% C TOP-ADJ 1-TRN	73138	82PR20K
A4R82	2100-2030	6		RESISTOR-TRMR 20K 10% C TOP-ADJ 1-TRN	73138	82PR20K
A4R83	0698-7234	5		RESISTOR 825 1% .05W F TC=0±100	24546	C3-1/8-T0-825R-F
A4R84	0698-7232	3		RESISTOR 681 1% .05W F TC=0±100	24546	C3-1/8-T0-681R-F
A4R85	0698-7260	7		RESISTOR 10K 1% .05W F TC=0±100	24546	C3-1/8-T0-1002-F
A4R86	0698-7251	6		RESISTOR 4.22K 1% .05W F TC=0±100	24546	C3-1/8-T0-4221-F

See introduction to this section for ordering information.

*Indicates factory selected value.

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4R87	0698-7243	6		RESISTOR 1.96K 1% .05W F TC=0±100	24546	C3-1/8-T0-1961-F
A4R88	0698-7264	1		RESISTOR 14.7K 1% .05W F TC=0±100	24546	C3-1/8-T0-1472-F
A4R89	0698-7263	0		RESISTOR 13.3K 1% .05W F TC=0±100	24546	C3-1/8-T0-1332-F
A4R90	0698-7264	1		RESISTOR 14.7K 1% .05W F TC=0±100	24546	C3-1/8-T0-1472-F
A4R91	0698-7240	3	1	RESISTOR 1.47K 1% .05W F TC=0±100	24546	C3-1/8-T0-1471-F
A4R92*	0698-7280	1	6	RESISTOR 68.1K 1% .05W F TC=0±100	24546	C3-1/8-T0-6812-F
A4R93	0698-7260	7		RESISTOR 10K 1% .05W F TC=0±100	24546	C3-1/8-T0-1002-F
A4R94	0698-7242	5	3	RESISTOR 1.78K 1% .05W F TC=0±100	24546	C3-1/8-T0-1781-F
A4R96	0698-7251	6		RESISTOR 4.22K 1% .05W F TC=0±100	24546	C3-1/8-T0-4221-F
A4R97	0698-7267	4		RESISTOR 19.6K 1% .05W F TC=0±100	24546	C3-1/8-T0-1962-F
A4R98	0698-7257	2		RESISTOR 7.5K 1% .05W F TC=0±100	24546	C3-1/8-T0-7501-F
A4R99	2100-1738	9	2	RESISTOR-TRMR 10K 10% C TOP-ADJ 1-TRN	73138	82PR10K
A4R100	0698-7262	9		RESISTOR 12.1K 1% .05W F TC=0±100	24546	C3-1/8-T0-1212-F
A4R101*	0698-7263	0	3	RESISTOR 13.3K 1% .05W F TC=0±100	24546	C3-1/8-T0-1332-F
A4R102	0698-3440	7		RESISTOR 196 1% .125W F TC=0±100	24546	CT4-1/8-TO-196R-F
A4R103	0757-0424	7	1	RESISTOR 1.1K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1101-F
A4R105	0698-7205	0		RESISTOR 51.1 1% .05W F TC=0±100	24546	C3-1/8-TO-51R1-F
A4R106*	0698-3440	7	2	RESISTOR 196 1% .125W F TC=0±100	24546	CT4-1/8-TO-196R-F
A4R108	0698-8827	4	5	RESISTOR 1M 1% .125W F TC=0±100	28480	0698-8827
A4R110	0698-7243	6		RESISTOR 1.96K 1% .05W F TC=0±100	24546	C3-1/8-T0-1961-F
A4TP1	1251-5618	0	16	CONNECTOR 8-PIN M POST TYPE	28480	1251-5618
A4TP2	1251-5618	0		CONNECTOR 8-PIN M POST TYPE	28480	1251-5618
A4TP3	1251-5618	0		CONNECTOR 8-PIN M POST TYPE	28480	1251-5618
A4TP4	1251-5618	0		CONNECTOR 8-PIN M POST TYPE	28480	1251-5618
A4TP5	1251-5618	0		CONNECTOR 8-PIN M POST TYPE	28480	1251-5618
A4TP6	1251-5618	0		CONNECTOR 8-PIN M POST TYPE	28480	1251-5618
A4TP7	1251-5618	0		CONNECTOR 8-PIN M POST TYPE	28480	1251-5618
A4TP8	1251-5618	0		CONNECTOR 8-PIN M POST TYPE	28480	1251-5618
A4TP9	0360-0535	0		TERMINAL-TEST POINT .330IN ABOVE	28480	0360-0535
A4TP10	0360-0535	0		TERMINAL-TEST POINT .330IN ABOVE	28480	0360-0535
A4TP11	0360-0535	0		TERMINAL-TEST POINT .330IN ABOVE	28480	0360-0535
A4TP12	0360-0535	0		TERMINAL-TEST POINT .330IN ABOVE	28480	0360-0535
A4U1	1826-1186	8		ANALOG SWITCH 4 SPST 16 -CERDIP	06665	SW-06GQ
A4U2	1826-0616	7	2	IC OP AMP PRCN QUAD 14-DIP-C PKG	06665	OP-11EY
A4U3	1826-0610	1	2	IC MULTIPLXR 4-CHAN-ANLG DUAL 16-DIP-C	06665	MUX24FQ
A4U4	1826-1186	8		ANALOG SWITCH 4 SPST 16 -CERDIP	06665	SW-06GQ
A4U5	1826-0616	7		IC OP AMP PRCN QUAD 14-DIP-C PKG	06665	OP-11EY
A4U6	1826-0610	1		IC MULTIPLXR 4-CHAN-ANLG DUAL 16-DIP-C	06665	MUX24FQ
A4U7	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A4U8	1826-1186	8		ANALOG SWITCH 4 SPST 16 -CERDIP	06665	SW-06GQ
A4U9	1826-0319	7	2	IC OP AMP LOW-BIAS-H-IMPD TO-99 PKG	04713	LF356G
A4U10	1826-1221	2	3	IC COMPARATOR PRCN 8-DIP-C PKG	28480	1826-1221
A4U11	1826-0752	2	6	D/A 12-BIT 16-CBRZ/SDR CMOS	24355	AD7542BD
A4U12	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A4U13	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A4U14	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A4U15	1820-1198	0	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS03N
A4U16	1826-0021	8	1	IC OP AMP GP TO-99 PKG	27014	LM310H
A4U17	1826-0447	2	1	IC OP AMP WB TO-99 PKG	27014	LF257H
A4U18	1826-0319	7		IC OP AMP LOW-BIAS-H-IMPD TO-99 PKG	04713	LF356G
A4VR1	1902-0041	4		DIODE-ZNR 5.11V 5% DO-35 PD=.4W	07263	1N751A
A4VR2	1902-0111	9	1	DIODE-ZNR 1N753A 6.2V 5% DO-7 PD=.4W	28480	1902-0111
A4VR3	1902-3070	5	2	DIODE-ZNR 4.22V 5% DO-35 PD=.4W	28480	1902-3070
A4VR4	1902-0049	2	2	DIODE-ZNR 6.19V 5% DO-35 PD=.4W	28480	1902-0049
A4VR5	1902-0049	2		DIODE-ZNR 6.19V 5% DO-35 PD=.4W	28480	1902-0049
A4W4	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
A4W6	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005

See introduction to this section for ordering information.

*indicates factory selected value.

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5	**83592-60005**	**6**	**1**	**BOARD ASSEMBLY-FM**	**28480**	**83592-60005**
A5C1	0160-0575	4	6	CAPACITOR-FXD .047UF ±20% 50VDC CER	28480	0160-0575
A5C2	0160-0572	1		CAPACITOR-FXD 2200PF ±20% 100VDC CER	28480	0160-0572
A5C3	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A5C4	0160-0945	2		CAPACITOR-FXD 910PF ±5% 100VDC MICA	28480	0160-0945
A5C5	0160-0575	4		CAPACITOR-FXD .047UF ±20% 50VDC CER	28480	0160-0575
A5C6	0160-2247	1	1	CAPACITOR-FXD 3.9PF ±.25PF 500VDC CER	28480	0160-2247
A5C7	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A5C8	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A5C9	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A5C10	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A5C11	0140-0198	5	1	CAPACITOR-FXD 200PF ±5% 300VDC MICA	72136	DM15F201J0300WV1CR
A5C12	0160-2199	2	1	CAPACITOR-FXD 30PF ±5% 300VDC MICA	28480	0160-2199
A5C14	0121-0446	6	1	CAPACITOR-V TRMR-CER 4.5-20PF 160V	28480	0121-0446
A5C15	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A5C16	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A5C17	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A5C18	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A5C20	0160-2249	3	2	CAPACITOR-FXD 4.7PF ±.25PF 500VDC CER	28480	0160-2249
A5C23	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A5C24	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A5C25	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A5C26	0160-3874	2		CAPACITOR-FXD 10PF ±.5PF 200VDC CER	28480	0160-3874
A5C27	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A5C28	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A5C29	0180-2617	1		CAPACITOR-FXD 6.8UF±10% 35VDC TA	25088	D6R8GS1B35K
A5C30	0180-2617	1		CAPACITOR-FXD 6.8UF±10% 35VDC TA	25088	D6R8GS1B35K
A5C31	0180-2617	1		CAPACITOR-FXD 6.8UF±10% 35VDC TA	25088	D6R8GS1B35K
A5C32	0180-2617	1		CAPACITOR-FXD 6.8UF±10% 35VDC TA	25088	D6R8GS1B35K
A5C33	0180-2207	5	1	CAPACITOR-FXD 100UF±10% 10VDC TA	56289	150D107X9010R2
A5C34	0180-0474	4	6	CAPACITOR-FXD 15UF±10% 20VDC TA	28480	0180-0474
A5C35	0180-0474	4		CAPACITOR-FXD 15UF±10% 20VDC TA	28480	0180-0474
A5C36	0180-0474	4		CAPACITOR-FXD 15UF±10% 20VDC TA	28480	0180-0474
A5C37	0180-0474	4		CAPACITOR-FXD 15UF±10% 20VDC TA	28480	0180-0474
A5C38	0180-0474	4		CAPACITOR-FXD 15UF±10% 20VDC TA	28480	0180-0474
A5C39	0180-0474	4		CAPACITOR-FXD 15UF±10% 20VDC TA	28480	0180-0474
A5C40	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A5C41	0160-2249	3		CAPACITOR-FXD 4.7PF ±.25PF 500VDC CER	28480	0160-2249
A5CR1	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-35	9N171	1N645
A5CR2	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-35	9N171	1N645
A5CR3	1901-0047	8	2	DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A5CR4	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A5CR5	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	15818	1N4150
A5CR6	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	15818	1N4150
A5CR7	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	15818	1N4150
A5CR8	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	15818	1N4150
A5CR9	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A5K1	0490-0916	6		RELAY-REED 1A 500MA 100VDC 5VDC-COIL	28480	0490-0916
A5K2	0490-1063	6	1	RELAY-REED 2A 500MA 50VDC 5VDC-COIL 10VA	28480	0490-1063
A5L1	9100-1625	0	1	INDUCTOR RF-CH-MLD 33UH 5%	28480	9100-1625
A5L2	9100-1619	2	4	INDUCTOR RF-CH-MLD 6.8UH 10%	28480	9100-1619
A5L3	9100-1619	2		INDUCTOR RF-CH-MLD 6.8UH 10%	28480	9100-1619
A5L4	08503-80001	9	4	COIL TOROID	28480	08503-80001
A5L5	9100-1619	2		INDUCTOR RF-CH-MLD 6.8UH 10%	28480	9100-1619
A5L6	9100-1619	2		INDUCTOR RF-CH-MLD 6.8UH 10%	28480	9100-1619
A5MP1				NOT ASSIGNED		
A5MP2	5040-6851	2	1	EXTRACTOR TAB	28480	5040-6851
A5MP3	5000-9043	6		PIN	28480	5000-9043
A5MP4	4330-0145	9	1	INSULATOR-BEAD GLASS	28480	4330-0145
A5MP5	7121-1250	9	1	LBL IN 83592	28480	7121-1250
A5MP6	7121-4611	2		LBL MADE IN USA	28480	7121-4611
A5MP7	1200-0173	5	4	INSULATOR-XSTR DAP-GL	2848	1200-0173
A5Q1	1854-0529	0	4	TRANSISTOR-DUAL NPN PD=750MW	28480	1854-0529
A5Q2	1854-0529	0		TRANSISTOR-DUAL NPN PD=750MW	28480	1854-0529
A5Q3	1854-0529	0		TRANSISTOR-DUAL NPN PD=750MW	28480	1854-0529
A5Q4	1854-0529	0		TRANSISTOR-DUAL NPN PD=750MW	28480	1854-0529
A5Q5	1854-0475	5	1	TRANSISTOR-DUAL NPN PD=750MW	28480	1854-0475

See introduction to this section for ordering information. *Indicates factory selected value.

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5R1	0698-0083	8	9	RESISTOR 1.96K 1% .125W F TC=0±100	24546	CT4-1/8-TO-1961-F
A5R2	0698-3154	0	4	RESISTOR 4.22K 1% .125W F TC=0±100	24546	CT4-1/8-TO-4221-F
A5R3	0698-3154	0		RESISTOR 4.22K 1% .125W F TC=0±100	24546	CT4-1/8-TO-4221-F
A5R4	0698-3154	0		RESISTOR 4.22K 1% .125W F TC=0±100	24546	CT4-1/8-TO-4221-F
A5R5	0698-3154	0		RESISTOR 4.22K 1% .125W F TC=0±100	24546	CT4-1/8-TO-4221-F
A5R6	0757-0439	4	2	RESISTOR 6.81K 1% .125W F TC=0±100	24546	CT4-1/8-T0-6811-F
A5R7	0757-0439	4		RESISTOR 6.81K 1% .125W F TC=0±100	24546	CT4-1/8-T0-6811-F
A5R8	0698-3158	4	2	RESISTOR 23.7K 1% .125W F TC=0±100	24546	CT4-1/8-T0-2372-F
A5R9	0698-6360	6	6	RESISTOR 10K .1% .125W F TC=0±25	28480	0698-6360
A5R10	0699-0124	0	1	RESISTOR 10.2K .1% .125W F TC=0±25	28480	0699-0124
A5R11	0698-3155	1	2	RESISTOR 4.64K 1% .125W F TC=0±100	24546	CT4-1/8-T0-4641-F
A5R12	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0±100	24546	CT4-1/8-TO-1961-F
A5R13	0698-3446	3	2	RESISTOR 383 1% .125W F TC=0±100	24546	CT4-1/8-T0-383R-F
A5R14	0757-0394	0	2	RESISTOR 51.1 1% .125W F TC=0±100	24546	CT4-1/8-T0-51R1-F
A5R15	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0±100	24546	CT4-1/8-T0-51R1-F
A5R17	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A5R18	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A5R19	2100-3749	6	3	RESISTOR-TRMR 5K 10% C SIDE-ADJ 17-TRN	28480	2100-3749
A5R20	0757-0458	7	4	RESISTOR 51.1K 1% .125W F TC=0±100	24546	CT4-1/8-T0-5112-F
A5R21	0698-3136	8	1	RESISTOR 17.8K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1782-F
A5R22	0698-6360	6		RESISTOR 10K .1% .125W F TC=0±25	28480	0698-6360
A5R23	0698-3151	7		RESISTOR 2.87K 1% .125W F TC=0±100	24546	CT4-1/8-TO-2871-F
A5R26	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0±100	24546	CT4-1/8-TO-1961-F
A5R27	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0±100	24546	CT4-1/8-TO-1961-F
A5R28	0757-0382	6	2	RESISTOR 16.2 1% .125W F TC=0±100	19701	5033R-1/8-T0-16R2-F
A5R29	0757-0382	6		RESISTOR 16.2 1% .125W F TC=0±100	19701	5033R-1/8-T0-16R2-F
A5R30	0757-0398	4		RESISTOR 75 1% .125W F TC=0±100	24546	CT4-1/8-T0-75R0-F
A5R32	0757-0403	2	2	RESISTOR 121 1% .125W F TC=0±100	24546	CT4-1/8-TO-121R-F
A5R33	0698-7280	1		RESISTOR 68.1K 1% .05W F TC=0±100	24546	C3-1/8-T0-6812-F
A5R34	2100-2574	3	4	RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	73138	82PAR500
A5R35	0698-7280	1		RESISTOR 68.1K 1% .05W F TC=0±100	24546	C3-1/8-T0-6812-F
A5R36	2100-2574	3		RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	73138	82PAR500
A5R37	0698-7280	1		RESISTOR 68.1K 1% .05W F TC=0±100	24546	C3-1/8-T0-6812-F
A5R38	2100-2574	3		RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	73138	82PAR500
A5R39	0698-7280	1		RESISTOR 68.1K 1% .05W F TC=0±100	24546	C3-1/8-T0-6812-F
A5R40	2100-2574	3		RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	73138	82PAR500
A5R41	2100-3611	1	9	RESISTOR-TRMR 50K 10% C SIDE-ADJ 17-TRN	28480	2100-3611
A5R42	2100-3611	1		RESISTOR-TRMR 50K 10% C SIDE-ADJ 17-TRN	28480	2100-3611
A5R43	2100-3611	1		RESISTOR-TRMR 50K 10% C SIDE-ADJ 17-TRN	28480	2100-3611
A5R44	2100-3611	1		RESISTOR-TRMR 50K 10% C SIDE-ADJ 17-TRN	28480	2100-3611
A5R45	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A5R46	0757-0420	3	3	RESISTOR 750 1% .125W F TC=0±100	24546	CT4-1/8-T0-751-F
A5R47	0757-0420	3		RESISTOR 750 1% .125W F TC=0±100	24546	CT4-1/8-T0-751-F
A5R48	2100-3759	8	2	RESISTOR-TRMR 2K 10% C SIDE-ADJ 17-TRN	28480	2100-3759
A5R49	0698-7280	1		RESISTOR 68.1K 1% .05W F TC=0±100	24546	C3-1/8-T0-6812-F
A5R50	2100-3749	6		RESISTOR-TRMR 5K 10% C SIDE-ADJ 17-TRN	28480	2100-3749
A5R51	0698-3156	2		RESISTOR 14.7K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1472-F
A5R52	0698-3156	2		RESISTOR 14.7K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1472-F
A5R53	0757-0346	2	6	RESISTOR 10 1% .125W F TC=0±100	28480	0757-0346
A5R54	0757-0346	2		RESISTOR 10 1% .125W F TC=0±100	28480	0757-0346
A5R55	0757-0346	2		RESISTOR 10 1% .125W F TC=0±100	28480	0757-0346
A5R56	0757-0346	2		RESISTOR 10 1% .125W F TC=0±100	28480	0757-0346
A5R57	0757-0346	2		RESISTOR 10 1% .125W F TC=0±100	28480	0757-0346
A5R58	0757-0346	2		RESISTOR 10 1% .125W F TC=0±100	28480	0757-0346
A5R59	0698-6360	6		RESISTOR 10K .1% .125W F TC=0±25	28480	0698-6360
A5R60	0698-6360	6		RESISTOR 10K .1% .125W F TC=0±25	28480	0698-6360
A5R61	0698-6360	6		RESISTOR 10K .1% .125W F TC=0±25	28480	0698-6360
A5R62	0698-6360	6		RESISTOR 10K .1% .125W F TC=0±25	28480	0698-6360
A5R63	0757-0467	8	1	RESISTOR 121K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1213-F
A5R64	0698-6363	9	2	RESISTOR 40K .1% .125W F TC=0±25	28480	0698-6363
A5R65	0757-0289	2	2	RESISTOR 13.3K 1% .125W F TC=0±100	19701	5033R-1/8-T0-1332-F
A5R66	0698-6363	9		RESISTOR 40K .1% .125W F TC=0±25	28480	0698-6363
A5R67	0698-3447	4	6	RESISTOR 422 1% .125W F TC=0±100	24546	CT4-1/8-T0-422R-F
A5R68	0698-3447	4		RESISTOR 422 1% .125W F TC=0±100	24546	CT4-1/8-T0-422R-F
A5R69	0698-3447	4		RESISTOR 422 1% .125W F TC=0±100	24546	CT4-1/8-T0-422R-F
A5R70	0698-3447	4		RESISTOR 422 1% .125W F TC=0±100	24546	CT4-1/8-T0-422R-F
A5R71	0698-3447	4		RESISTOR 422 1% .125W F TC=0±100	24546	CT4-1/8-T0-422R-F
A5R72	0698-3447	4		RESISTOR 422 1% .125W F TC=0±100	24546	CT4-1/8-T0-422R-F
A5R73	0757-0280	3	11	RESISTOR 1K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1001-F
A5R74	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1001-F

See introduction to this section for ordering information.

*Indicates factory selected value.

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5R75	2100-2522	1	1	RESISTOR-TRMR 10K 10% C SIDE-ADJ 1-TRN	73138	82PAR10K
A5R76	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1001-F
A5R77	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1001-F
A5R78	0698-3158	4		RESISTOR 23.7K 1% .125W F TC=0±100	24546	CT4-1/8-T0-2372-F
A5R79	0757-0403	2		RESISTOR 121 1% .125W F TC=0±100	24546	CT4-1/8-TO-121R-F
A5R80	0698-0082	7	1	RESISTOR 464 1% .125W F TC=0±100	24546	CT4-1/8-T0-4640-F
A5TP1	0360-0535	0		TERMINAL-TEST POINT .330IN ABOVE	28480	0360-0535
A5TP2	0360-0535	0		TERMINAL-TEST POINT .330IN ABOVE	28480	0360-0535
A5TP3	0360-0535	0		TERMINAL-TEST POINT .330IN ABOVE	28480	0360-0535
A5TP4	0360-0535	0		TERMINAL-TEST POINT .330IN ABOVE	28480	0360-0535
A5TP5	0360-0535	0		TERMINAL-TEST POINT .330IN ABOVE	28480	0360-0535
A5TP6	0360-0535	0		TERMINAL-TEST POINT .330IN ABOVE	28480	0360-0535
A5TP7	0360-0535	0		TERMINAL-TEST POINT .330IN ABOVE	28480	0360-0535
A5TP8	0360-0535	0		TERMINAL-TEST POINT .330IN ABOVE	28480	0360-0535
A5TP9	0360-0535	0		TERMINAL-TEST POINT .330IN ABOVE	28480	0360-0535
A5TP10	0360-0535	0		TERMINAL-TEST POINT .330IN ABOVE	28480	0360-0535
A5TP11	0360-0535	0		TERMINAL-TEST POINT .330IN ABOVE	28480	0360-0535
A5U1	1810-0206	8	1	NETWORK-RES 8-SIP 10.0K OHM X 7	11236	750-81-R10K
A5U2	1810-0208	0	1	NETWORK-RES 8-SIP 68.0K OHM X 7	11236	750-81-R68K
A5U3	1826-0416	5	3	IC SWITCH ANLG QUAD 16-DIP-C PKG	27014	LF13331D
A5U4	1810-0205	7	1	NETWORK-RES 8-SIP 4.7K OHM X 7	11236	750-81-R4.7K
A5U5	1810-0321	8	1	NETWORK-RES 8-SIP 220.0K OHM X 7	11236	750-81-R220K
A5U6	1820-1196	8	5	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A5U7	1826-0092	3		IC OP AMP GP DUAL TO-99 PKG	28480	1826-0092
A5U8	1826-0349	3	1	IC V RGLTR TO-39	07263	UA78M06HL
A5U9	1826-0558	6	1	IC 337 V RGLTR TO-39	27014	LM337H
A5U10	1826-0546	2	1	IC WIDEBAND AMPL VID TO-100 PKG	18324	NE592H
A5U11	1826-0476	7	2	IC SWITCH ANLG 8-DIP-P PKG	01295	TL601CP
A5U12	1826-0416	5		IC SWITCH ANLG QUAD 16-DIP-C PKG	27014	LF13331D
A5U13	1826-0416	5		IC SWITCH ANLG QUAD 16-DIP-C PKG	27014	LF13331D
A5U14	1826-0557	5	1	IC OP AMP GP QUAD 14-DIP-C PKG	27014	LM348J
A5U16	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A5U17	1826-0699	6	1	D/A 8-BIT 16-CBRZ/SDR CMOS	24355	AD7524AD
A5U18	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A5U19	1826-0700	0	1	IC OP AMP WB 14-DIP-C PKG	34371	HA1-5195-5
A5U20	1820-0224	1	1	IC OP AMP SPCL TO-99 PKG	27014	LH0002CH
A5U21	1810-0366	1	1	NETWORK-RES 6-SIP 220.0 OHM X 5	11236	750-61-R220
A5VR1	1902-3002	3	3	DIODE-ZNR 2.37V 5% DO-7 PD=.4W TC=-.074%	28480	1902-3002
A5VR2	1902-3002	3		DIODE-ZNR 2.37V 5% DO-7 PD=.4W TC=-.074%	28480	1902-3002
A5W1	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
A5W4	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
A5W5	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
A5W6	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
A5W7	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005

See introduction to this section for ordering information.

*Indicates factory selected value.

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6	**83592-60106**	**8**	**1**	**BOARD ASSEMBLY-SWEEP CONTROL**	**28480**	**83592-60106**
A6C5	0180-2617	1		CAPACITOR-FXD 6.8UF ±10% 35VDC TA	25088	D6R8GS1B35K
A6C6	0180-2617	1		CAPACITOR-FXD 6.8UF ±10% 35VDC TA	25088	D6R8GS1B35K
A6C7	0180-2815	1	3	CAPACITOR-FXD 100UF ±20% 10VDC TA	28480	0180-2815
A6C9	0180-0228	6	6	CAPACITOR-FXD 22UF ±10% 15VDC TA	56289	150D226X9015B2
A6C10	0180-0228	6		CAPACITOR-FXD 22UF ±10% 15VDC TA	56289	150D226X9015B2
A6C14	0160-3878	6		CAPACITOR-FXD 1000PF ±20% 100VDC CER	28480	0160-3878
A6C15	0160-0573	2	1	CAPACITOR-FXD 4700PF ±20% 100VDC CER	28480	0160-0573
A6C16	0160-3878	6		CAPACITOR-FXD 1000PF ±20% 100VDC CER	28480	0160-3878
A6C17	0160-3878	6		CAPACITOR-FXD 1000PF ±20% 100VDC CER	28480	0160-3878
A6C19	0160-0575	4		CAPACITOR-FXD .047UF ±20% 50VDC CER	28480	0160-0575
A6C20	0160-3878	6		CAPACITOR-FXD 1000PF ±20% 100VDC CER	28480	0160-3878
A6C21	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A6C22	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A6C23	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A6C24	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A6C25	0160-3878	6		CAPACITOR-FXD 1000PF ±20% 100VDC CER	28480	0160-3878
A6C26	0160-3878	6		CAPACITOR-FXD 1000PF ±20% 100VDC CER	28480	0160-3878
A6C27	0160-0575	4		CAPACITOR-FXD .047UF ±20% 50VDC CER	28480	0160-0575
A6C28	0160-3874	2		CAPACITOR-FXD 10PF ±.5PF 200VDC CER	28480	0160-3874
A6CR1	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A6CR2	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A6CR3	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A6CR4	1901-0050	3	7	DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A6CR5	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A6CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A6CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A6CR10	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A6CR11	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A6CR12	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A6CR13	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-35	9N171	1N645
A6L1	9140-0137	1	6	INDUCTOR RF-CH-MLD 1MH 5%	28480	9140-0137
A6L2	9140-0137	1		INDUCTOR RF-CH-MLD 1MH 5%	28480	9140-0137
A6L3	08503-80001	9		COIL TOROID	28480	08503-80001
A6MP1				NOT ASSIGNED		
A6MP2	5040-6849	8	1	BD EXTR BLUE	28480	5040-6849
A6MP3	5000-9043	6		PIN	28480	5000-9043
A6MP4	7121-1153	1		LBL IN 83592	28480	7121-1153
A6Q1	1855-0423	5		TRANSISTOR MOSFET N-CHAN E-MODE TO-237	17856	VN10KM
A6Q2	1854-0477	7		TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
A6Q3	1855-0423	5		TRANSISTOR MOSFET N-CHAN E-MODE TO-237	17856	VN10KM
A6Q4	1854-0019	3	1	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
A6Q5	1853-0405	9	2	TRANSISTOR PNP SI PD=300MW FT=850MHZ	04713	2N4209
A6Q6	1853-0405	9		TRANSISTOR PNP SI PD=300MW FT=850MHZ	04713	2N4209
A6Q7	1855-0423	5		TRANSISTOR MOSFET N-CHAN E-MODE TO-237	17856	VN10KM
A6Q9	1854-0477	7		TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
A6Q10	1853-0281	9	3	TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
A6Q11	1854-0809	9	2	TRANSISTOR NPN 2N2369A SI TO-18 PD=360MW	28480	1854-0809
A6Q12	1854-0809	9		TRANSISTOR NPN 2N2369A SI TO-18 PD=360MW	28480	1854-0809
A6R4	0757-0466	7	1	RESISTOR 110K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1103-F
A6R5	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1001-F
A6R6	0757-1094	9	1	RESISTOR 1.47K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1471-F
A6R7	0698-3446	3		RESISTOR 383 1% .125W F TC=0±100	24546	CT4-1/8-T0-383R-F
A6R8	0698-7212	9		RESISTOR 100 1% .05W F TC=0±100	24546	C3-1/8-TO-100R-F
A6R9	0698-7260	7		RESISTOR 10K 1% .05W F TC=0±100	24546	C3-1/8-T0-1002-F
A6R10	0698-7267	4		RESISTOR 19.6K 1% .05W F TC=0±100	24546	C3-1/8-T0-1962-F
A6R11	0698-7283	4	2	RESISTOR 90.9K 1% .05W F TC=0±100	24546	C3-1/8-T0-9092-F
A6R12	2100-1738	9		RESISTOR-TRMR 10K 10% C TOP-ADJ 1-TRN	73138	82PR10K
A6R13	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A6R14	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1001-F
A6R15	0698-8469	0	9	RESISTOR 6.99K .1% .1W F TC=0+4	28480	0698-8469
A6R16	2100-3756	5	1	RESISTOR-TRMR 20 10% C SIDE-ADJ 17-TRN	28480	2100-3756
A6R17	0698-8469	0		RESISTOR 6.99K .1% .1W F TC=0+4	28480	0698-8469
A6R18	0698-8469	0		RESISTOR 6.99K .1% .1W F TC=0+4	28480	0698-8469
A6R19	0698-8469	0		RESISTOR 6.99K .1% .1W F TC=0+4	28480	0698-8469
A6R20	0699-0642	7	1	RESISTOR 10K .1% .1W F TC=0±5	28480	0699-0642
A6R21	2100-3757	6	3	RESISTOR-TRMR 100 10% C SIDE-ADJ 17-TRN	28480	2100-3757
A6R22	0699-0831	6	1	RESISTOR 9.95K .1% .1W F TC=0±5	28480	0699-0831
A6R23	0699-0830	5	2	RESISTOR 30.423K .1% .1W F TC=0±5	28480	0699-0830

See introduction to this section for ordering information.

*Indicates factory selected value.

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6R24	2100-3732	7	3	RESISTOR-TRMR 500 10% C SIDE-ADJ 17-TRN	28480	2100-3732
A6R25	0699-0830	5		RESISTOR 30.423K .1% .1W F TC=0±5	28480	0699-0830
A6R26	2100-3732	7		RESISTOR-TRMR 500 10% C SIDE-ADJ 17-TRN	28480	2100-3732
A6R27	0699-0829	2	1	RESISTOR 42.884K .1% .1W F TC=0±5	28480	0699-0829
A6R28	2100-0545	4	2	RESISTOR-TRMR 1K 10% C SIDE-ADJ 17-TRN	28480	2100-0545
A6R29	0699-0828	1	1	RESISTOR 82.541K .1% .1W F TC=0±5	28480	0699-0828
A6R30	2100-3759	8		RESISTOR-TRMR 2K 10% C SIDE-ADJ 17-TRN	28480	2100-3759
A6R31	0698-8469	0		RESISTOR 6.99K .1% .1W F TC=0+4	28480	0698-8469
A6R32	0698-8469	0		RESISTOR 6.99K .1% .1W F TC=0+4	28480	0698-8469
A6R33	0698-8469	0		RESISTOR 6.99K .1% .1W F TC=0+4	28480	0698-8469
A6R34	2100-3755	4	1	RESISTOR-TRMR 50 10% C SIDE-ADJ 17-TRN	28480	2100-3755
A6R35	0698-8469	0		RESISTOR 6.99K .1% .1W F TC=0+4	28480	0698-8469
A6R36	0698-8827	4		RESISTOR 1M 1% .125W F TC=0±100	28480	0698-8827
A6R37	2100-3750	9	2	RESISTOR-TRMR 20K 10% C SIDE-ADJ 17-TRN	28480	2100-3750
A6R38	0698-8827	4		RESISTOR 1M 1% .125W F TC=0±100	28480	0698-8827
A6R39	0699-0154	6	1	RESISTOR 7.2K .1% .125W F TC=0±25	28480	0699-0154
A6R40	0698-6867	8	1	RESISTOR 7.35K .25% .125W F TC=0±50	28480	0698-6867
A6R41	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A6R42	0698-3260	9	3	RESISTOR 464K 1% .125W F TC=0±100	28480	0698-3260
A6R43	0698-3150	6	3	RESISTOR 2.37K 1% .125W F TC=0±100	24546	CT4-1/8-T0-2371-F
A6R44	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A6R45	0698-3260	9		RESISTOR 464K 1% .125W F TC=0±100	28480	0698-3260
A6R46	0698-3150	6		RESISTOR 2.37K 1% .125W F TC=0±100	24546	CT4-1/8-T0-2371-F
A6R47	0698-7234	5		RESISTOR 825 1% .05W F TC=0±100	24546	C3-1/8-T0-825R-F
A6R48	0698-7234	5		RESISTOR 825 1% .05W F TC=0±100	24546	C3-1/8-T0-825R-F
A6R49	0698-7227	6	1	RESISTOR 422 1% .05W F TC=0±100	24546	C3-1/8-TO-422R-F
A6R50	0698-7219	6		RESISTOR 196 1% .05W F TC=0±100	24546	C3-1/8-TO-196R-F
A6R51	0698-7212	9		RESISTOR 100 1% .05W F TC=0±100	24546	C3-1/8-TO-100R-F
A6R52	0698-3150	6		RESISTOR 2.37K 1% .125W F TC=0±100	24546	CT4-1/8-T0-2371-F
A6R53	0698-3429	2	1	RESISTOR 19.6 1% .125W F TC=0±100	03888	PME55-1/8-T0-19R6-F
A6R54	0698-3453	2	3	RESISTOR 196K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1963-F
A6R55	0698-8827	4		RESISTOR 1M 1% .125W F TC=0±100	28480	0698-8827
A6R56	0698-3159	5		RESISTOR 26.1K 1% .125W F TC=0±100	24546	CT4-1/8-T0-2612-F
A6R57	0698-3266	5	1	RESISTOR 237K 1% .125W F TC=0±100	24546	CT4-1/8-T0-2373-F
A6R58	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1001-F
A6R59	0698-7236	7		RESISTOR 1K 1% .05W F TC=0±100	24546	C3-1/8-T0-1001-F
A6R60	0698-7277	6		RESISTOR 51.1K 1% .05W F TC=0±100	24546	C3-1/8-T0-5112-F
A6R61	0698-7277	6		RESISTOR 51.1K 1% .05W F TC=0±100	24546	C3-1/8-T0-5112-F
A6R62	0757-0458	7		RESISTOR 51.1K 1% .125W F TC=0±100	24546	CT4-1/8-T0-5112-F
A6R63	2100-2030	6		RESISTOR-TRMR 20K 10% C TOP-ADJ 1-TRN	73138	82PR20K
A6R64	0698-7260	7		RESISTOR 10K 1% .05W F TC=0±100	24546	C3-1/8-T0-1002-F
A6R65	0757-0440	7	2	RESISTOR 7.5K 1% .125W F TC=0±100	24546	CT4-1/8-T0-7501-F
A6R66	0698-7272	1	1	RESISTOR 31.6K 1% .05W F TC=0±100	24546	C3-1/8-T0-3162-F
A6R67	0698-7253	8		RESISTOR 5.11K 1% .05W F TC=0±100	24546	C3-1/8-T0-5111-F
A6R68	2100-2030	6		RESISTOR-TRMR 20K 10% C TOP-ADJ 1-TRN	73138	82PR20K
A6R69	2100-2030	6		RESISTOR-TRMR 20K 10% C TOP-ADJ 1-TRN	73138	82PR20K
A6R71	0698-7237	8	1	RESISTOR 1.1K 1% .05W F TC=0±100	24546	C3-1/8-T0-1101-F
A6R72	0698-7242	5		RESISTOR 1.78K 1% .05W F TC=0±100	24546	C3-1/8-T0-1781-F
A6R73	2100-2521	0	2	RESISTOR-TRMR 2K 10% C SIDE-ADJ 1-TRN	73138	82PAR2K
A6R74	2100-2521	0		RESISTOR-TRMR 2K 10% C SIDE-ADJ 1-TRN	73138	82PAR2K
A6R76	0698-7283	4		RESISTOR 90.9K 1% .05W F TC=0±100	24546	C3-1/8-T0-9092-F
A6R77	0698-7285	6	1	RESISTOR 110K 1% .05W F TC=0±100	24546	C3-1/8-T0-1103-F
A6R78	2100-2692	6	1	RESISTOR-TRMR 1M 20% C SIDE-ADJ 1-TRN	73138	82PAR1M
A6R80*	0698-7236	7	3	RESISTOR 1K 1% .05W F TC=0±100	24546	C3-1/8-T0-1001-F
A6R81	0698-7260	7		RESISTOR 10K 1% .05W F TC=0±100	24546	C3-1/8-T0-1002-F
A6R82	0698-7243	6		RESISTOR 1.96K 1% .05W F TC=0±100	24546	C3-1/8-T0-1961-F
A6R83	0698-7242	5		RESISTOR 1.78K 1% .05W F TC=0±100	24546	C3-1/8-T0-1781-F
A6R84	0698-7238	9		RESISTOR 1.21K 1% .05W F TC=0±100	24546	C3-1/8-T0-1211-F
A6R85	0698-7260	7		RESISTOR 10K 1% .05W F TC=0±100	24546	C3-1/8-T0-1002-F
A6R86	0698-7260	7		RESISTOR 10K 1% .05W F TC=0±100	24546	C3-1/8-T0-1002-F
A6R87	0698-7260	7		RESISTOR 10K 1% .05W F TC=0±100	24546	C3-1/8-T0-1002-F
A6TP1	1251-4672	4	10	CONNECTOR 10-PIN M POST TYPE	28480	1251-4672
A6TP2	1251-4672	4		CONNECTOR 10-PIN M POST TYPE	28480	1251-4672
A6TP3	1251-4672	4		CONNECTOR 10-PIN M POST TYPE	28480	1251-4672
A6TP4	1251-4672	4		CONNECTOR 10-PIN M POST TYPE	28480	1251-4672
A6TP5	1251-4672	4		CONNECTOR 10-PIN M POST TYPE	28480	1251-4672

See introduction to this section for ordering information.

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Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6TP6	1251-4672	4		CONNECTOR 10-PIN M POST TYPE	28480	1251-4672
A6TP7	1251-4672	4		CONNECTOR 10-PIN M POST TYPE	28480	1251-4672
A6TP8	1251-4672	4		CONNECTOR 10-PIN M POST TYPE	28480	1251-4672
A6TP9	1251-4672	4		CONNECTOR 10-PIN M POST TYPE	28480	1251-4672
A6TP10	1251-4672	4		CONNECTOR 10-PIN M POST TYPE	28480	1251-4672
A6U1	1826-0720	4	5	IC SWITCH ANLG QUAD 16-DIP-C PKG	06665	SW-02FQ
A6U2	1820-1211	8	1	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86AN
A6U3	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A6U4	1826-0720	4		IC SWITCH ANLG QUAD 16-DIP-C PKG	06665	SW-02FQ
A6U5	1826-1048	1	16	IC OP AMP PRCN 8-DIP-C PKG	06665	OP-07CZ
A6U6	1826-1048	1		IC OP AMP PRCN 8-DIP-C PKG	06665	OP-07CZ
A6U8	1820-1112	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A6U9	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A6U10	1826-1186	8		ANALOG SWITCH 4 SPST 16 -CERDIP	06665	SW-06GQ
A6U11	1826-1186	8		ANALOG SWITCH 4 SPST 16 -CERDIP	06665	SW-06GQ
A6U12	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A6U13	1820-2024	3	5	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A6U14	1826-1221	2		IC COMPARATOR PRCN 8-DIP-C PKG	28480	1826-1221
A6U15	1826-1048	1		IC OP AMP PRCN 8-DIP-C PKG	06665	OP-07CZ
A6U16	1820-1246	9	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS09N
A6U17	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A6U18	1826-0752	2		D/A 12-BIT 16-CBRZ/SDR CMOS	24355	AD7542BD
A6U19	1826-1048	1		IC OP AMP PRCN 8-DIP-C PKG	06665	OP-07CZ
A6U20	1826-1048	1		IC OP AMP PRCN 8-DIP-C PKG	06665	OP-07CZ
A6U21	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A6U22	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A6U23	1826-1221	2		IC COMPARATOR PRCN 8-DIP-C PKG	28480	1826-1221
A6U24	1826-0092	3		IC OP AMP GP DUAL TO-99 PKG	28480	1826-0092
A6U26	1826-0185	5	1	IC OP AMP SPCL TO-99 PKG	3L585	CA3080
A6U27	1826-0915	9	1	IC OP AMP LOW-BIAS-H-IMPD 8-DIP-C PKG	04713	MC34001BU
A6VR1	1902-3002	3		DIODE-ZNR 2.37V 5% DO-7 PD=.4W TC=-.074%	28480	1902-3002
A6W1	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
A6W4	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005

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Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A7	**83595-60068**	**4**	**1**	**BOARD ASSEMBLY-YTM DRIVER**	**28480**	**83595-60068**
A7C1	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A7C2	0160-3877	5	2	CAPACITOR-FXD 100PF ±20% 200VDC CER	28480	0160-3877
A7C3	0160-0162	5	1	CAPACITOR-FXD .022UF ±10% 200VDC POLYE	28480	0160-0162
A7C4	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A7C5	0160-3877	5		CAPACITOR-FXD 100PF ±20% 200VDC CER	28480	0160-3877
A7C6	0160-0574	3	3	CAPACITOR-FXD .022UF ±20% 100VDC CER	28480	0160-0574
A7C7	0180-0116	1	6	CAPACITOR-FXD 6.8UF±10% 35VDC TA	56289	150D685X9035B2
A7C8	0180-0116	1		CAPACITOR-FXD 6.8UF±10% 35VDC TA	56289	150D685X9035B2
A7C9	0180-2815	1		CAPACITOR-FXD 100UF±20% 10VDC TA	28480	0180-2815
A7C10	0180-0116	1		CAPACITOR-FXD 6.8UF±10% 35VDC TA	56289	150D685X9035B2
A7C11	0180-0228	6		CAPACITOR-FXD 22UF±10% 15VDC TA	56289	150D226X9015B2
A7C12	0160-0574	3		CAPACITOR-FXD .022UF ±20% 100VDC CER	28480	0160-0574
A7C13	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A7C14	0160-3878	6		CAPACITOR-FXD 1000PF ±20% 100VDC CER	28480	0160-3878
A7C15	0160-3878	6		CAPACITOR-FXD 1000PF ±20% 100VDC CER	28480	0160-3878
A7C16	0160-0575	4		CAPACITOR-FXD .047UF ±20% 50VDC CER	28480	0160-0575
A7C17	0180-2731	0	2	CAPACITOR-FXD 2.2UF±10% 20VDC TA	28480	0180-2731
A7C18	0160-3874	2		CAPACITOR-FXD 10PF ±.5PF 200VDC CER	28480	0160-3874
A7C19	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A7C20	0180-0228	6		CAPACITOR-FXD 22UF±10% 15VDC TA	56289	150D226X9015B2
A7C21	0180-2794	5	1	CAPACITOR-FXD 3.3UF±20% 35VDC TA	28480	0180-2794
A7CR1	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A7CR2	1901-0539	3	2	DIODE-SM SIG SCHOTTKY	28480	1901-0539
A7CR3	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-35	9N171	1N645
A7CR4	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-35	9N171	1N645
A7CR5	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-35	9N171	1N645
A7CR7	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A7CR8	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-35	9N171	1N645
A7CR9	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A7L1	9140-0137	1		INDUCTOR RF-CH-MLD 1MH 5%	28480	9140-0137
A7L2	9140-0137	1		INDUCTOR RF-CH-MLD 1MH 5%	28480	9140-0137
A7L3	08503-80001	9		COIL TOROID	28480	08503-80001
A7MP1				NOT ASSIGNED		
A7MP2	5040-6844	3	1	BOARD EXTRACTOR	28480	5040-6844
A7MP3	5000-9043	6		PIN	28480	5000-9043
A7MP4	1251-7204	4	1	CONNECTOR 20-PIN M DUAL INLINE	28480	1251-7204
A7MP5	1200-0173	5		INSULATOR-XSTR DAP-GL	28480	1200-0173
A7Q1	1853-0044	2	4	TRANSISTOR PNP SI TO-39 PD=1W FT=200MHZ	28480	1853-0044
A7Q2	1853-0044	2		TRANSISTOR PNP SI TO-39 PD=1W FT=200MHZ	28480	1853-0044
A7R1	0757-0443	0	1	RESISTOR 11K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1102-F
A7R2	0757-0420	3		RESISTOR 750 1% .125W F TC=0±100	24546	CT4-1/8-T0-751-F
A7R3	0757-0458	7		RESISTOR 51.1K 1% .125W F TC=0±100	24546	CT4-1/8-T0-5112-F
A7R4	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A7R5	0698-3449	6	1	RESISTOR 28.7K 1% .125W F TC=0±100	24546	CT4-1/8-T0-2872-F
A7R6	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0±100	24546	CT4-1/8-TO-1961-F
A7R7	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0±100	24546	CT4-1/8-TO-1961-F
A7R8	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A7R9	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A7R10	2100-3611	1		RESISTOR-TRMR 50K 10% C SIDE-ADJ 17-TRN	28480	2100-3611
A7R11	0757-0200	7	1	RESISTOR 5.62K 1% .125W F TC=0±100	24546	CT4-1/8-T0-5621-F
A7R12	2100-3611	1		RESISTOR-TRMR 50K 10% C SIDE-ADJ 17-TRN	28480	2100-3611
A7R13	0757-0447	4	1	RESISTOR 16.2K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1622-F
A7R14	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A7R15	0698-3260	9		RESISTOR 464K 1% .125W F TC=0±100	28480	0698-3260
A7R16	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1001-F
A7R17	0698-3457	6		RESISTOR 316K 1% .125W F TC=0±100	28480	0698-3457
A7R18	2100-3611	1		RESISTOR-TRMR 50K 10% C SIDE-ADJ 17-TRN	28480	2100-3611
A7R19	2100-3732	7		RESISTOR-TRMR 500 10% C SIDE-ADJ 17-TRN	28480	2100-3732
A7R20	0699-0796	2	1	RESISTOR 22.95K .1% .1W F TC=0+4	28480	0699-0796
A7R21	0698-6406	1	4	RESISTOR 8.54K .1% .1W F TC=0+4	28480	0698-6406
A7R22	2100-3749	6		RESISTOR-TRMR 5K 10% C SIDE-ADJ 17-TRN	28480	2100-3749
A7R23	0699-0800	9	1	RESISTOR 48.5K .1% .1W F TC=0+4	28480	0699-0800
A7R24	2100-3757	6		RESISTOR-TRMR 100 10% C SIDE-ADJ 17-TRN	28480	2100-3757
A7R25	0699-0801	0	1	RESISTOR 9.041K .1% .1W F TC=0+4	28480	0699-0801

See introduction to this section for ordering information.

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Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A7R26	0698-8960	6	1	RESISTOR 750K 1% .125W F TC=0±100	28480	0698-8960
A7R27	0698-8489	4	4	RESISTOR 15K .1% .1W F TC=0+4	28480	0698-8489
A7R28	0757-0444	1	2	RESISTOR 12.1K 1% .125W F TC=0±100	24546	CT4-1/8-TO-1212-F
A7R29	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A7R30	0757-0470	3	3	RESISTOR 162K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1623-F
A7R31	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A7R32	0757-0274	5	2	RESISTOR 1.21K 1% .125W F TC=0±100	24546	CT4-1/8-TO-1211-F
A7R33	0698-3453	2		RESISTOR 196K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1963-F
A7R40	0698-8489	4		RESISTOR 15K .1% .1W F TC=0+4	28480	0698-8489
A7R41	0698-6406	1		RESISTOR 8.54K .1% .1W F TC=0+4	28480	0698-6406
A7R42	2100-0544	3		RESISTOR-TRMR 100K 10% C SIDE-ADJ 17-TRN	28480	2100-0544
A7R43	2100-3611	1		RESISTOR-TRMR 50K 10% C SIDE-ADJ 17-TRN	28480	2100-3611
A7R44	0811-1037	6	2	RESISTOR 315 1% 3W PW TC=0±20	28480	0811-1037
A7R45	2100-3753	2		RESISTOR-TRMR 200K 10% C SIDE-ADJ 17-TRN	28480	2100-3753
A7R46	2100-3611	1		RESISTOR-TRMR 50K 10% C SIDE-ADJ 17-TRN	28480	2100-3611
A7R47	0757-0289	2		RESISTOR 13.3K 1% .125W F TC=0±100	19701	5033R-1/8-T0-1332-F
A7R48	0757-0440	7		RESISTOR 7.5K 1% .125W F TC=0±100	24546	CT4-1/8-T0-7501-F
A7R49	0698-6721	3	1	RESISTOR 19K 1% .125W F TC=0±25	28480	0698-6721
A7R50	0698-8827	4		RESISTOR 1M 1% .125W F TC=0±100	28480	0698-8827
A7R51	2100-0670	6		RESISTOR-TRMR 10K 10% C SIDE-ADJ 17-TRN	28480	2100-0670
A7R52	0698-6358	2	1	RESISTOR 100K .1% .125W F TC=0±25	28480	0698-6358
A7R53	0698-3159	5		RESISTOR 26.1K 1% .125W F TC=0±100	24546	CT4-1/8-T0-2612-F
A7R54	0698-8958	2	2	RESISTOR 511K 1% .125W F TC=0±100	28480	0698-8958
A7R55	2100-2517	4	2	RESISTOR-TRMR 50K 10% C SIDE-ADJ 1-TRN	73138	82PAR50K
A7R56	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1001-F
A7R57	0757-0290	5	2	RESISTOR 6.19K 1% .125W F TC=0±100	19701	5033R-1/8-T0-6191-F
A7R58	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A7R59	0811-1037	6		RESISTOR 315 1% 3W PW TC=0±20	28480	0811-1037
A7R60	0698-0084	9	4	RESISTOR 2.15K 1% .125W F TC=0±100	24546	CT4-1/8-T0-2151-F
A7R61	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0±100	24546	CT4-1/8-T0-2151-F
A7R62	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A7R63	0757-0444	1		RESISTOR 12.1K 1% .125W F TC=0±100	24546	CT4-1/8-TO-1212-F
A7R64	0698-6977	1	1	RESISTOR 30K .1% .125W F TC=0±25	28480	0698-6977
A7R65	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0±100	24546	CT4-1/8-T0-5111-F
A7R66	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0±100	24546	CT4-1/8-T0-5111-F
A7R67	0698-6362	8	1	RESISTOR 1K .1% .125W F TC=0±25	28480	0698-6362
A7R68	0698-8469	0		RESISTOR 6.99K .1% .1W F TC=0+4	28480	0698-8469
A7R72	0698-8959	3	1	RESISTOR 619K 1% .125W F TC=0±100	28480	0698-8959
A7R73	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A7R74	0757-0418	9	1	RESISTOR 619 1% .125W F TC=0±100	24546	CT4-1/8-T0-619R-F
A7S1	3101-0471	8	4	SWITCH-RKR DIP-RKR-ASSY 10-1A .05A 30VDC	28480	3101-0471
A7S2	3101-0471	8		SWITCH-RKR DIP-RKR-ASSY 10-1A .05A 30VDC	28480	3101-0471
A7TP1	1251-5618	0		CONNECTOR 8-PIN M POST TYPE	28480	1251-5618
A7TP2	1251-5618	0		CONNECTOR 8-PIN M POST TYPE	28480	1251-5618
A7TP3	1251-5618	0		CONNECTOR 8-PIN M POST TYPE	28480	1251-5618
A7TP4	1251-5618	0		CONNECTOR 8-PIN M POST TYPE	28480	1251-5618
A7TP5	1251-5618	0		CONNECTOR 8-PIN M POST TYPE	28480	1251-5618
A7TP6	1251-5618	0		CONNECTOR 8-PIN M POST TYPE	28480	1251-5618
A7TP7	1251-5618	0		CONNECTOR 8-PIN M POST TYPE	28480	1251-5618
A7TP8	1251-5618	0		CONNECTOR 8-PIN M POST TYPE	28480	1251-5618
A7TP9	0360-0535	0		TERMINAL-TEST POINT .330IN ABOVE	28480	0360-0535
A7U1	1810-0277	3	4	NETWORK-RES 10-SIP 2.2K OHM X 9	91637	CSC10A01-222G/MSP10A01-
A7U2	1810-0277	3		NETWORK-RES 10-SIP 2.2K OHM X 9	91637	CSC10A01-222G/MSP10A01-
A7U3	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A7U4	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A7U5	1826-0180	0		IC TIMER TTL MONO/ASTBL	18324	NE555N
A7U7	1820-1568	8	2	IC BFR TTL LS BUS QUAD	01295	SN74LS125AN
A7U8	1820-1144	6	2	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A7U9	1826-0720	4		IC SWITCH ANLG QUAD 16-DIP-C PKG	06665	SW-02FQ
A7U10	1826-0720	4		IC SWITCH ANLG QUAD 16-DIP-C PKG	06665	SW-02FQ
A7U11	1826-0753	3	2	IC OP AMP LOW-BIAS-H-IMPD QUAD 14-DIP-C	04713	MC34004BL
A7U12	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A7U13	1826-0752	2		D/A 12-BIT 16-CBRZ/SDR CMOS	24355	AD7542BD
A7U14	1826-1048	1		IC OP AMP PRCN 8-DIP-C PKG	06665	OP-07CZ
A7U15	1826-1048	1		IC OP AMP PRCN 8-DIP-C PKG	06665	OP-07CZ
A7U16	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A7U17	1826-0752	2		D/A 12-BIT 16-CBRZ/SDR CMOS	24355	AD7542BD
A7U18	1826-1048	1		IC OP AMP PRCN 8-DIP-C PKG	06665	OP-07CZ
A7U19	1826-1349	5	1	IC OP AMP GP 8-DIP-C PKG	02187	OP-02CZ
A7U20	1826-0758	8	2	IC MULTIPLIER ANLG TO-100 PKG	28480	1826-0758
A7U21	1826-1048	1		IC OP AMP PRCN 8-DIP-C PKG	06665	OP-07CZ
A7U22	1826-1048	1		IC OP AMP PRCN 8-DIP-C PKG	06665	OP-07CZ
A7VR1	1902-0197	1	2	DIODE-ZNR 82V 5% PD=1W IR=5UA	28480	1902-0197
A7XA1	1200-1257	8	1	SOCKET-IC 20-CONT DIP DIP-SLDR	00779	2-641612-2

See introduction to this section for ordering information.

*Indicates factory selected value.

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8	**83595-60070**	**8**	**1**	**BOARD ASSEMBLY-YO DRIVER**	**28480**	**83595-60070**
A8C1	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A8C2	0160-4389	6	2	CAPACITOR-FXD 100PF ±5PF 200VDC CER	28480	0160-4389
A8C3	0160-0161	4	1	CAPACITOR-FXD .01UF ±10% 200VDC POLYE	28480	0160-0161
A8C4	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A8C5	0160-4389	6		CAPACITOR-FXD 100PF ±5PF 200VDC CER	28480	0160-4389
A8C6	0160-0575	4		CAPACITOR-FXD .047UF ±20% 50VDC CER	28480	0160-0575
A8C7	0180-0116	1		CAPACITOR-FXD 6.8UF±10% 35VDC TA	56289	150D685X9035B2
A8C8	0180-0116	1		CAPACITOR-FXD 6.8UF±10% 35VDC TA	56289	150D685X9035B2
A8C9	0180-2815	1		CAPACITOR-FXD 100UF±20% 10VDC TA	28480	0180-2815
A8C10	0180-0116	1		CAPACITOR-FXD 6.8UF±10% 35VDC TA	56289	150D685X9035B2
A8C11	0180-0228	6		CAPACITOR-FXD 22UF±10% 15VDC TA	56289	150D226X9015B2
A8C12	0160-0574	3		CAPACITOR-FXD .022UF ±20% 100VDC CER	28480	0160-0574
A8C13	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A8C14	0160-3874	2		CAPACITOR-FXD 10PF ±.5PF 200VDC CER	28480	0160-3874
A8C15	0160-3878	6		CAPACITOR-FXD 1000PF ±20% 100VDC CER	28480	0160-3878
A8C16	0180-3020	2	1	CAPACITOR-FXD 120UF±10% 50VDC TA	28480	0180-3020
A8C17	0180-0228	6		CAPACITOR-FXD 22UF±10% 15VDC TA	56289	150D226X9015B2
A8C18	0160-4084	8		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-4084
A8C19	0160-3878	6		CAPACITOR-FXD 1000PF ±20% 100VDC CER	28480	0160-3878
A8C20	0180-2731	0		CAPACITOR-FXD 2.2UF±10% 20VDC TA	28480	0180-2731
A8C21	0180-2186	9	1	CAPACITOR-FXD 300UF±20% 30VDC TA	28480	0180-2186
A8C22	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A8C23	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
A8C24	0160-3878	6		CAPACITOR-FXD 1000PF ±20% 100VDC CER	28480	0160-3878
A8C25	0160-4801	7	1	CAPACITOR-FXD 100PF ±5% 100VDC CER	28480	0160-4801
A8CR1	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A8CR2	1901-0539	3		DIODE-SM SIG SCHOTTKY	28480	1901-0539
A8CR4	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-35	9N171	1N645
A8CR5	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-35	9N171	1N645
A8CR6	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-35	9N171	1N645
A8CR7	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A8CR8	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-35	9N171	1N645
A8CR9	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-35	9N171	1N645
A8K1	0490-0916	6		RELAY-REED 1A 500MA 100VDC 5VDC-COIL	28480	0490-0916
A8L1	9140-0137	1		INDUCTOR RF-CH-MLD 1MH 5%	28480	9140-0137
A8L2	9140-0137	1		INDUCTOR RF-CH-MLD 1MH 5%	28480	9140-0137
A8L3	08503-80001	9		COIL TOROID	28480	08503-80001
A8MP1				NOT ASSIGNED		
A8MP2	5040-6846	5	1	BOARD EXTRACTOR	28480	5040-6846
A8MP3	5000-9073	2	1	PIN	28480	5000-9073
A8MP4	1251-7203	3	1	CONNECTOR 8-PIN M DUAL INLINE	28480	1251-7203
A8MP5	1200-0173	5		INSULATOR-XSTR DAP-GL	28480	1200-0173
A8Q1	1853-0281	9		TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
A8Q2	1853-0281	9		TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
A8Q3	1853-0044	2		TRANSISTOR PNP SI TO-39 PD=1W FT=200MHZ	28480	1853-0044
A8Q4	1853-0044	2		TRANSISTOR PNP SI TO-39 PD=1W FT=200MHZ	28480	1853-0044
A8R1	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A8R2	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0±100	24546	CT4-1/8-TO-1961-F
A8R3	0757-0458	7		RESISTOR 51.1K 1% .125W F TC=0±100	24546	CT4-1/8-T0-5112-F
A8R4	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A8R5	0757-0462	3	1	RESISTOR 75K 1% .125W F TC=0±100	24546	CT4-1/8-T0-7502-F
A8R6	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0±100	24546	CT4-1/8-TO-1961-F
A8R7	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0±100	24546	CT4-1/8-TO-1961-F
A8R8	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A8R9	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A8R10	2100-0670	6		RESISTOR-TRMR 10K 10% C SIDE-ADJ 17-TRN	28480	2100-0670
A8R11	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0±100	24546	CT4-1/8-T0-4641-F
A8R12	2100-3752	1	1	RESISTOR-TRMR 500K 10% C SIDE-ADJ 17-TRN	28480	2100-3752
A8R13	0757-0460	1	1	RESISTOR 61.9K 1% .125W F TC=0±100	24546	CT4-1/8-T0-6192-F
A8R14	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A8R15	0698-3452	1	1	RESISTOR 147K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1473-F
A8R16	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1001-F
A8R17	0698-3456	5	1	RESISTOR 287K 1% .125W F TC=0±100	24546	CT4-1/8-T0-2873-F
A8R18	2100-3750	9		RESISTOR-TRMR 20K 10% C SIDE-ADJ 17-TRN	28480	2100-3750
A8R19	2100-3757	6		RESISTOR-TRMR 100 10% C SIDE-ADJ 17-TRN	28480	2100-3757
A8R20	0699-0797	3	1	RESISTOR 7.65K .1% .1W F TC=0+4	28480	0699-0797

See introduction to this section for ordering information.

*Indicates factory selected value.

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8R21	0698-6406	1		RESISTOR 8.54K .1% .1W F TC=0+4	28480	0698-6406
A8R22	2100-0545	4		RESISTOR-TRMR 1K 10% C SIDE-ADJ 17-TRN	28480	2100-0545
A8R23	0699-0799	5	1	RESISTOR 21.1K .1% .1W F TC=0+4	28480	0699-0799
A8R24	2100-3758	7	1	RESISTOR-TRMR 200 10% C SIDE-ADJ 17-TRN	28480	2100-3758
A8R25	0699-0798	4	1	RESISTOR 11.475K .1% .1W F TC=0+4	28480	0699-0798
A8R26	0757-0470	3		RESISTOR 162K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1623-F
A8R27	0698-8489	4		RESISTOR 15K .1% .1W F TC=0+4	28480	0698-8489
A8R28	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A8R29	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A8R30	0757-0470	3		RESISTOR 162K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1623-F
A8R31	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A8R32	0757-0274	5		RESISTOR 1.21K 1% .125W F TC=0±100	24546	CT4-1/8-TO-1211-F
A8R33	0698-3453	2		RESISTOR 196K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1963-F
A8R40	0698-8489	4		RESISTOR 15K .1% .1W F TC=0+4	28480	0698-8489
A8R41	0698-6406	1		RESISTOR 8.54K .1% .1W F TC=0+4	28480	0698-6406
A8R42	0698-8472	5	1	RESISTOR 2.653K .1% .1W F TC=0±5	28480	0698-8472
A8R43	0698-6409	4	1	RESISTOR 19.68K .1% .1W F TC=0+4	28480	0698-6409
A8R44	2100-3161	6	1	RESISTOR-TRMR 20K 10% C SIDE-ADJ 17-TRN	73138	89PR20K
A8R45	0699-0518	6	1	RESISTOR 11.489K .1% .1W F TC=0+4	28480	0699-0518
A8R46	0757-0416	7	3	RESISTOR 511 1% .125W F TC=0±100	24546	CT4-1/8-T0-511R-F
A8R47	0757-0416	7		RESISTOR 511 1% .125W F TC=0±100	24546	CT4-1/8-T0-511R-F
A8R48	0757-0416	7		RESISTOR 511 1% .125W F TC=0±100	24546	CT4-1/8-T0-511R-F
A8R49	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0±100	24546	CT4-1/8-T0-5111-F
A8R50	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0±100	24546	CT4-1/8-T0-5111-F
A8R51	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0±100	24546	CT4-1/8-T0-5111-F
A8R52	0757-0180	2	1	RESISTOR 31.6 1% .125W F TC=0±100	28480	0757-0180
A8R53	0698-3159	5		RESISTOR 26.1K 1% .125W F TC=0±100	24546	CT4-1/8-T0-2612-F
A8R54	0698-8958	2		RESISTOR 511K 1% .125W F TC=0±100	28480	0698-8958
A8R55	2100-2517	4		RESISTOR-TRMR 50K 10% C SIDE-ADJ 1-TRN	73138	82PAR50K
A8R56	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0±100	24546	CT4-1/8-T0-5111-F
A8R57	0757-0465	6		RESISTOR 100K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1003-F
A8R58	0698-3457	6		RESISTOR 316K 1% .125W F TC=0±100	28480	0698-3457
A8R59	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A8R60	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0±100	24546	CT4-1/8-T0-2151-F
A8R61	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0±100	24546	CT4-1/8-T0-2151-F
A8R62	0698-3455	4	1	RESISTOR 261K 1% .125W F TC=0±100	24546	CT4-1/8-T0-2613-F
A8R63	0698-3152	8	1	RESISTOR 3.48K 1% .125W F TC=0±100	24546	CT4-1/8-T0-3481-F
A8R64	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1001-F
A8R65	0698-3156	2		RESISTOR 14.7K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1472-F
A8R66	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	CT4-1/8-T0-1002-F
A8R67	0757-0290	5		RESISTOR 6.19K 1% .125W F TC=0±100	19701	5033R-1/8-T0-6191-F
A8R70	0698-7220	9	2	RESISTOR 215 1% .05W F TC=0±100	24546	C3-1/8-TO-215R-F
A8R71	0698-7220	9		RESISTOR 215 1% .05W F TC=0±100	24546	C3-1/8-TO-215R-F
A8S1	3101-0471	8		SWITCH-RKR DIP-RKR-ASSY 10-1A .05A 30VDC	28480	3101-0471
A8S2	3101-0471	8		SWITCH-RKR DIP-RKR-ASSY 10-1A .05A 30VDC	28480	3101-0471
A8TP1	1251-5925	2	12	CONNECTOR 12-PIN M POST TYPE	28480	1251-5925
A8TP2	1251-5925	2		CONNECTOR 12-PIN M POST TYPE	28480	1251-5925
A8TP3	1251-5925	2		CONNECTOR 12-PIN M POST TYPE	28480	1251-5925
A8TP4	1251-5925	2		CONNECTOR 12-PIN M POST TYPE	28480	1251-5925
A8TP5	1251-5925	2		CONNECTOR 12-PIN M POST TYPE	28480	1251-5925
A8TP6	1251-5925	2		CONNECTOR 12-PIN M POST TYPE	28480	1251-5925
A8TP7	1251-5925	2		CONNECTOR 12-PIN M POST TYPE	28480	1251-5925
A8TP8	1251-5925	2		CONNECTOR 12-PIN M POST TYPE	28480	1251-5925
A8TP9	1251-5925	2		CONNECTOR 12-PIN M POST TYPE	28480	1251-5925
A8TP10	1251-5925	2		CONNECTOR 12-PIN M POST TYPE	28480	1251-5925
A8TP11	1251-5925	2		CONNECTOR 12-PIN M POST TYPE	28480	1251-5925
A8TP12	1251-5925	2		CONNECTOR 12-PIN M POST TYPE	28480	1251-5925
A8U1	1810-0277	3		NETWORK-RES 10-SIP 2.2K OHM X 9	91637	CSC10A01-222G/MSP10A01-
A8U2	1810-0277	3		NETWORK-RES 10-SIP 2.2K OHM X 9	91637	CSC10A01-222G/MSP10A01-
A8U3	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A8U4	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A8U5	1826-1048	1		IC OP AMP PRCN 8-DIP-C PKG	06665	OP-07CZ
A8U6	1826-0476	7		IC SWITCH ANLG 8-DIP-P PKG	01295	TL601CP
A8U7	1820-1568	8		IC BFR TTL LS BUS QUAD	01295	SN74LS125AN
A8U8	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A8U9	1826-0180	0		IC TIMER TTL MONO/ASTBL	18324	NE555N
A8U10	1826-0753	3		IC OP AMP LOW-BIAS-H-IMPD QUAD 14-DIP-C	04713	MC34004BL

See introduction to this section for ordering information.

*Indicates factory selected value.

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8U11	1826-1048	1		IC OP AMP PRCN 8-DIP-C PKG	06665	OP-07CZ
A8U12	1826-0758	8		IC MULTIPLIER ANLG TO-100 PKG	28480	1826-0758
A8U13	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A8U14	1826-0752	2		D/A 12-BIT 16-CBRZ/SDR CMOS	24355	AD7542BD
A8U15	1826-1048	1		IC OP AMP PRCN 8-DIP-C PKG	06665	OP-07CZ
A8U16	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A8U17	1826-0752	2		D/A 12-BIT 16-CBRZ/SDR CMOS	24355	AD7542BD
A8U18	1826-1048	1		IC OP AMP PRCN 8-DIP-C PKG	06665	OP-07CZ
A8U19	1826-0720	4		IC SWITCH ANLG QUAD 16-DIP-C PKG	06665	SW-02FQ
A8U20	1826-1048	1		IC OP AMP PRCN 8-DIP-C PKG	06665	OP-07CZ
A8U21	1826-1048	1		IC OP AMP PRCN 8-DIP-C PKG	06665	OP-07CZ
A8VR1	1902-0197	1		DIODE-ZNR 82V 5% PD=1W IR=5UA	28480	1902-0197
A8VR2	1902-0625	0	3	DIODE-ZNR 1N829 6.2V 5% DO-7 PD=.25W	04713	1N829
A8VR3	1902-0625	0		DIODE-ZNR 1N829 6.2V 5% DO-7 PD=.25W	04713	1N829
A8VR4	1902-0625	0		DIODE-ZNR 1N829 6.2V 5% DO-7 PD=.25W	04713	1N829
A8VR5	1902-3070	5		DIODE-ZNR 4.22V 5% DO-35 PD=.4W	28480	1902-3070
A8XA1	1200-0455	6	1	SOCKET-IC 8-CONT DIP-SLDR	28480	1200-0455

See introduction to this section for ordering information.

*Indicates factory selected value.

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A9	**83525-60010**	2	1	**BOARD ASSEMBLY-TRANSISTOR HEAT SINK**	**28480**	**83525-60010**
A9C1	0180-0291	3	1	CAPACITOR-FXD 1UF ± 10% 35VDC TA	56289	150D105X9035A2
A9C2	0180-1735	2	1	CAPACITOR-FXD .22UF ± 10% 35VDC TA	56289	150D224X9035A2
A9MP1	0380-0745	6	8	STANDOFF-RVT-ON .187-IN-LG 6-32-THD	28480	0380-0745
A9MP2	0380-0322	5	3	SPACER-RVT-ON .062-IN-LG .152-IN-ID	28480	0380-0322
A9MP3	1251-2313	6	6	CONNECTOR-SGL CONT SKT .04-IN-BSC-SZ RND	28480	1251-2313
A9MP4	7121-4611	2		LBL IN MADE USA	28480	7121-4611
A10	**83595-60078**	6	1	**BOARD ASSEMBLY-MOTHER**	**28480**	**83595-60078**
A10C1	0160-3879	7		CAPACITOR-FXD .01UF ± 20% 100VDC CER	28480	0160-3879
A10C2	0160-3879	7		CAPACITOR-FXD .01UF ± 20% 100VDC CER	28480	0160-3879
A10C3	0160-3879	7		CAPACITOR-FXD .01UF ± 20% 100VDC CER	28480	0160-3879
A10C4	0160-3879	7		CAPACITOR-FXD .01UF ± 20% 100VDC CER	28480	0160-3879
A10C5	0160-3879	7		CAPACITOR-FXD .01UF ± 20% 100VDC CER	28480	0160-3879
A10C6	0160-3879	7		CAPACITOR-FXD .01UF ± 20% 100VDC CER	28480	0160-3879
A10C7	0160-3879	7		CAPACITOR-FXD .01UF ± 20% 100VDC CER	28480	0160-3879
A10CR1	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-35	9N171	1N645
A10J1	1251-5926	3		CONNECTOR 50-PIN M POST TYPE	28480	1251-5926
A10J2	1251-6952	7	1	CONN-POST TYPE 100-PIN-SPCG 26-CONT	28480	1251-6952
A10J3	1251-6343	0	1	CONNECTOR 18-PIN M POST TYPE	28480	1251-6343
A10J4	1200-1205	6	2	SOCKET-IC 16-CONT DIP DIP-SLDR	00779	2-641610-2
A10J5	1200-1205	6		SOCKET-IC 16-CONT DIP DIP-SLDR	00779	2-641610-2
A10J6	1250-0257	1	1	CONNECTOR-RF SMB M PC 50-OHM	28480	1250-0257
A10MP1				NOT ASSIGNED		
A10MP2	1251-1115	4	5	POLARIZING KEY-PC EDGE CONN	28480	1251-1115
A10MP3	7121-4611	2		LBL IN MADE USA	28480	7121-4611
A10R1	0698-8812	7	1	RESISTOR 1 1% .125W F TC=0±100	28480	0698-8812
A10XA3	1251-1365	6	6	CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A10XA4	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A10XA5	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A10XA6	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A10XA7	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A10XA8	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A10XA9	1251-0472	4	1	CONNECTOR-PC EDGE 6-CONT/ROW 2-ROWS	28480	1251-0472
A11	**86222-60007**	7	1	**CAVITY OSCILLATOR**	**28480**	**86222-60007**
A11C1	0180-2216	6	1	CAPACITOR-FXD 350UF +75-10% 16VDC AL	56289	30D357G016DH2
A11C2	0180-2144	9	1	CAPACITOR-FXD 200UF +75-10% 25VDC AL	56289	30D207G025DH9
A12	**83592-60065**	8	1	**SYTM REPLACEMENT KIT** LOWER LEVEL PARTS ARE NOT AVAILABLE SEPARATELY)	**28480**	**83592-60066**
A12	83592-60066	9	1	RESTORED SYTM REPLACEMENT KIT	28480	83592-60066
A13	**83592-60096**	5	1	**2.3-7.0 GHZ YO REPLACEMENT KIT** (LOWER LEVEL PARTS ARE NOT AVAILABLE SEPARATELY	**28480**	**83592-60096**
A13	83592-60097	6	1	RESTORED 2.3-7.0GHZ YO REPLACEMENT KIT	28480	83592-60097
A14	**83595-60075**	3	1	**POWER AMPLIFIER REPLACEMENT KIT** (LOWER LEVEL PARTS ARE NOT AVAILABLE SEPARATELY)	**28480**	**83595-60075**
A14	83595-60076	4	1	RESTORED POWER AMP REPLACEMENT KIT	28480	83595-60076
A15	**5086-7238**	7	1	**DC RETURN**	**28480**	**5086-7238**
A16	**5086-7339**	8	1	**MODULATOR/SPLITTER** (LOWER LEVEL PARTS ARE NOT AVAILABLE SEPARATELY)	**28480**	**5086-7339**
A16	5086-6339	7	1	RESTORED MODULATOR/SPLITTER	28480	5086-6339
A17	**5086-7217**	2	1	**AMPLIFIER .01-2.4GHZ**	**28480**	**5086-7217**
A17	5086-6217	0	1	RESTORED AMPLIFIER .01-2.4 GHZ	28480	5086-6217
A18	**5086-7219**	4	1	**MODULATOR MIXER**	**28480**	**5086-7219**
A18	5086-6219	2	1	RESTORED MODULATOR MIXER	28480	5086-6219

See introduction to this section for ordering information.

*Indicates factory selected value.

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
AT1	0960-0638	6	1	ISOLATOR-2.0-7.0 GHZ	28480	0960-0638
CR1	86290-60045	5	1	LBHCD DETECTOR	28480	6290-6004
CR2	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
CR3	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
DC1	5086-7220	7	1	DIRECTIONAL DETECTOR	28480	5086-7220
DC2	0955-0125	5	1	DIRECTIONAL COUPLER .01-26.5 GHZ	28480	0955-0125
E1	5040-0345	7	2	INSULATOR:CONNECTOR	28480	5040-0345
E2	5040-0345	7	2	INSULATOR:CONNECTOR	28480	5040-0345
J1	5061-5386	0	2	CONNECTOR ASSEMBLY TYPE-N	28480	5061-5386
J2	1250-0118	3	3	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0118
J3	5061-5386	0	2	CONNECTOR ASSEMBLY TYPE-N	28480	5061-5386
J4	1250-0118	3	3	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0118
J5	1250-0118	3	3	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0118
R1	0811-3573	9	1	RESISTOR-MATCHED SET WIREWOUND CHASSIS	28480	0811-3573

See introduction to this section for ordering information.

*Indicates factory selected value.

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				CABLES		
W1	83592-20045	0	1	CABLE-RF COUPLER/OUTPUT	28480	83592-20045
W2	83592-60021	6	1	CABLE COAX EXT/MTR ALC	28480	83592-60021
W3	83592-60025	0	1	CABLE ASSEMBLY RIBBON FRONT PANEL	28480	83592-60025
W4	83592-60018	1	1	CABLE ASSEMBLY RIBBON RF SECTION	28480	83592-60018
W5	83592-60017	0	1	CABLE COAX SQUARE WAVE IN	28480	83592-60017
W6	83592-60013	6	1	CABLE COAX PULSE MOD	28480	83592-60013
W7	83525-60029	3	1	CABLE COAX VTUNE	28480	83525-60029
W8	83592-60012	5	1	CABLE COAX, GREY, DETECTOR	28480	83592-60012
W9	83592-60019	2	2	CABLE COAX, BLUE, FM	28480	83592-60019
W10	83592-60016	9	1	CABLE COAX, PURPLE, INT DET 0	28480	83592-60016
W11	83592-60020	5	1	CABLE COAX, GREEN, FM IN	28480	83592-60020
W12	83592-60011	4	1	CABLE COAX, BROWN, AM IN	28480	83592-60011
W13	83592-60014	7	1	CABLE COAX, YELLOW, MOD 1	28480	83592-60014
W14	83592-60019	2		CABLE COAX, RIBBON, RF SECTION	28480	83592-60019
W15	83592-20047	2	1	CABLE-RF DC2/YTM	28480	83592-20047
W16	83592-20039	2	1	CABLE-RF AT1/YTM	28480	83592-20039
W17	83592-20038	1	1	CABLE-RF POWER AMPLIFIER/AT1	28480	83592-20038
W18	83592-20034	7	1	CABLE-RF DET/DCB	28480	83592-20034
W19	83592-20044	9	1	CABLE-RF LAMP/DETECTOR	28480	83592-20044
W20	83592-20042	7	1	CABLE-RF A16/A14	28480	83592-20042
W21	83592-20041	6	1	CABLE-RF A16/A18	28480	83592-20041
W22	83592-20030	3	1	CABLE-RF A11/A18	28480	83592-20030
W23	83592-20031	4	1	CABLE-RF A18/A17	28480	83592-20031
W24	83592-20035	8	1	CABLE-RF A15/A12	28480	83592-20035
W25	83592-20036	9	1	CABLE-RF A13/A16	28480	83592-20036
W26	83592-20043	8	1	CABLE-RF A16/J3 AUX OUTPUT	28480	83592-20043
W27	83592-60010	3	1	WIRING HARNESS, RF SECTION	28480	83592-60010
W28	83525-60066	8	1	CABLE ASSEMBLY POWER SUPPLY	28480	83525-60066
W29	83525-60056	6	1	CABLE ASSEMBLY RIBBON REAR CONNECTOR	28480	83525-60056

See introduction to this section for ordering information.

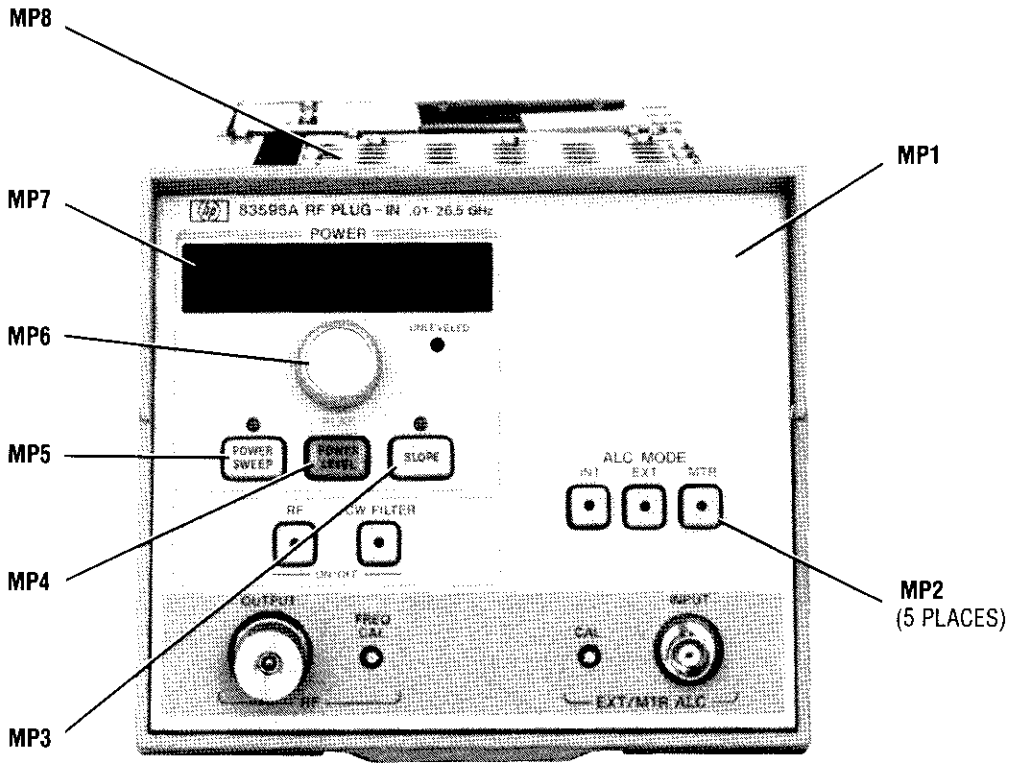
*Indicates factory selected value.

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				OPTION 002		
A19	83592-60019	2	1	ATTENUATOR 55DB	28480	83592-60019
A19MP1	83592-00010	7	1	BRACKET ATTENUATOR	28480	83592-00010
W15	83592-20048	3	1	CABLE RF SYTF/COUPLER	28480	83592-20048
W30	83595-20014	6	1	CABLE RF ATTENUATOR/FRONT OUT	28480	83595-20014
W31	83592-20029	0	1	CABLE RF COUPLER/ATTENUATOR	28480	83592-20029
				OPTION 004		
MP35	83592-20062	1	1	PLUG BUTTON DOME	28480	83592-20062
MP36	83592-20063	2	1	PLUG BUTTON DOME	28480	83592-20063
W2	83592-60024	9	1	CABLE ALC R/SMB	28480	83592-60024
W15	83592-20048	3	1	CABLE RF+SYTF/COUPLER	28480	83592-20048
W32	83595-20074	8	1	CABLE RF COUPLER/REAR OUT	28480	83595-20074
				OPTION 002 AND 004 INCLUDES ALL OPTION 002 AND 004 PARTS, IN ADDITION TO THE FOLLOWING:		
W33	83592-20051	8	1	CABLE RF-ATTENUATOR/REAR OUT	28480	83592-20051

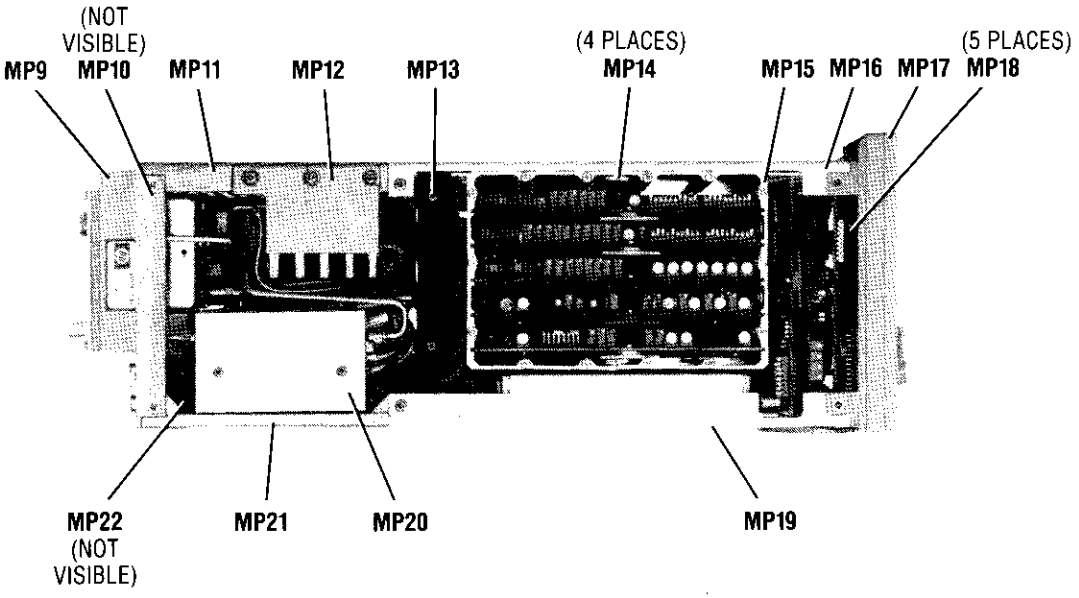
See introduction to this section for ordering information.

*Indicates factory selected value.



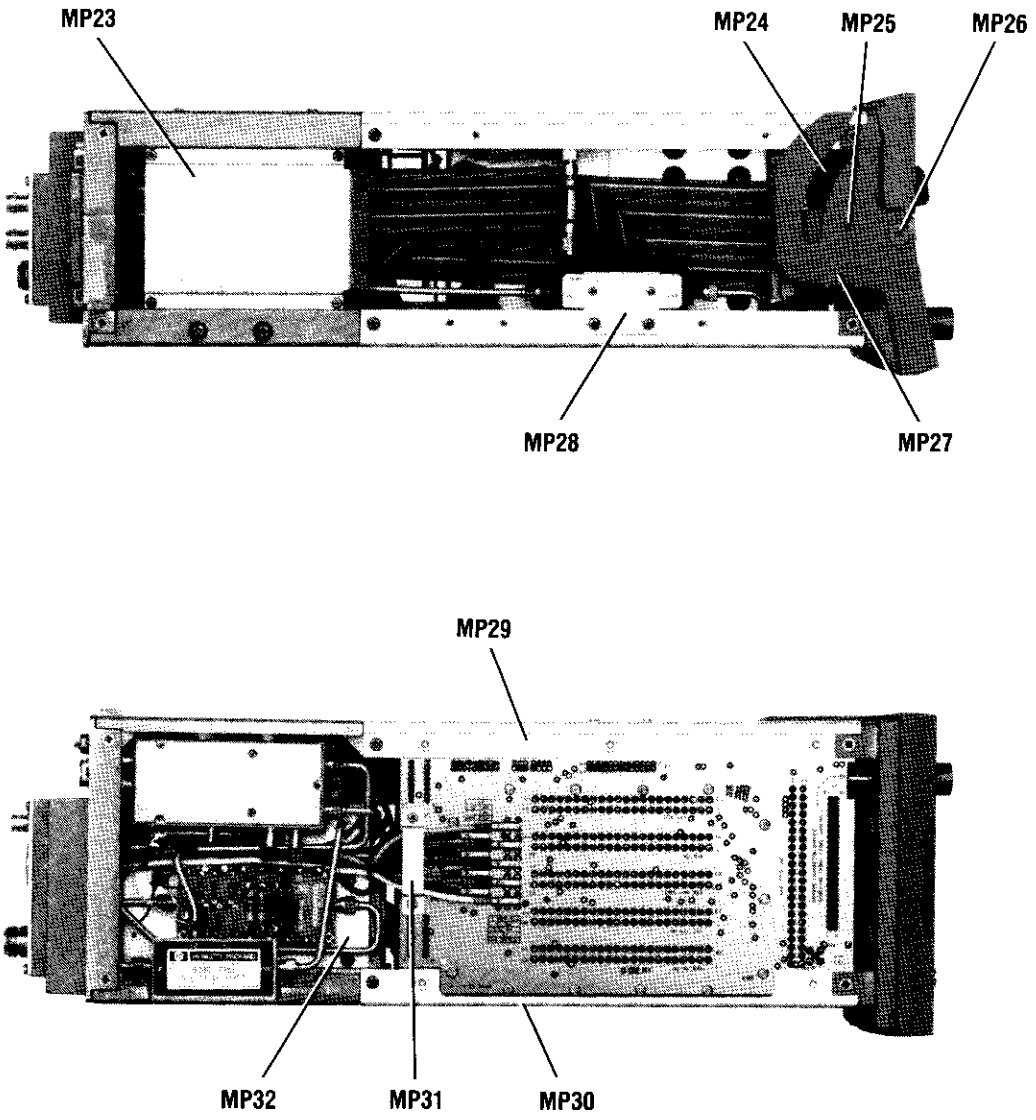
Item	HP Part Number	CD	Qty	Description	Mfr. Code	Manufacturer's Part Number
MP1	83592-00024	3	1	FRONT PANEL - DRESS (STD AND OPTION 002)	28480	83592-00024
MP2	5041-0285	6	5	KEY - CAP LITE	28480	5041-0285
MP3	5041-1926	4	1	KEY - CAP SLOPE	28480	5041-1926
MP4	5041-1924	2	1	KEY - CAP POWER LEVEL	28480	5041-192424
MP5	5041-1925	3	1	KEY - CAP POWER SWEEP	28480	5041-1925
MP6	0370-3023	8	1	KNOB - ¾ JACK .25-IND-ID	28480	0370-3023
MP7	83522-20028	5	1	WINDOW - DISPLAY	28480	83522-20028
MP8	83525-00005	9	1	COVER PC	28480	83525-00005

Figure 6-1. Major Mechanical Parts (1 of 4)



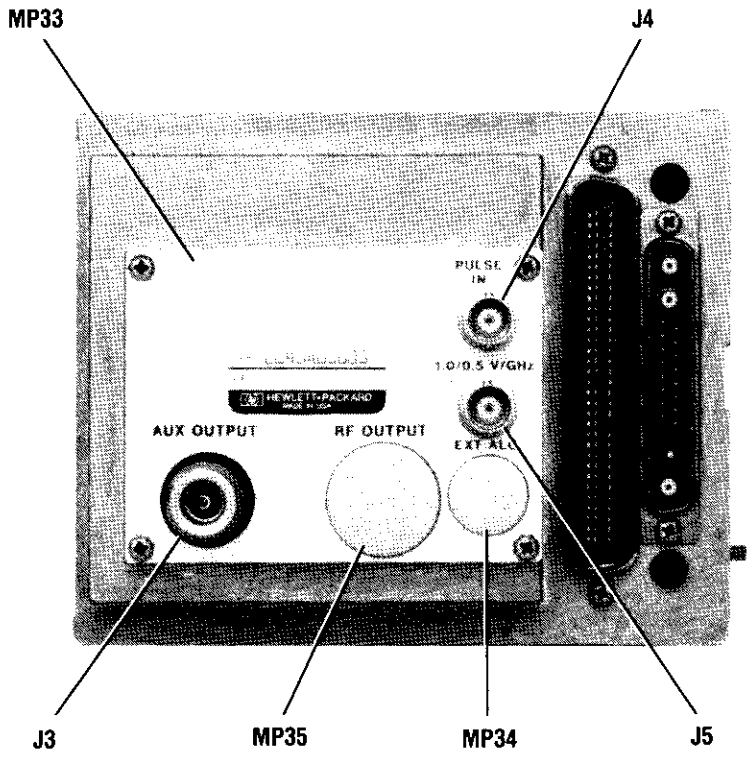
Item	HP Part Number	CD	Qty	Description	Mfr. Code	Manufacturer's Part Number
MP9	0050-2032	9	1	CASTING - AL FRAME (RR)	28480	0050-2032
MP10	0050-2067	0	1	CASTING - AL OSCILLATOR BRACKET	28480	0050-2067
MP11	0050-2069	2	1	CASTING - AL HEAT SINK RF	28480	0050-2069
MP12	0050-2068	1	1	CASTING - AL HEAT SINK	28480	0050-2068
MP13	83525-20036	8	1	CASTING - AL TRANSISTOR HEAT SINK	28480	83525-20036
MP14	1400-1095	6	1	CLIP - FASTENER .400 × .300 × .090 HI; BE	28480	1400-1095
MP15	83525-20070	0	1	SHIELD ASSEMBLY (CARD CAGE)	28480	83525-20070
MP16	83592-20016	5	1	SIDERAIL - UPPER RIGHT	28480	83592-20016
MP17	83545-20081	7	1	CASTING FRONT	28480	83545-20081
MP18	0510-1267	6	5	RETAINER PUSH-ON KB-TO-SHFT EXT	28480	0510-1267
MP19	83592-20017	6	1	SIDERAIL - UPPER LEFT	28480	83592-20017
MP20	83592-20008	3	1	SHIELD ISOLATOR	28480	83592-20008
MP21	0050-2066	9	1	CASTING - AL HEAT SINK RF	28480	0050-2066
MP22	83592-20006	1	1	BRACKET ISOLATOR	28480	83592-20006
MP23	83592-20013	1	0	BRACKET DET/DCB	28480	83592-20013

Figure 6-1. Major Mechanical Parts (2 of 4)



Item	HP Part Number	CD	Qty	Description	Mfr. Code	Manufacturer's Part Number
MP24	83525-00010	6	1	GUARD	28480	83525-00010
MP25	1460-1851	8	1	SPACER WIREFORM MUW BLK OXD	28480	1460-1851
MP26	1480-0337	5	1	PIN-ROLL 0.094-IN-DIA, 0.188-IN-LG-STL	28480	1480-0337
MP27	83525-20069	7	1	LATCH - SCREW	28480	83525-20069
MP28	83525-20040	4	1	LATCH	28480	83525-20040
MP29	83592-00009	4	1	BRACKET COUPLER	28480	83592-00009
MP30	83592-20018	7	1	SIDERAIL - LOWER LEFT	28480	83592-20018
MP31	83592-20015	4	1	SIDERAIL - LOWER RIGHT	28480	83592-20015
MP32	83592-00012	9	1	WIRE HOLDER	28480	83592-00012
MP33	83592-00004	9	1	BRACKET AMPLIFIER	28480	83592-00004

Figure 6-1. Major Mechanical Parts (3 of 4)



Item	HP Part Number	CD	Qty	Description	Mfr. Code	Manufacturer's Part Number
MP34	83592-00028	7	1	PANEL - REAR	28480	83592-00028
MP35	5021-0906	6	3	BUSHING PLASTIC	28480	5021-0906
MP36	11869-20020	4	1	ALIGHMENT PIN	28480	11869-20020
MP37	6960-0002	4	1	PLUG-HOLE 0.500 D (STANDARD)	28480	6960-0002
MP38	6960-0003	5	1	PLUG-HOLE 0.750 D (STANDARD)	28480	6960-0003

Figure 6-1. Major Mechanical Parts (1 of 4)

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				ATTACHING HARDWARE NOTE: SEE FIGURE 6-2 FOR ATTACHING HARDWARE LOCATIONS		
1	0360-1190	5	1	TERMINAL-SLDR LUG PL-MTG FOR-#3/8SCR	28480	0360-1190
2	0360-1632	0	1	TERMINAL-SLDR LUG LK-MTG FOR-#3/8SCR	28480	0360-1632
3	0520-0127	6	2	SCREW-MACH 2-56 .188-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
4	0624-0099	1	30	SCREW-TPG 4-20 .375-IN-LG PAN-HD-POZIL	00000	ORDER BY DESCRIPTION
5	2190-0016	3	2	WASHER-LK INTL T 3/8 IN. .377 IN-ID	28480	2190-0016
6	2190-0018	5	4	WASHER-LK HLCL NO. 6 .141-IN-ID	28480	2190-0018
7	2190-0104	0	1	WASHER-LK INTL T 7/16 IN. .439-IN-ID	28480	2190-0104
8	2190-0112	0	2	WASHER-LK HLCL NO. 2 .088-IN-ID	28480	2190-0112
9	2190-0401	0	2	WASHER-FL NM NO. 4 .12-IN-ID .312-IN-OD	28480	2190-0401
10	2200-0101	0	4	SCREW-MACH 4-40 .188-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
11	2200-0103	2	2	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
12	2200-0105	4	6	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
13	2200-0104	3	6	SCREW-MACH 4-40 .25-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
14	2200-0111	2	8	SCREW-MACH 4-40 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
15	2260-0009	3	4	NUT-HEX-W/LK WR 4-40-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
16	2360-0115	4	15	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
17	2360-0117	6	3	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
18	2360-0119	8	2	SCREW-MACH 6-32 .438-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
19	2360-0190	5	3	SCREW-MACH 6-32 .188-IN-LG 100 DEG	00000	ORDER BY DESCRIPTION
20	2360-0209	7	4	SCREW-MACH 6-32 1-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
21	2360-0331	6	5	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	28480	2360-0331
22	2360-0333	8	8	SCREW-MACH 6-32 .25-IN-LG 100 DEG	28480	2360-0333
23	2360-0334	9	9	SCREW-MACH 6-32 .312-IN-LG 100 DEG	28480	2360-0334
24	2460-0009	7	2	SCREW-MACH 6-32 .188-IN-LG PAN-HD-PHL	00000	ORDER BY DESCRIPTION
25	2950-0001	8	4	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
26	2950-0132	6	1	NUT-HEX-DBL-CHAM 7/16-28-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
27	3050-0003	3	4	WASHER-FL NM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
28	3050-0010	2	4	WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0010
29	3050-0105	6	4	WASHER-FL MTLC NO. 4 .125-IN-ID	28480	3050-0105
30	0520-0126	5	2	SCREW-MACH 2-56 .125-IN-LG 100 DEG	28480	0520-0126
31	0520-0166	3	2	SCREW-MACH 2-56 .375-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
32	2200-0003	1	2	SCREW-MACH 4-40 .25-IN-LG RD-HD-SLT	00000	ORDER BY DESCRIPTION
33	2200-0140	7	2	SCREW-MACH 4-40 .25-IN-LG 100 DEG	00000	ORDER BY DESCRIPTION
34	2510-0047	0	2	SCREW-MACH 8-32 .438-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION

See introduction to this section for ordering information.

*Indicates factory selected value.

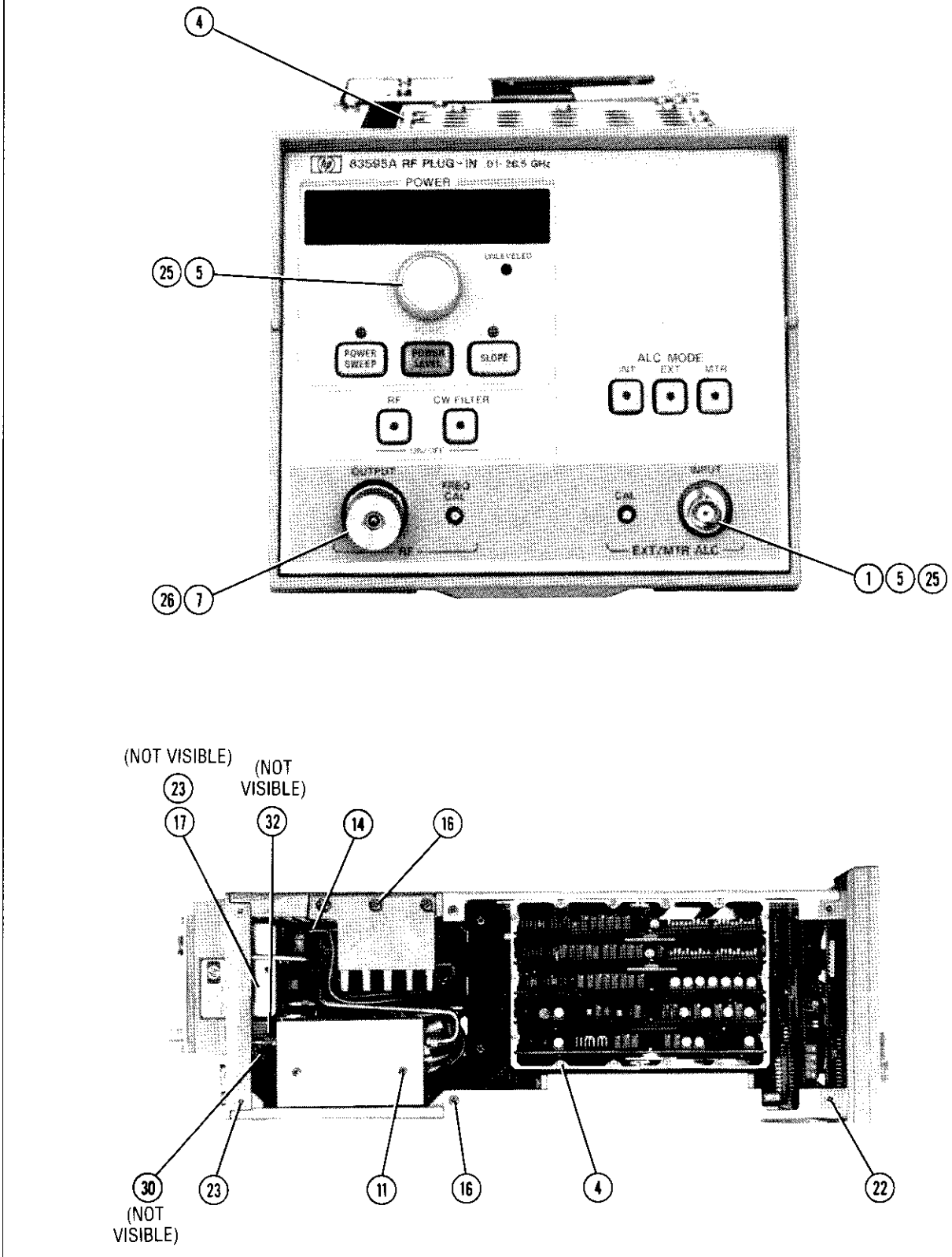


Figure 6-2. Attaching Hardware (1 of 3)

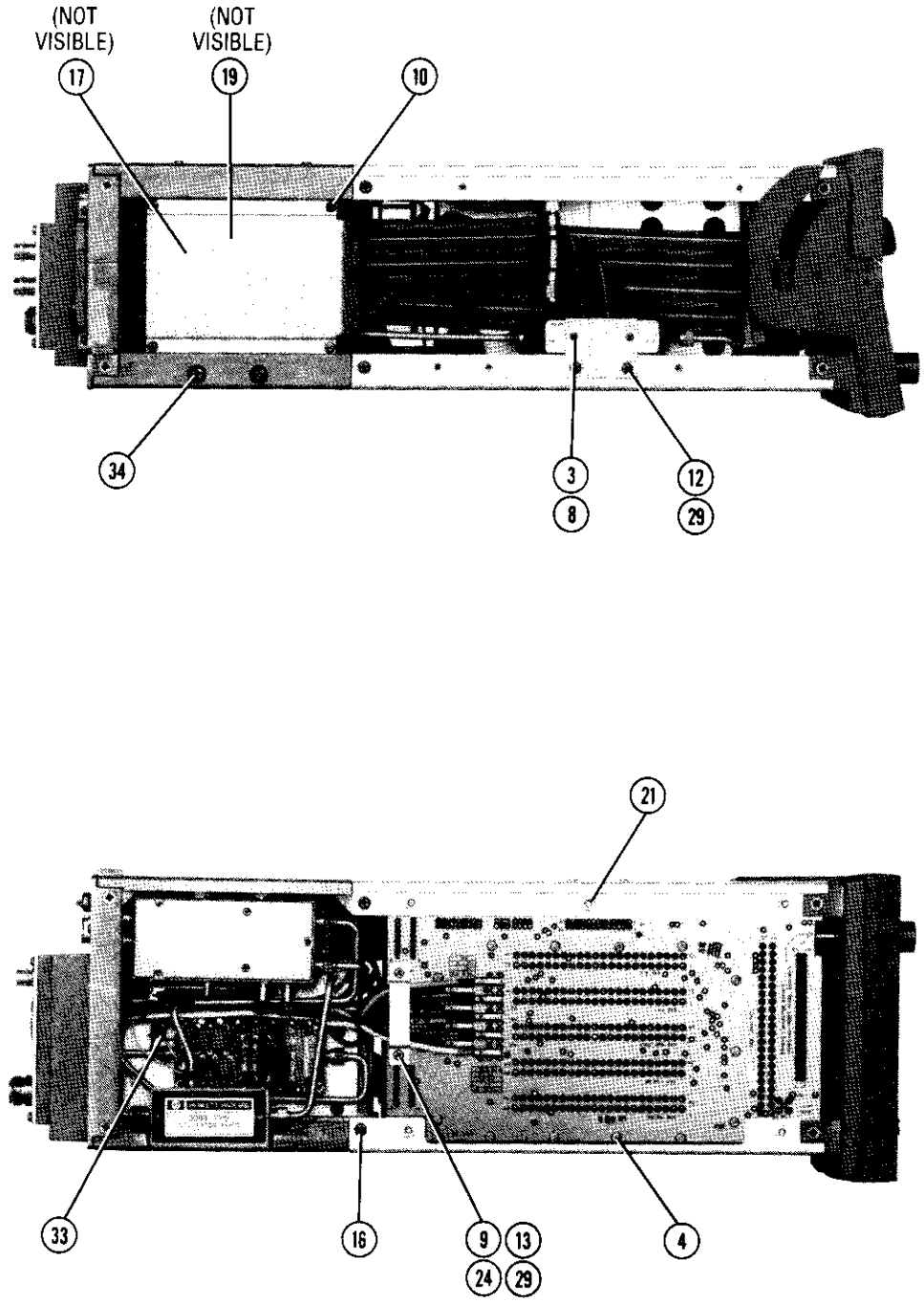


Figure 6-2. Attaching Hardware (2 of 3)

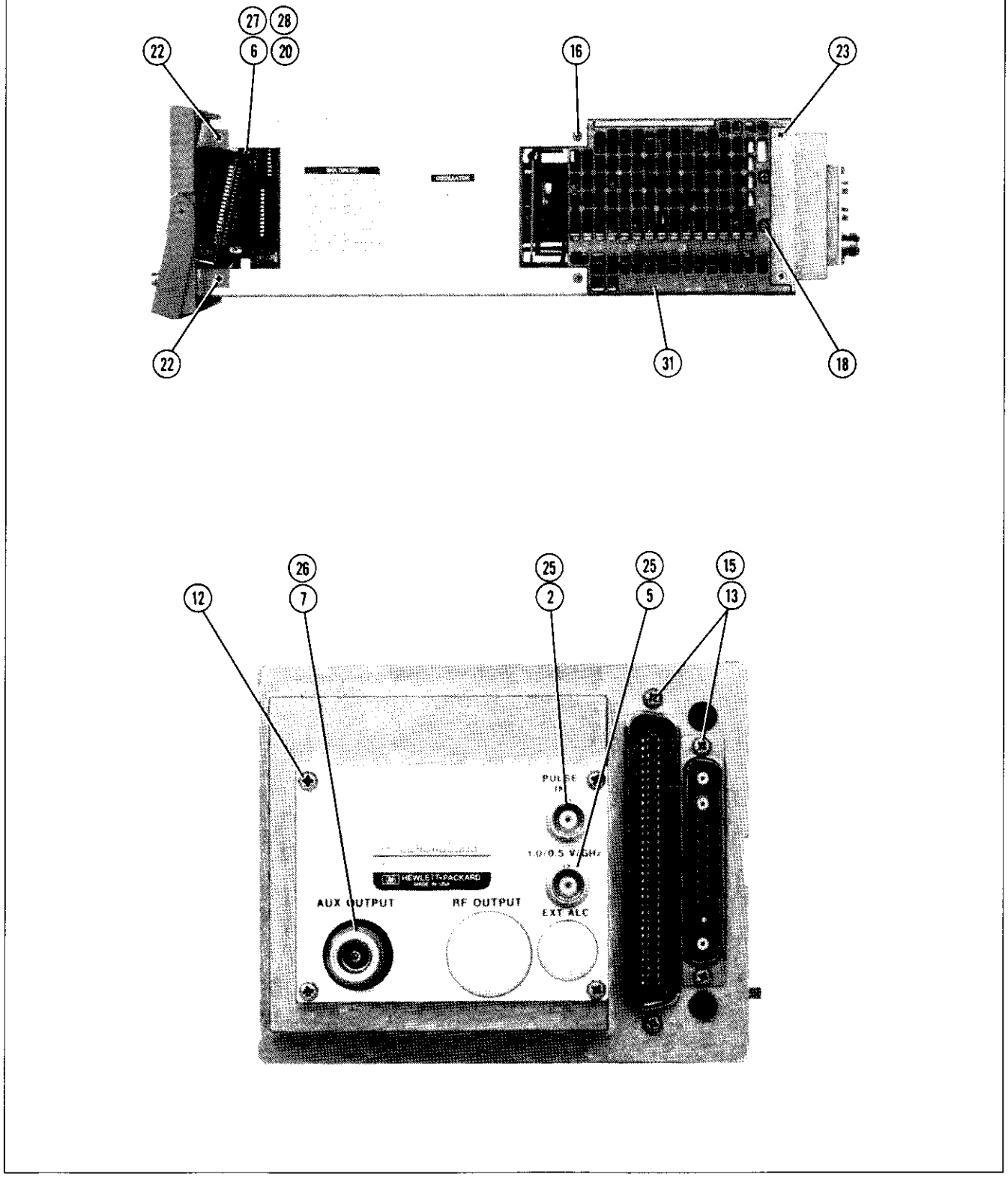
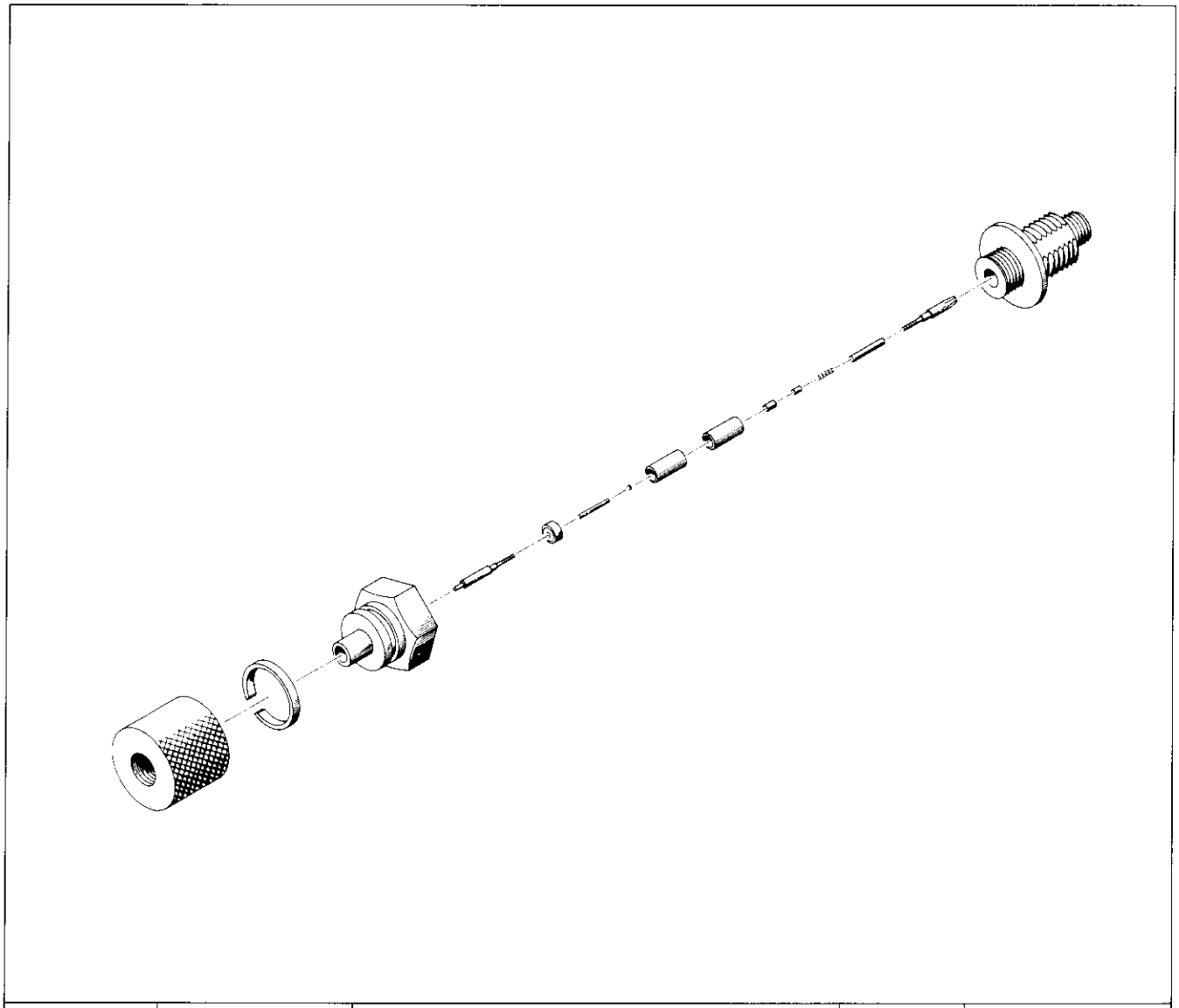


Figure 6-2. Attaching Hardware (3 of 3)



Reference Designation	HP Part Number	Description	Mfr. Code	Manufacturer's Part Number
J1	86290-60005	CONNECTOR ASSY (TYPE-N) (RF OUTPUT) SAME AS J3 (AUX OUT)	28480	86290-60005
J1MP1	1250-0914	BODY: RF CONNECTOR (TYPE-N)	02660	131-150
J1MP2	1250-0915	CONTACT: RF CONNECTOR (TYPE-N)	02660	131-149
J1MP3	5040-0306	INSULATOR	28480	5040-0306
J1MP4	08555-20093	CENTER CONDUCTOR	28480	08555-20093
J1MP5	08555-20094	BODY; BULKHEAD	28480	08555-20094
J1MP6	2190-0104	WASHER; LOCK 0.439 INCH ID	00000	OBD
J1MP7	2950-0132	NUT: HEX 7/16 - 28	00000	OBD
J1MP8	08761-2027	INSULATOR	28480	08761-2027

Figure 6-3. RF Output Connector, Exploded View

Section 7. Manual Backdating

INTRODUCTION

This manual has been written for and applies directly to instruments with serial numbers prefixed as indicated on the title page. Earlier versions of the instrument (serial numbers prefixed lower than the ones indicated on the title page) may be slightly different in design or appearance.

There is a separate manual available documenting earlier versions of the HP 83595A. If your instrument was manufactured before the printing of this manual, you can order a separate manual that documents these earlier versions. (HP Part Number 83595-90003).

Later versions of the instrument (serial prefixes higher than the ones indicated on the title page) are documented in a yellow *Manual Changes Supplement*.

For additional important information about serial number coverage, refer to INSTRUMENTS COVERED BY THE MANUAL in Section 1.

Section 8. Service

INTRODUCTION

This section provides instructions for troubleshooting and repairing the HP 83595A RF plug-in. Information includes circuit descriptions, troubleshooting procedures, block diagrams, schematics, and component location maps for each PC (printed circuit) assembly.

WARNING

Adjustments or repairs inside the HP 8350/83595A with the top or bottom cover removed and the AC power connected should be avoided whenever possible. Any procedure requiring a cover to be removed from the instrument and AC power connected to the mainframe SHOULD BE PERFORMED ONLY BY QUALIFIED SERVICE PERSONNEL WHO ARE AWARE OF THE HAZARDS INVOLVED. With the AC power cable connected to the instrument, the AC line voltage is present on the terminals of the line power module on the rear panel, and at the LINE power switch, whether the switch is ON or OFF. The AC line voltage on these terminals can, if contacted, produce fatal electrical shock. You must also be aware that capacitors inside the instrument may remain charged even though the instrument has been disconnected from its AC power source.

After you have completed a repair, check the instrument carefully to make sure all safety features are intact and functioning, and that all protective grounds are solidly connected.

SERVICE INFORMATION

Each smaller section within the larger Service Section pertains to a specific assembly and are arranged in assembly number order. Table 8-1 provides a Service Information Index.

SCHEMATIC DIAGRAM NOTES

Figure 8-1, Schematic Diagram Notes, provides definitions to schematic symbols.

MNEMONICS

The Motherboard Wiring List lists alphabetically and defines all HP 83595A signal mnemonics, references the point-to-point distribution of each signal to and from the PC assembly sockets and the cable connectors on the A10 Motherboard assembly, and identifies the signal source. This table is located in the tabbed section A10 Motherboard and Wiring Lists.

SERVICE AIDS

Two Extender Cable Assemblies, HP Part Number 08350-60034 (64 pin) and 08350-60035 (17 pin), are designed to power the RF plug-in when it is removed from the HP 8350 sweep oscillator for troubleshooting. These service aids are recommended for convenience in servicing the HP 83595A.

A 44-pin extender assembly (HP Part No. 08350-60031) is available to allow access to printed circuit assembly components while maintaining electrical contact with the plug-in. This and other service aids are referenced in section 1, Table 1-3, of this manual.

Table 8-1. Service Information Index

Assembly	Fig. No.	Assembly	Fig. No.
OVERALL		**A6 SWEEP CONTROL**	
Troubleshooting/Circuit Description		Troubleshooting/Circuit Description	
Simplified Overall Block	8-7	Block Diagram	8-47
Overall Block Diagram	8-8	Component Locations	8-48
		Schematic	8-49
A1/A2 FRONT PANEL		**A7/A9 SYTM DRIVER/ REFERENCE RESISTOR**	
Troubleshooting/Circuit Description		Troubleshooting/Circuit Description	
Block Diagram	8-15	Block Diagram	8-57
Front Panel A1 Component Locations		SYTM Driver A7 Component Locations	8-58
Front Panel Interface A2	8-16	Reference Resistor A9 Component Locations	8-59
Component Locations	8-17	Schematic	8-60
Schematic	8-18		
A3 DIGITAL INTERFACE		**A8/A9 YO DRIVER/ REFERENCE RESISTOR**	
Troubleshooting/Circuit Description		Troubleshooting/Circuit Description	
Block Diagrams	8-21	Block Diagram	8-68
Component Locations	8-22	YO Driver A8 Component Locations	8-69
Schematic	8-23	Reference Resistor A9 Component Locations	8-70
		Schematic	8-71
A4 ALC		**RF SECTION**	
Troubleshooting/Circuit Description		Troubleshooting/Circuit Description	
Block Diagram	8-32	A12A1 Component Locations	8-72
Component Locations	8-33	A13A1 Component Locations	8-73
Schematic	8-34	A14A1 Component Locations	8-74
		A16A1 Component Locations	8-75
		RF Section Schematic	8-76
A5 FM DRIVER		**A10 MOTHERBOARD**	
Troubleshooting/Circuit Description		Component Locations	8-79
Block Diagram	8-40	Cable List - Table 8-22	
Component Locations	8-41	Wiring List - Table 8-23	
Schematic	8-42	**HP 83595A**	
		Major Assemblies Locations	8-80

BASIC COMPONENT SYMBOLOGY

R, L, C — Resistance is in ohms, inductance is in microhenries, capacitance is in microfarads, unless otherwise noted.

P/O — Part of.

Indicates a factory selected component.

Panel Control.

Screwdriver adjustment.

Encloses front panel designation.

Encloses rear panel designation.

Circuit assembly borderline.

Other assembly borderline.

Heavy line with arrows indicates path and direction of main signal.

Indicates path and direction of main feedback.

Earth ground symbol.

Assembly ground. May be accompanied by a number or letter to specify a particular ground.

Chassis ground.

n — Represents n number of transmission paths.

Test Point: Terminal provided for test probe.

Pin Edge Connector output of PC board.

Indicates wire or cable color code. Color code same as resistor color code. First number indicates base color, second and third numbers indicate colored stripes.

Indicates shielding conductor for cables.

Indicates a plug-in connection.

Indicates a soldered or mechanical connection.

Connection symbol indicating a male connection.

Connection symbol indicating a female connection.

Resistor.

Variable Resistor.

General purpose diode.

Step recovery diode.

Schottky diode.

Breakdown Diode: Zener

Light-Emitting Diode.

SCR (Silicon Controlled Rectifier).

Thermistor

FET: Field Effect Transistor (N-channel).

FET: Field Effect Transistor-Guarded gate- (N channel).

Dual Transistor.

Transistor NPN

Transistor PNP

Electrolytic Capacitor.

Toroid: Magnetic core inductor.

Operational Amplifier.

Fuse

Pushbutton Switch.

Toggle Switch.

Thermal Switch.

Summing Point.

Oscillator; RPG (Rotary Pulse Generator).

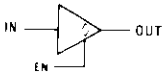
Fan, Motor.

Toroidal Transformer

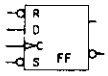
Figure 8-1. Schematic Diagram Notes (1 of 3)

INTEGRATED CIRCUIT SYMBOLOGY

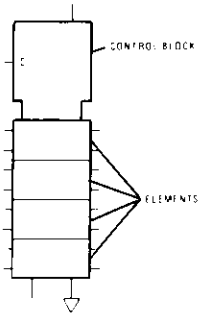
Schmitt Trigger: The gate of the Schmitt Trigger switches at different points for positive - and negative-going signals. The difference between the positive and negative thresholds is defined as hysteresis voltage.



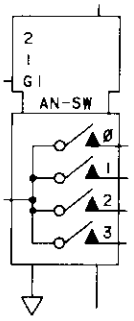
3-State Buffer: Three States:
Enable (EN) Input low: High impedence output.
Enable input high: Output = 0 or
Output = 1



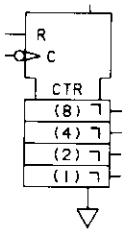
Data Flip-Flop: Set (S) and Reset (R) are asynchronous controls. Active S sets the noninverting output high and the inverting output (○—) low; active R resets both outputs. When S and R are both inactive, the outputs remain latched in the last state. An active clock (—▷) enables the D input, at which time the noninverting output = D, and the inverting output = $\bar{D}$.



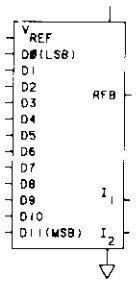
Control Block: All controlling inputs (gates, clocks, inhibits, etc.) connect to the control block.
Elements: Can be one or more of any logic function (flip-flop, counter, gate, RAM, etc.). Data inputs are on the left side of element, data outputs on the right.



Analog Switch: Control lines 1 and 2 decode to select one of four inputs. G1, high=enable.



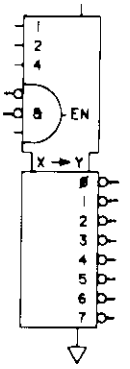
Counter: Binary-weighted registers count on the falling edge of each clock pulse. Active (high) R clears all registers.



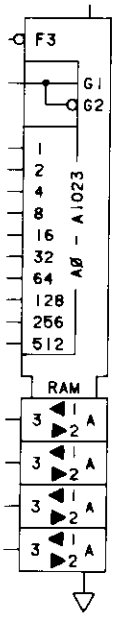
Digital to Analog Converter (DAC): Provides a scaled current output (I_1), the product of V_{REF} and the fractional binary input:

$D_{11}2^{-1} + D_{10}2^{-2} + D_9 2^{-3} + \ldots D_0 2^{-12}$

The product of V_{REF} and complement of the binary input appears at I_2.



Decoder: The logic states of the three select lines A, B, and C, and the three enable inputs (EN), determine which one of the eight outputs will be decoded. The selected output will be low, while all others are high.



Random-Access Memory (RAM): Binary addresses (A0 to A9) access one of 1024 registers in RAM. When G1 is high, bits appearing at D0 to D3 will be written to the addressed location (A0 to A9). When G2 is low, bits appearing at D0 to D3 have been accessed from the addressed location.

Figure 8-1. Schematic Diagram Notes (2 of 3)

FUNCTION LABEL ABBREVIATIONS

Σ	Adder	◇	Open Collector	LED	Light-Emitting Diode
	Amplifier/Buffer		Monostable Multivibrator	MUX	Multiplexer
	Schmitt Trigger	BCD	Binary Coded Decimal	RAM	Random-Access Memory
&	AND	CTR	Counter	REG	Register
≥1	OR	DAC	Digital-to-Analog Converter	ROM	Read Only Memory
=1	Exclusive OR	FF	Flip-Flop	RPG	Rotary Pulse Generator
X→Y	Encoder, Decoder	I/O	Input/Output		

LINE LABEL ABBREVIATIONS

CK, C	Clock Input	MSB	Most Significant Bit	T	Trigger Input (Monostable)
D	Data or Delay Input (Flip-Flop)	Q	Output	WR	Write
EN	Enable	$\overline{Q}$	Not Q Complement of Q	+1	Count Up
F	3-State Enable Input	R	Reset or Clear Input	−1	Count Down
G	Gating Input	RD	Read	3-ST	3-State (placed by function)
LSB	Least Significant Bit	S	Set Input		

Figure 8-1. Schematic Diagram Notes (3 of 3)

TROUBLESHOOTING

CAUTION

Improper methods of discharging the −40 Volt supply may result in damage to the instrument. Refer to the HP 8350 Sweep Oscillator Operating and Service Manual for these procedures.

Troubleshooting is generally divided into two maintenance levels in this manual. The first level isolates the problem to a circuit or assembly. SELF-TEST (described below) together with the Overall Block Diagram and Troubleshooting hints, helps to isolate the problem source to a particular assembly.

The second maintenance level isolates the trouble to the component. Operator-initiated tests, schematic diagrams, and circuit descriptions for each assembly aid in troubleshooting to the component level.

SELF-TEST

HP 8350 software provides microprocessor and operator-initiated checks. These checks verify the proper functioning of the majority of the HP 8350 and 83595A digital circuitry and a portion of the analog devices.

Whenever the HP 8350 is powered ON, or the front panel **[INSTR PRESET]** pushbutton is pressed, instrument SELF-TEST is initiated. Instrument SELF-TEST checks a number of circuits in both the HP 8350 and the 83595A. If a failure in the HP 83595A is detected during SELF-TEST, error code E001 will be displayed Table 8-2 lists other error codes associated with the HP 83595A RF plug-in.

If the front panel displays an error code, refer to the Overall Block Diagram and Troubleshooting section. This section will help the operator to define the troubled area.

Table 8-2. Associated Error Codes

Error Code	Circuit Tested
E001	Addresses HP 83595A ROM and reads Check Sum back to HP 8350.
E050	Erroneous Front Panel Pushbutton Flag.
E051	Erroneous Front Panel Pushbutton Code received by HP 8350 Microprocessor.
E052	Checks for Timer Failure in A3.
E053	Checks PIA circuits in A3.
NOTE **Error Codes E050 through E099 are reserved for the RF plug-ins, however, not all are used.**	

OPERATOR-INITIATED TESTS

The HP 8350 microprocessor services several operator-initiated tests of the 83595A to check functions which are not exercised during SELF-TEST. The tests may be initiated by making the appropriate key entry indexed in Table 8-3.

Access to most of the HP 83595A digital circuitry can be achieved through local programming with the following key entry commands:

Function	Key Entry
Hex Address Entry	**[SHIFT] [0] [0] [M1]*** (enter hex address)
Hex Data WRITE	**[M2]** (enter data: two hex digits)
Hex Data READ	**[M3]**
Hex Data Rotation Write	**[M4]**
Hex Addressed Fast Read	**[M5]**

*To address a different location, press **[M1]** and enter the new address, or use the increment and decrement keys, **[▲] [▼]** to step to the new address.

NOTE: Before addressing an HP 83595A component, determine whether or not the HP 8350 microprocessor can READ or WRITE to that particular device. The majority of HP 83595A digital chips do NOT have both READ and WRITE capabilities.

By entering the hex address location of a specific device, that device can be exercised. (Addresses are supplied next to the mnemonic on each schematic. Also, circuit descriptions usually include address decoder tables to define the addresses used on that particular assembly.) Hex address entry must be made prior to any of the following:

HEX DATA WRITE, **[M2]**, allows the operator to write any combination of hex data bytes to the addressed device. The outputs can then be checked to see if the device is functioning properly.

HEX DATA READ, **[M3]**, allows the operator to read the outputs of an addressed device.

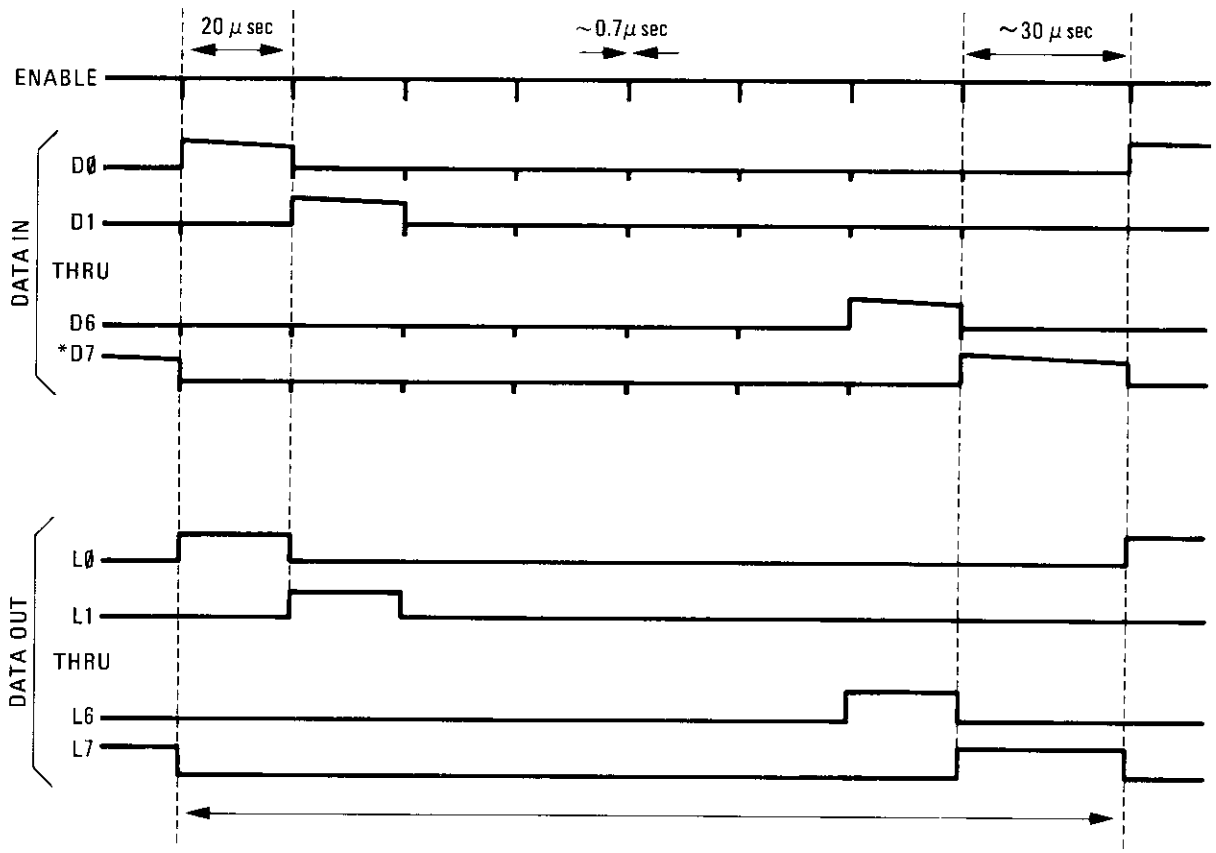
HEX DATA ROTATION WRITE, **[M4]**, strobes a one "1", (high state) through a column of zeroes (low states) to the addressed device. In effect, hex data rotation write is a rapid WRITE mode, exercising the addressed device in real time. The microprocessor inputs the data continuously, without servicing interrupts from the rest of the instrument. Latch enable lines, inputs, and outputs can be checked in this mode. Figure 8-2 illustrates the appropriate waveforms.

HEX ADDRESSED FAST READ, **[M5]**, provides an operator-initiated check for verification of the data bus, in which the addressed device is clocked in real time. Latch outputs can be traced from the onboard location back through the data bus to the microprocessor. At each buffer, verify TTL level response to the enable pulse. Enable line waveforms are shown in Figure 8-3.

All operations can be exited by pressing **[INSTR PRESET]**.

Table 8-3. Operator-Initiated Self Test Routines Available

Data Entry	Test	Assembly*	Test Point
SHIFT 50	Power Level DAC	A4	A4TP2
SHIFT 51	Power Sweep DAC	A5	A5TP8
SHIFT 52	Scale/Offset DACs	A7,A8	A7TP1, A7TP9, A8TP2, A8TP3
SHIFT 53	Address Decoder; checks major address decoder lines.	A7,A8	A3U6, A3U7, A3U9, A3U13
SHIFT 54	Address Decoder; checks individual board address decoders.	A4 thru A8	Address Decoders
SHIFT 55	Interrupt Control	A3	A3U4 pin 38
SHIFT 56	Bandswitch DAC	A6	A6TP1
*Refer to troubleshooting procedure of the appropriate assembly for waveforms and detailed procedures.			



*DURATION OF LAST BIT PULSE IS APPROXIMATELY 30 μ SEC DUE TO DELAY BETWEEN RECYCLE.

Figure 8-2. Hex Data Rotation Write — Bit Pattern

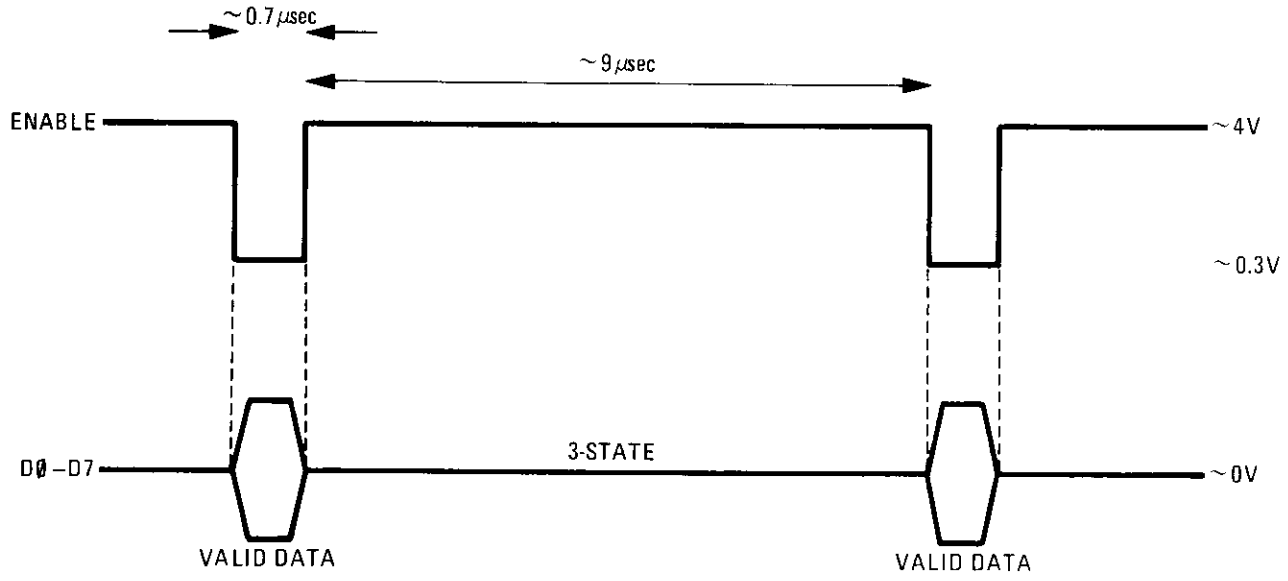


Figure 8-3. Hex Addressed Fast Read — Timing Diagram

HEXADECIMAL

Hexadecimal is the number system used to locally address the HP 8350 and 83595A logic components. Available operator-initiated self test routines are indexed in Table 8-3.

The hexadecimal system uses 16 digits: 0 through 9 and A through F. Since 16 is the fourth power of two, four-bit binary numbers can be expressed with one hexadecimal digit, making local programming easier. Table 8-4 provides hexadecimal conversions to binary and decimal equivalents.

When the HP 8350 is in the hex data write mode several front panel keyboard pushbuttons convert to hexadecimal digit entries. The hex numbers assigned to the DATA ENTRY keys are shown in Figure 8-4.

Table 8-4. Hexadecimal Equivalents

Hexadecimal	Binary	Decimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
A	1010	10
b	1011	11
C	1100	12
d	1101	13
E	1110	14
F	1111	15

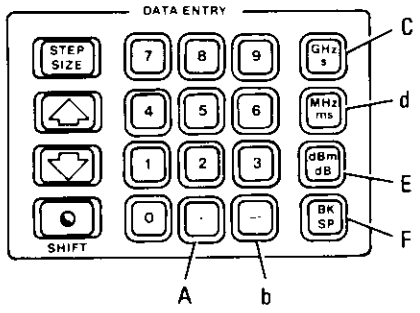


Figure 8-4. Hex Entry Keys

RECOMMENDED TEST EQUIPMENT

Test equipment required to maintain the HP 83595A is listed in Section 1. If the equipment listed is not available, equipment that meets the minimum specifications shown may be substituted.

REPAIR

Module Exchange Program

This instrument may be quickly repaired by replacing a defective module with a restored-exchange module. To support the module repair strategy, Hewlett-Packard has set up a module exchange program.

The procedure for using the module exchange program is given in Figure 8-5. When you locate the defective module, order a replacement module through the nearest Hewlett-Packard sales office. The restored-exchange module will be sent immediately directly from a customer service replacement parts center. When you receive the exchange module, return the defective module in the same special carton in which the exchange module was received. DO NOT return a defective module to Hewlett-Packard until you receive the exchange module.

If you are not going to return the defective module to Hewlett-Packard, or if you are ordering a module for spare parts stock, etc., order a new module using the new module part number listed in Table 6-3.

The Hewlett-Packard module exchange program allows you to obtain a fully tested and guaranteed restored-exchange module at a reduced price. (The reduced price is contingent upon return of the defective module to Hewlett-Packard.) Assemblies available for module exchange are listed in Table 6-1.

Replacing YO A13, SYTM A12, YO Driver A8, or SYTM Driver A7

Each YO (YIG oscillator) or SYTM (switched YIG tuned multiplier) requires a unique set of resistors to be installed on its respective driver assembly (A7 or A8) for proper YIG coil drive. The values of these resistors are documented on labels attached to the side of the HP 83595A near the RF section. If the driver assembly (A7 or A8) is replaced, the resistor header containing these resistors must be installed on the new assembly. Also, if the YO or SYTM is replaced, the resistor header shipped with the YO or SYTM must be installed on the driver assembly in place of the old resistors. (In some cases, some or all of the resistors may be deleted, depending on the drive requirements of the individual YO or SYTM.)

Rear Panel Connector Replacement

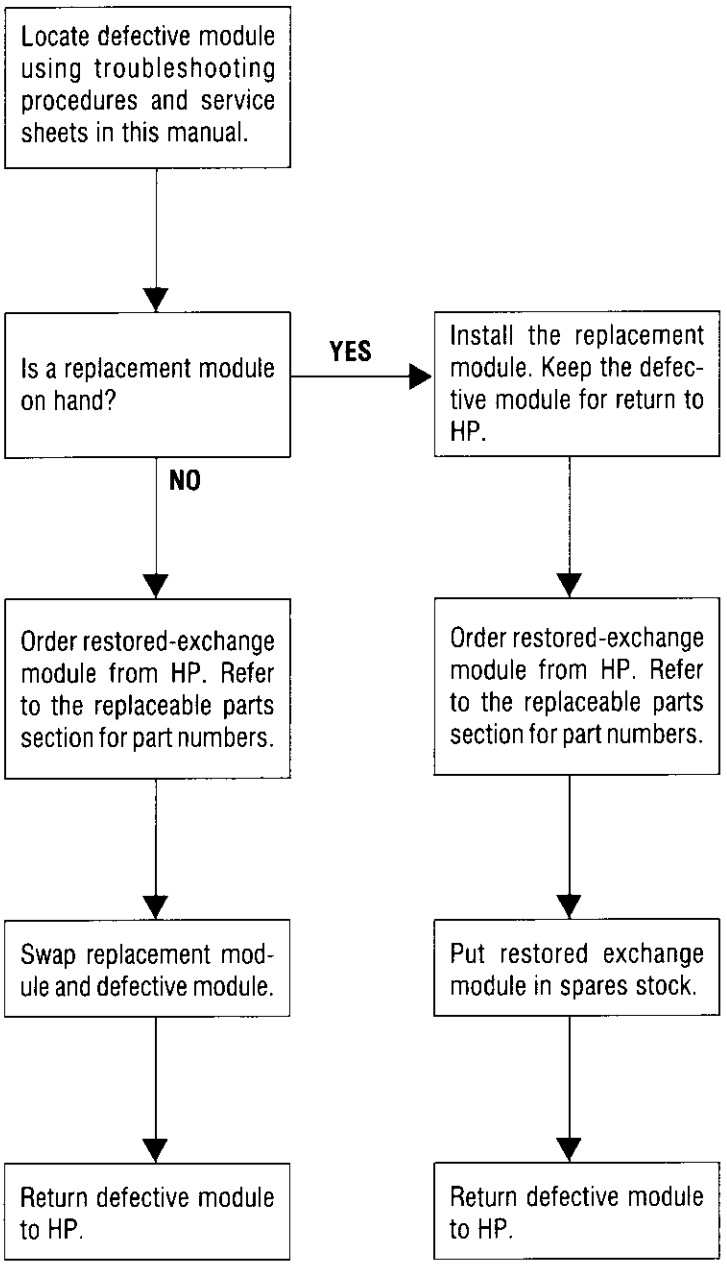
When replacing rear panel connector P1, connector P2 also must be partially removed to remove P1 from the rear panel casting.

When reassembling rear panel connectors P1 and P2 into the casting, alignment is very critical to ensure proper interface with the mating HP 8350 connectors. Align the center of the attaching bolts with a steel rule and tighten in place in accordance with the placement drawing in Figure 8-6.

AFTER-SERVICE PRODUCT SAFETY CHECKS

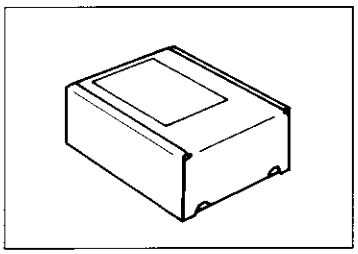
Visually inspect the interior of the instrument for any signs of abnormal internally generated heat, such as discolored printed circuit assemblies or components, damaged insulation, or evidence of arcing. Determine and remedy the cause of any such condition.

The module exchange program described here is a fast, efficient, economical method of keeping your Hewlett-Packard instrument in service.



*HP pays postage on boxes mailed in U.S.A.

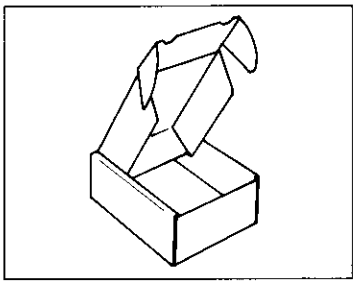
A.



Restored-exchange modules are shipped individually in boxes like this. In addition to the circuit module, the box contains:

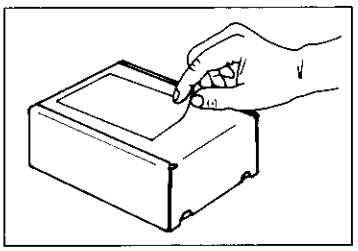
Exchange assembly failure report
Return address label

B.



Open box carefully - it will be used to return defective module to HP. Complete failure report. Place it and defective module in box. Be sure to remove enclosed return address label.

C.



Seal box with tape. Inside U.S.A.*, stick preprinted return address label over label already on box, and return box to HP. Outside U.S.A., do not use address label; instead address box to the nearest HP office.

Figure 8-5. Module Exchange Procedure

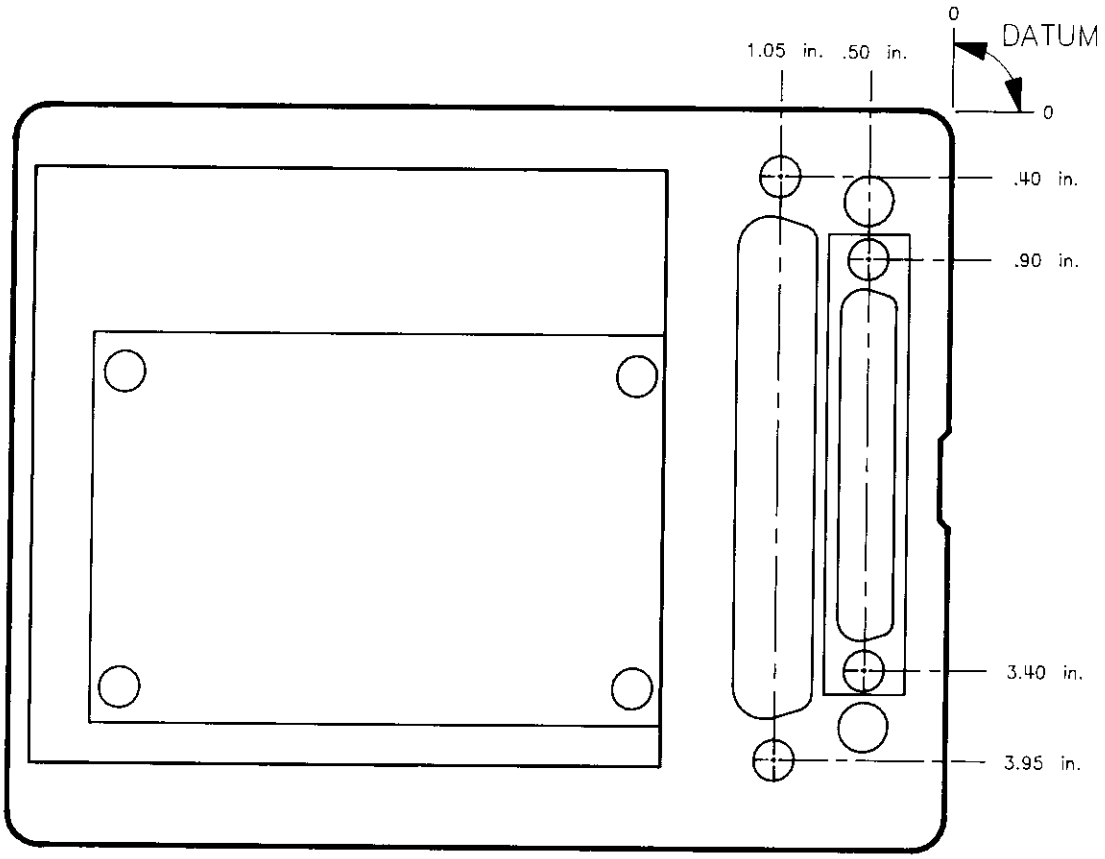


Figure 8-6. Rear Panel Connector Alignment

HP 83595A Overall Troubleshooting

INTRODUCTION

The purpose of this troubleshooting information is to provide an aid in isolating a problem in the HP 83595A to a specific assembly. Further troubleshooting information is supplied with each assembly service section to isolate the problem to the component level.

The first step in overall troubleshooting is to identify the symptom(s) and determine under what conditions the problem exists. If the problem is an RF plug-in error code (E001 or E050 through E053) refer to the Error Code section of this troubleshooting procedure. Also ensure that the HP 8350 used with the HP 83595A is calibrated and functionally operating.

DETERMINING THE PROBLEM

A failure in the HP 83595A normally affects one of the following functions.

Front Panel/Digital Control – Probable symptoms are error code E001, incorrect annunciator or digit displays, inability to control operation from front panel, or erratic instrument response to front panel entries. The problem is generally on the A1, A2, or A3 assemblies, or with the RF plug-in/HP 8350 interface.

Frequency Control – Frequency control problems include frequency inaccuracy, sweep control problems or power losses due to the SYTM not tracking the YO frequency. If the HP 8350 VTUNE output and power supplies are verified, the problem is most likely on the A5, A6, A7, A8, or A9 assemblies, or in the RF section. If a frequency accuracy problem occurs only during swept operation, and the inaccuracy increases with faster sweep times, the problem is most likely with the delay compensation circuit on the A8 YO driver assembly. Power losses that can be corrected with the front panel PEAK control indicate that the YO/SYTM tracking needs calibration (Refer to Section 5, Adjustments).

Power Control – Typical problems are no RF output, maximum unleveled RF output, or excessive power level variations. The problem is most likely with the A4, A5, or RF section. If the trouble is limited to power sweep and slope control, the problem is most likely with the power sweep DAC on the A5 assembly. If the power loss is in bands 1 through 4, try adjusting the front panel PEAK control to peak the power. If the power losses are eliminated, perform the YO/SYTM tracking adjustments in Section 5.

RF Path – Problems associated with high-frequency microcircuits include spurious or harmonic distortion, no RF power, or full unleveled RF power. For a harmonic distortion problem, refer to Section 5, Adjustments. For power problems, try peaking the power with the front panel PEAK control, then refer to the A4 ALC Troubleshooting before suspecting the RF components.

Once the problem is identified, exercise the RF plug-in to determine under what conditions the problem exists. Some important conditions to check are:

Band related – Does problem exist for only band 0 or bands 1 through 4, or does it exist on all bands? If a power or leveling problem is restricted to one band, the problem is limited to the respective detector, modulator driver, or modulator.

Sweep Mode related – Is problem only for swept modes of operation, or does it also exist in CW operation? If problem exists in CW operation, troubleshoot in this mode (it is easier to check waveforms and voltages in CW operation). For problems that occur only for swept operation, check if problem exists for single band sweeps. If the problem occurs only for multiband sweeps, suspect the bandswitch control circuit on the A6 sweep control assembly.

Control related – Try different methods of entering data (i.e. RPG, data entry keys, or increment/decrement keys). If the problem is related to a specific control, troubleshoot that control and respective circuits. If the problem is related to a specific type of control (i.e. pushbuttons) refer to the A1/A2 service information and troubleshoot the respective interface circuit.

Sweep Time related – Swept frequency accuracy problems that get worse with faster sweep times are probably caused by the delay compensation circuit on the A8 YO driver assembly. If it is necessary to adjust the front panel PEAK control for different sweep times, the trouble is probably caused by the delay compensation circuit on the A7 SYTM driver.

ERROR CODES

RF plug-in error codes are displayed in the HP 8350 left FREQUENCY display. The error codes may be generated as a result of the INSTRUMENT PRESET self test (**E001**, **E052**, or **E053**), or during normal instrument operation (error codes **E050** or **E051**). A description of each error code is provided in Table 8-9. Further troubleshooting information for each error code follows.

Error Code E001

Error code **E001** indicates that the HP 8350 microprocessor is unable to properly read plug-in ROM. Initial checks should be made to verify proper mating of rear panel connectors with the HP 8350. Also check cable connections to the A3 digital interface and ensure A3 is properly installed. Refer to the A3 service information for specific troubleshooting information.

Error Code E050

Error code **E050** is generated when the HP 8350 microprocessor responds to an RF plug-in keyboard flag and no key has been pressed. Check the logic state of the FLAG input to the A3 digital interface (A3P1 pin 42). It should be a stable logic low until a front panel key is pressed (when it is briefly strobed high). If it is not a stable low, refer to the A1/A2 service information for further troubleshooting. If FLAG is a stable low, check that the L PIFLG output of A3 (A3J1 pin 39) is a stable high and pulses low when a front panel key is pressed. If necessary, trace the logic state of L PIFLG on the HP 8350 A3 microprocessor.

Error Code E051

Error code **E051** indicates that an invalid keycode is received by the HP 8350 microprocessor. Refer to the A1/A2 service information to troubleshoot the keyboard matrix and keyboard/display interface circuit.

Error Code E052

Error code **E052** is generated if there is a problem with the interval timer on the A3 digital interface. A test routine is run at power-on or when INSTRUMENT PRESET self test is initiated. If error code **E052** is generated, refer to the A3 digital interface service information for further troubleshooting.

Error Code E053

Error Code **E053** is generated at power-on or INSTRUMENT PRESET when there is a problem with the PIA (peripheral interface adapter) on the A3 digital interface. If error code **E053** is generated, refer to the A3 digital interface service information for further troubleshooting.

DIGITAL CONTROL/FRONT PANEL

A digital control problem usually affects the entire plug-in, but may disable only a section of the instrument. Generally, a digital control problem is indicated by a front panel failure. If the problem is limited to a specific type of control (pushbutton or RPG) or display (annunciator or digital display), the indication is that of a front panel failure. An RPG failure may indicate problems on the front panel assemblies of the HP 8350 mainframe, where RPG pulses are decoded. If multiple front panel functions are inoperative or erratic, the problem is most likely a digital control problem. Detailed troubleshooting procedures for checking front panel operation are provided in the A1/A2 service information. For digital control problems, refer to the A3 digital interface service information, and check the address, data, and control line outputs of the A3 assembly.

When there is a problem with a digital-to-analog interface (i.e. DAC), the symptom is generally a discontinuity in the analog response.

FREQUENCY CONTROL

Troubleshooting a frequency control problem can be greatly simplified by first defining the conditions under which the problem exists. When troubleshooting, the RF plug-in should be operating in the least complicated mode that exhibits the frequency control problem. For instance, a CW frequency is less complicated than a swept mode, and a single band sweep is less complicated than a multiband sweep.

NOTE: To ensure accurate frequency counter readings, check for adequate RF output power.

Frequency Accuracy Problem for Band 0 (.01 to 2.4 GHz)

Frequency accuracy problems that occur only in band 0 are most likely related to the front panel FREQ CAL adjustment. Refer to Section 3 for the FREQ CAL adjustment procedure.

Frequency Accuracy Problem for Bands 1 through 4 (2.4 to 26.5 GHz)

There is a possibility that frequency accuracy problems may appear in bands 1 through 4 only if the error is compensated in band 0 by the FREQ CAL adjustment. If the FREQ CAL potentiometer is adjusted towards an endpoint, troubleshoot for a frequency accuracy problem in all bands.

Frequency Accuracy Problem for All Bands

Frequency accuracy problems that affect all bands are most likely caused by the A8 YO driver being out of calibration. Perform the related adjustments in Section 5 before further troubleshooting.

Swept Frequency Accuracy Problem

A frequency accuracy problem that occurs only during swept frequency modes is typically a delay compensation problem. Refer to the A8 YO driver for further troubleshooting.

POWER CONTROL

Power control problems normally fall into one of the following catagories.

No RF Output Power

Maximum Unleveled RF Output Power (no power control)

Excessive power variation

No RF Output Power

Remove the A4 ALC assembly; the RF output power should go to a maximum level. If not, the trouble is in the RF section. If the RF output goes to maximum, the problem is in the A4 ALC assembly.

Maximum Unleveled RF Output Power

Check leveling in external and meter leveling modes. If power is leveled for these modes, the problem is with the internal detector. Otherwise, refer to the troubleshooting information for the A4 ALC assembly.

Excessive Power Variations

Refer to the troubleshooting information for the A4 ALC assembly.

Low Power

If unable to obtain specified maximum leveled power for frequencies greater than 2.4 GHz, try peaking the power with the front panel PEAK function. Set the HP 83595A to external ALC mode (this opens the ALC loop), press **[SHIFT] [CW]**, and adjust the POWER control to maximize the RF output power over the 2.4 to 26.5 GHz frequency range. If this works, perform the YO/SYTM Tracking adjustments in Section 5. Otherwise refer to the RF section service information for further troubleshooting.

RF SECTION

RF section problems are usually indicated by no RF power, full unleveled RF power, excessive harmonics, or spurious responses. For an RF power problem refer to the Power Control section of this troubleshooting information. For excessive harmonics in band 0 (.01 to 2.4 GHz) or spurious responses, refer to the RF section service information for further troubleshooting.

Table 8-9. HP 83595A Error Codes

Error Code	Function Tested	Operator Initiated Test	Troubleshooting Hints
E001	HP 8350/83595A		Check the RF plug-in connections and cable connections to A3. Do hex data write to front panel and hex data read of A3S1 configuration switch. See E001 Troubleshooting in this procedure for specifics.
E050	Plug-in keyboard		Check PIFLG
E051	Invalid key code	SHIFT 04	See A1/A2 service information for further troubleshooting.
E052	Interval Timer	SHIFT 55	See A3 service information for further troubleshooting.
E053	PIA	SHIFT 55	See A3 service information for further troubleshooting.

HP 83595A RF Plug-In Overall Block Diagram Description

INTRODUCTION

The operating principles of the HP 83595A RF Plug-in are described in two levels. The functional block diagram description describes major functional areas of the instrument. The detailed block diagram description discusses the theory in greater depth, and outlines the breakdown of functions among the various instrument assemblies.

FUNCTIONAL BLOCK DIAGRAM DESCRIPTION

The HP 83595A RF plug-in, used with the HP 8350 sweep oscillator, covers the 0.01 to 26.5 GHz frequency range in five bands with +10 dBm of leveled RF power available up to 20.0 GHz (+4 dBm between 20.0 and 26.5 GHz). In addition to internal leveling, external detectors or power meters can be used to level the RF power. Furthermore, the HP 83595A can sweep power proportional to either frequency or sweep.

The HP 83595A can be broken down into four functional sections:

Digital Control/Front Panel

Frequency Control

Power Control (ALC)

RF Section

The functional description for each of these four functions is described briefly below.

Digital Control/Front Panel

The entire HP 83595A is digitally controlled by the HP 8350 microprocessor. It must be emphasized that nearly all functions are commanded by the HP 8350; very few activities take place without microprocessor intervention.

The digital control section of the HP 83595A is the focal point of all communication between plug-in and mainframe. It receives commands ordered by the microprocessor along the HP 8350's instrument bus. Once in the HP 83595A, these commands are decoded and routed to the appropriate part of the plug-in to control virtually every capability. The digital control section also contains a block of ROM (read only memory), which provides the microprocessor with the constants and program software tailored to the plug-in. The digital control section, then, is the control center for the entire plug-in.

The front panel interface is the communication link between the front panel displays or controls and the rest of the plug-in. It receives and stores information to be presented by the numerical display or annunciators through the digital control block, and continuously refreshes the display. It also receives the user's commands through the front panel pushbuttons and RPG (rotary pulse generator), and sends them back through the digital control block to the HP 8350 microprocessor. Certain analog signals, such as FREQ CAL, pass through the front panel interface directly to the appropriate part of the HP 83595A.

Frequency Control

The frequency control block is responsible for converting the tuning ramp (VTUNE) from the HP 8350 sweep oscillator into drive currents for controlling the YO (yttrium-iron-garnet oscillator) and SYTM switched YIG tuned multiplier). The tuning voltage is offset, scaled and buffered to provide a buffered tuning voltage for both the YO and SYTM drivers. The two drivers each digitally scale and offset the buffered tuning voltage (BVTUNE) to yield tuning voltages that enable the SYTM (which is basically a harmonic generator followed by a tunable bandpass filter) to track the YO fundamental frequency or a multiple. Each driver develops a delay compensation signal that is summed with the scaled tuning voltage on each driver to compensate for delay in the YO or SYTM. Lastly, low-frequency components of external FM (frequency modulation) are filtered and also summed in to produce total YO and SYTM control voltages. However the YO and SYTM are current controlled devices, so current drivers convert the control voltages to drive currents for the YO and SYTM.

The high-frequency FM components cannot be summed in with the drive currents due to the limited dynamic response of the YO and SYTM. The YO contains a separate coil that allows smaller yet faster frequency modulation. The amount of deviation is limited and is within the bandpass characteristics of the SYTM, so the SYTM does not require any frequency control for high-frequency modulation.

The sweep interrupt block monitors the tuning voltage (VTUNE) when the HP 83595A is performing a sweep requiring more than one band. When a tuning voltage corresponding to the end of a band is sensed, these circuits temporarily stop the sweep ramp and interrupt the HP 8350 microprocessor. The microprocessor then prepares the plug-in for the new band, including new scaling and offset values, and continues the sweep.

Power Leveling (ALC)

The power control circuits determine the RF output power level, and ensure that the power is constant across the sweep. A feedback loop detects the RF power level, compares it with a reference voltage, and adjusts modulators in the RF path to correct for amplitude errors.

The power level is digitally programmed from the HP 8350 sweep oscillator. A scaled sweep ramp to provide the power slope or power sweep function is added, yielding a reference power level.

RF detectors provide a voltage proportional to the actual RF power level. This is then compared to the desired reference power level voltage to produce an error voltage. The error is then amplified to drive RF modulators and correct the output power level.

RF Section

The RF section includes the high-frequency microcircuits and their bias components which produce and amplify the RF output.

The 0.01 to 26.5 GHz frequency range is covered in five bands. The YO is the tunable source for all bands. The switched YTM selects the RF output from one of two paths. The upper bands (bands 1 through 4) are obtained by amplifying the direct YO output and then generating harmonics in the SYTM. The SYTM contains a tunable bandpass filter that is tuned to the desired RF output frequency. As a result, the SYTM passes the desired RF output frequency and rejects unwanted harmonics.

Band 0 uses a fixed 3.8 GHz oscillator to mix down the YO output, covering the 0.01 to 2.4 GHz frequency range. When band 0 is selected, the switched YTM provides a straight through path for the 0.01 to 2.4 GHz RF.

Two directional couplers with detectors sense the RF power level and send a voltage to the ALC circuits for internal power leveling.

In Option 002 instruments, a programmable step attenuator is included to provide up to −55 dB of additional output power control range.

Detailed Block Diagram Description

DIGITAL CONTROL/FRONT PANEL

A3 Digital Interface

The A3 digital interface assembly acts as the HP 83595A's distribution center, receiving digital commands from the HP 8350 sweep oscillator and routing them to the appropriate assembly within the plug-in.

The buffer receives the digital control (including timing), data, and address signals from the HP 8350 sweep oscillator's instrument bus. The control and address lines are unidirectional and pass only to the plug-in, whereas the data lines are bi-directional and carry information both to and from the plug-in. A single buffer returns the plug-in flag (L PIFLG) to the HP 8350, indicating that a plug-in front panel key was pushed.

The address decoder provides the major control lines which eventually direct data to the correct part of the plug-in. Address and control lines are decoded to produce enable lines: two for ROM (read only memory); three for the configuration switches/interrupt control; five for the front panel; and two for the remainder of the plug-in assemblies.

The ROM stores program software and constants used by the HP 8350 microprocessor while executing routines dedicated to the plug-in. Two address decoding lines, plus twelve address lines, select the byte of data to be sent back to the HP 8350.

The configuration switch/interrupt control circuits serve a dual purpose. The configuration switch encodes information about the plug-in options used, and certain user-defined parameters. During INSTRUMENT PRESET and power-on, the switch positions are read by the HP 8350 microprocessor, then used to configure the HP 83595A according to the parameters selected. As interrupt control, the circuits monitor the L SIRQ line, and send an interrupt (L PIIRQ) to the HP 8350 to begin each bandswitch. During a bandswitch, the interrupt control is programmed to count down time intervals specified by the microprocessor. At the end of these intervals, the L PIIRQ line is again activated to notify the HP 8350 that the time interval has elapsed.

The RF plug-in interface buffers the data and address lines for use thoughout the rest of the RF plug-in. The data bus is bi-directional, so that the HP 8350 can read information from the A2 front panel interface, A6 sweep control, A7 SYTM driver, and A8 YO driver assemblies. The control lines, which complete the internal bus, come directly from the address decoder. This internal bus sends control messages and data for DACs (digital-to-analog converter) to digital interface circuits on each assembly. These digital interface circuits are essentially buffers between the digital and analog circuits.

A2 Front Panel Interface, A1 Front Panel

NOTE: Due to their strong functional interrelation, the A2 front panel interface and A1 front panel assemblies are discussed together.

The A2 front panel interface and A1 front panel assemblies are primarily responsible for displaying the status and power level of the RF plug-in, and transmitting pushbutton and RPG commands back to the HP 8350 sweep oscillator for processing. Front panel analog adjustments, and the analog 1V/0.5V/GHz rear panel output, are also processed on these assemblies.

The keyboard/display interface performs two functions. As a keyboard interface, it strobes the columns of the pushbutton switch matrix, while sensing the row lines. When a key is pushed, the row line tracks the strobed column line corresponding to that key. The keyboard interface detects this, sets the FLAG line to alert the microprocessor, and transmits the encoded data back to the HP 8350 for processing. As a display interface, the same column strobes are buffered and used to drive the digits of the power display. While a digit is enabled, the appropriate seven-segment data, stored inside the display interface is buffered to drive the segments. The scanning is done at a fast rate to avoid flickering.

The annunciator interface stores data to drive the LED (light emitting diode) annunciators which displays the status of various functions. However, the unleveled annunciator is not digitally controlled, but is driven from a separate unleveled circuit which monitors the ALC assembly.

The power control interface digitally controls several functional areas. Three of the lines are buffered by the attenuator control, which operates the A19 step attenuator in instruments equipped with Option 002. The RF on circuits control the biasing for the A13 YIG oscillator and the A17 amplifier. When the RF is turned off, the bias to these assemblies is removed, shutting off the oscillator and amplifier for minimum RF output.

The frequency tracking amplifier and 1V/0.5V/GHz blocks are the only active analog circuits on the A2 and A1 assemblies. The frequency tracking amplifier monitors the SYTM DRIVE V, a voltage proportional to the RF output frequency. Its output tracks the RF output frequency, and is used to compensate for frequency-dependent non-linearities in the ALC loop. The 1V/0.5V/GHz circuit further processes this signal to produce a rear-panel output supplying 1 VDC or 0.5 VDC per GHz of output frequency for use with external equipment.

Miscellaneous front panel controls must pass through the A1 and A2 assemblies. The RPG produces pulses when rotated, and sends them directly back to the HP 8350 sweep oscillator to be decoded and processed to adjust the power or fine-tune the SYTM bandpass frequency. The FREQ CAL adjustment is used to fine-tune the band 0 output frequency to correct for drift or error in the A11 cavity oscillator frequency. The EXT/MTR ALC CAL adjusts the absolute power level when external detector or power meter leveling is used.

FREQUENCY CONTROL

The frequency control section of the plug-in is responsible for determining the actual RF output frequency. Based on the tuning voltage VTUNE and digital data, the correct drive currents are developed for tuning the A13 YIG oscillator and A12 YIG tuned multiplier. FM is also processed in these circuits.

A6 Sweep Control

The A6 sweep control assembly scales and offsets the tuning voltage from the HP 8350 sweep oscillator to provide a series of 0 to −10V ramps (one ramp for each band) during a multiband sweep. For single band sweeps, the A6 sweep control assembly just buffers and inverts the the 0 to 10V VTUNE ramp from the HP 8350.

The bandswitch comparator and sweep control/interrupt logic sections monitor the buffered tuning voltage. When the sweep ramp requires a change of band, this circuit issues "stop sweep" and blanking pulse requests. At the same time, an interrupt is sent to the mainframe through the A3 assembly, requesting service for the bandswitch. After this point, the microprocessor completes the bandswitch sequence through the sweep control circuits.

SRD and PIN switch bias circuits control the switched YTM for band selection and SRD (step recovery diode) biasing. The PIN SW output controls a PIN diode switch in the SYTM to select either a straight through path for band 0, or SYTM operation for bands 1 through 4. The SRD BIAS output optimizes the SRD biasing for the frequency and power level of operation.

A8 YO Driver, A9 Reference Resistor Assembly

The A8 YO driver assembly scales and offsets the buffered tuning voltage from the A6 sweep control assembly and converts it to a current for controlling the A13 YIG oscillator frequency.

The buffered tuning voltage, BVTUNE, is scaled offset and summed with various correction signals to produce the tuning current for the A13 YIG oscillator. The scaling and offsetting is used to change the frequency range of the YO depending on the band of operation. For each band, the 0 to 10V ramp must tune the YO over a different frequency range as shown in Table 8-7.

Table 8-7. YO Frequency Bands

Band	YO Frequency Range (GHz)
Band 0	3.81 to 6.2 GHz
Band 1	2.4 to 7.0 GHz
Band 2	3.5 to 6.75 GHz
Band 3	4.5 to 6.67 GHz
Band 4	5.0 to 6.63 GHz

The scaling and offset DACs are also used to compensate for differences in oscillator sensitivities. The amount of scaling and offset is set by the frequency cal switches. At power on or INSTRUMENT PRESET, the status of the cal switches is read by the HP 8350 and stored in RAM (random access memory). This information is then used along with frequency range (band) information to program the DACs. The −10V Reference generates a stable voltage source used as a reference on the A6 sweep control, A7 SYTM driver, A8 YO driver, and A4 ALC assemblies.

The delay compensation circuit produces signals to compensate for time delay in the YO response. The coils in the YO are used to set up a strong controlled magnetic field to control the RF frequency. Due to inductive reactance of the electromagnets, there is a delay between the applied voltage and resultant current flow through the coils. The delay compensation circuit monitors the scaled tuning voltage, and from its amplitude and slope produces a signal added to the YO DRIVE V to compensate for swept frequency errors that would occur because of the response delays.

The +20V tracking circuit monitors the +20V supply, producing an output which follows this voltage. Since the current through the YO is referenced to this supply, this prevents power supply drift or noise from creating frequency errors.

The summing junction adds together the scaled tuning voltage, offset, delay compensation, +20V tracking voltage, and offset compensation, plus the front-panel FREQ CAL in band 0. The YO LO FM from the A5 FM driver (described below) is also added. The product is the YO DRIVE V, a signal proportional to the YO frequency.

The remainder of the A8 circuits and the A9 components convert the YO DRIVE V to a current to control the YO frequency. The final current drive transistor is controlled by the A8 assembly. The current through this transistor, and hence the YO, generates a proportional voltage across the chassis mounted reference resistor, which is monitored and compared to the YO DRIVE V. Any errors between the two are corrected in a closed loop, producing a current proportional to the YO DRIVE V. Compensation elements (Comp) correct for nonlinearities in the YO. If the YO is replaced, this section of circuitry requires changing.

In CW mode, a relay connects a large capacitor across the YO's coil. The capacitor resists changes in the YO current to reduce residual FM noise.

The frequency cal switches set the frequency end-point accuracy. These switches are set when the plug-in is calibrated, and are read by the HP 8350 during INSTRUMENT PRESET or initial power on. This information is used to program the scale and offset DACs.

A7 SYTM Driver, A9 Reference Resistor Assembly

The A7 SYTM driver assembly scales and offsets the buffered tuning voltage from the A6 sweep control assembly and converts it to a current for controlling the A12 switched YIG tuned multiplier frequency for bands 1 through 4.

The buffered tuning voltage, BVTUNE, is scaled, offset and summed with various correction signals to produce the tuning current for the A12 SYTM. The scaling and offsetting is used to change the frequency range of the SYTM depending on the band of operation. For each band, the 0 to 10V ramp must tune the SYTM over a different frequency range as shown in Table 8-8.

Table 8-8. SYTM Frequency Bands

Band	SYTM Frequency Range (GHz)
Band 0	Not Used
Band 1	2.4 to 7.0 GHz
Band 2	7.0 to 13.5 GHz
Band 3	13.5 to 20.0 GHz
Band 4	20.0 to 26.5 GHz

The scaling and offset DACs are also used to compensate for differences in SYTM sensitivities. The amount of scaling and offset is set by the frequency cal switches. At initial power on or INSTRUMENT PRESET, the status of the cal switches is read by the HP 8350 and stored in RAM. This information is then used along with frequency range (band) information to program the DACs. The −10V reference from the A8 YO driver is a stable voltage source used as a reference for the offset DAC.

The delay compensation circuit produces signals to compensate for time delay in the SYTM response. The coils in the SYTM are used to set up a strong controlled magnetic field to control the RF bandpass frequency. Due to inductive reactance of the electromagnets, there is a delay between the applied voltage and resultant current flow through the coils. The delay compensation circuit monitors the scaled tuning voltage, and from its amplitude and slope produces a signal added to the SYTM DRIVE V to compensate for swept bandpass frequency errors that would occur because of the response delays.

The +20V tracking circuit monitors the +20V supply, producing an output which follows this voltage. Since the current through the SYTM is referenced to this supply, this prevents power supply drift or noise from creating bandpass frequency errors.

The summing junction adds together the scaled tuning voltage, offset, delay compensation, +20V tracking voltage, and offset compensation. The SYTM LO FM from the A5 FM driver (described below) is also added. The product is the SYTM DRIVE V, a signal proportional to the RF output frequency.

The remainder of the A7 circuits and the A9 components convert the SYTM DRIVE V to a current to control the SYTM bandpass frequency. The final current drive transistor is controlled by the A7 assembly. The current through this transistor, and hence the SYTM, generates a proportional voltage across the chassis mounted reference resistor, which is monitored and compared to the SYTM DRIVE V. Any errors between the two are corrected in a closed loop, producing a current proportional to the SYTM DRIVE V. Compensation elements (Comp) correct for nonlinearities in the SYTM. If the SYTM is replaced, this section of circuitry requires changing.

The frequency cal switches set the SYTM's frequency end-point accuracy for tracking the YO frequency. These switches are set when the plug-in is calibrated, and are read by the HP 8350 during INSTRUMENT PRESET or power on. This information is used to program the scale and offset DACs.

P/O A5 FM Driver

The A5 FM driver assembly splits the external FM signal, passed through the mainframe, into two frequency ranges (low frequency and high frequency). The low frequency modulation is added to the main coil tuning voltages for both the YO and SYTM; the high frequency modulation is routed to a separate coil inside the YO dedicated to high-frequency FM.

The external FM input is routed to the A5 FM driver assembly, where it splits into two paths. One path is low-pass filtered, removing high frequency components; the other path is high-pass filtered, removing low frequency components. The filters are matched in stop-band response, such that one picks up where the other leaves off. Two sensitivity select circuits determine the FM sensitivity (RF output deviation of −20 or −6 MHz/volt) and select either crossover or direct coupling. The low frequency path is further divided into two paths, one for driving the YIG oscillator and the other for the SYTM. Since, for bands 2 , 3, and 4, the RF output is actually a harmonic of the YO frequency, the FM sensitivity of the YO (in relation to changes in the RF output frequency) varies between bands. Also, if the rear panel AUX OUTPUT (YO fundamental frequency) is used for phaselocking, the FM sensitivity for the SYTM varies between bands. Thus, variable gain amplifiers (controlled by band select logic) scale the FM driver outputs according to the band of operation and phaselock source (as selected by the A3S1 configuration switch).

The YO LO FM is eventually added to the YO DRIVE V, and modulates the YO output frequency through its main coils. The SYTM LO FM is added to the YTM DRIVE V, and modulates the SYTM bandpass frequency through its main coils. Thus, for low frequency modulation, both the YO and SYTM track each other in frequency.

The YO and SYTM main coils cannot respond to fast deviations due to inductive and magnetic delays. Therefore, the YO contains a separate, small, but higher frequency response "FM coil". The HI FREQ FM is sent to this coil, allowing limited high-frequency modulation. Since this modulation is limited, and does not extend beyond the bandwidth of the SYTM, no high-frequency modulation is required for the SYTM.

ALC/POWER CONTROL

The A4 ALC assembly, and parts of the A5 FM driver assembly, are responsible for power level control. Power leveling is accomplished by detecting the output RF power level, comparing it to a fixed reference voltage, and adjusting RF modulators to correct for power errors. This results in constant RF power level across the entire sweep. The absolute RF power is digitally controlled, and can be set between +10 and −5 dBm. (Instruments with Option 002 use an RF step attenuator to achieve power control down to −60 dBm. However, this is not part of the leveling loop.) The power sweep and power slope functions are obtained by adding a scaled voltage ramp offset to the reference power level.

A4 ALC Assembly

The A4 ALC assembly receives its inputs from the various detectors, and selects one of them for leveling. The sources include DC1 directional detector (band 0), CR1 detector (bands 1 through 4), the EXTERNAL INPUT (external negative detector), and a fourth position which inverts the polarity of the external input (power meter detection). The selected detector voltage is proportional to the peak RF amplitude. The input sample and hold stores the detected level during pulse modulation. This prevents subsequent circuits from saturating when the RF power goes low during blanking or pulse modulation. The logger amplifier produces a voltage proportional to the log of peak RF amplitude, and essentially represents the RF power level in dB.

The reference, or desired, power level is established digitally by a 12-bit DAC, scaling the −10V REF from the A8 assembly. This establishes a voltage proportional to the desired output level in dBm. The EXT AM signal from the HP 8350 sweep oscillator, and the PWR/SWP COMP signal from the A5 FM driver assembly (described below), are summed in to produce PWR REF, a voltage proportional to the desired RF output power.

The second summing junction adds the EXT CAL input from the front panel. This offset voltage is used to calibrate absolute power when external leveling is used. The final product of the power reference chain is a reference voltage representing the desired RF output amplitude.

The ultimate goal of the leveling loop is to make the actual RF power equal to the desired RF power. A third summing junction compares the voltages representing these two quantities, and yields a signal representing the error between actual and desired power. This error voltage is sampled and held during pulse modulation to prevent subsequent circuits from saturating. The held error signal is amplified, and the RF blanking signal added to switch off the RF power during bandswitch, retrace, and internal square wave modulation (from the HP 8350), without saturating any other components in the path. An additional circuit monitors the input to the modulator drivers, and lights a front panel unleveled LED if this voltage exceeds the normal range for leveled power.

P/O A5 FM Driver

The A5 FM driver assembly includes circuits to produce the PWR/SWP COMP signal added to yield the PWR REF. The power sweep function is achieved by scaling the VSW sweep voltage with a DAC. By programming the appropriate scale factor, a voltage representing dB/GHz or dB/Sweep is produced.

The ALC compensation is a "four breakpoint, adjustable slope network" which compensates for fixed frequency-dependent nonlinearities in the RF path, typically the couplers and detectors. Its input is FREQ TRK V, a voltage proportional to frequency. This signal drives an array of four transistors, and their outputs are summed together to yield the ALC compensation signal. The gain of each transistor, and the voltage at which they conduct, are adjustable. A ninth adjustment adds the FREQ TRK V directly. In this way, a complicated compensation function, approximated by five straight lines, is produced. (An additional adjustment on the A4 assembly adds another compensation signal proportional to frequency for band 0 only.)

The power sweep DAC adds a ramp voltage to the power reference signal when the power sweep or power slope functions are activated. Its input, VSW, is a sweep ramp that essentially tracks the tuning voltage, but always runs from 0 to 10 VDC. A digitally programmable multiplying DAC scales this voltage according to the dB/SWP or dB/GHz value selected. (If these functions are disabled, the DAC is set to its minimum value.) This ramp is added to the ALC compensation signal described above, and added to the power reference signal on the A4 assembly.

RF SECTION

The RF section includes the microcircuits and their bias boards that produce the actual RF output power. These components include A11 through A19, AT1, DC1, DC2, and CR1.

The A13 YIG oscillator is the fundamental frequency-controllable microwave source for the HP 83595A RF plug-in, ranging 2.4 to 7.0 GHz. The YO's frequency is determined by the current flowing through large electromagnetic coils inside, supplied by the A8 and A9 assemblies. Due to the response time limitations of the main coils, a smaller coil with a much faster response but limited range is used to modulate the output frequency when faster rates are needed.

The A16 modulator/splitter splits the YO output into two paths (one for band 0 and the other four bands 1 through 4), provides pulse modulation for all bands, provides amplitude control for leveling in bands 1 through 4, and couples part of the YO output to the rear panel AUX OUTPUT connector.

For bands 1 through 4, the fundamental YO output is amplified by the A14 power amplifier. The AT1 isolator provides 20 dB of isolation between the power amplifier and the A12 SYTM. The fundamental YO frequency from the isolator is applied to a SRD (step recovery diode) in the SYTM. The SRD passes not only the fundamental frequency, but also generates an output that is rich in harmonics. The YIG tuned filter is a bandpass filter that is tuned to the desired RF output frequency by the A7 SYTM driver. Thus, the SYTM uses the YO fundamental frequency to generate an RF output corresponding to either the YO fundamental frequency (band 1).

For band 0, the A16 modulator/splitter output (3.81 to 6.2 GHz) to the A18 modulator/mixer is mixed with the fixed 3.8 GHz output of the A11 cavity oscillator, yielding the heterodyned band 0 output from 0.01 to 2.4 GHz. Power control and leveling is accomplished by modulating the 3.8 GHz input before the mixer, internal to the A18 modulator/mixer.

The A17 amplifier boosts the mixed-down low-power output from the A18 assembly. The amplifier also serves to remove unwanted high-frequency mixing products. The A17A1 amplifier bias assembly is connected directly to the microcircuit, has no adjustable or replaceable parts, and is not separately replaceable.

The DC1 directional detector uses a broadband resistive bridge to couple off a portion of the RF energy. This energy is rectified and filtered to provide a detected output for band 0 leveling.

The A15 DC return allows SYTM bias currents to pass to ground, while preventing them from affecting other circuits.

For band 0, the A12 SYTM provides a straight through path for the 0.01 to 2.4 GHz RF.

The DC2 directional coupler directs a portion of the RF energy to CR1 detector, producing a voltage proportional to the RF power level for leveling in bands 1 through 4. Although the low-frequency (band 0) output must pass through DC2, this coupler plays no part in band 0 leveling.

The RF output is finally directed to the front panel RF OUTPUT connector. On instruments with Option 004, different cabling takes the output to the rear panel connector. On instruments with Option 002, the A19 RF step attenuator is included, providing from 0 to 55 dB of attenuation in 5 dB steps. This attenuated output is then routed to the front panel connector (Option 002 only) or rear panel connector (Option 002 with Option 004).

Troubleshooting the A1 Front Panel and A2 Front Panel Interface Assemblies

NOTE: The entire plug-in depends on the A3 digital interface assembly for control, address, and data signals. Before troubleshooting the A1/A2 assembly, verify proper functioning of A3. See Overall Troubleshooting for verification procedures.

NOTE: Troubleshooting information for both the A1 front panel and A2 front panel interface assemblies is combined. All reference designators refer to the A2 assembly unless otherwise noted.

INTRODUCTION

Visually inspect the cabling inside the plug-in for damage or loose connections. Check that the large ribbon cable connections (W29, P1, and P2) are properly seated over the correct pins on Motherboard A10J2 and A3 digital interface A3J1. (On plug-ins with Opt 002 Attenuator, W29P2 may be difficult to see). Check that W3 ribbon cable connections are securely seated over A10J1 and A2J1.

Check power supplies to the front panel: +5V at A10XA3, pins 6 and 7. Then check continuity between these points and A10J1, pin 2.

ERROR CODES

Error codes E050 and E051 indicate a communication problem between the front panel interface assembly and the HP 8350 microprocessor. Code implications and further troubleshooting hints are discussed later, under the subheading Keyboard.

DIGITAL DISPLAY

The plug-in display can be directly commanded by the HP 8350 microprocessor using hex data write (see paragraph Operator-Initiated Tests for an explanation of hex data write). An effective test pattern can be input which toggles the states of adjacent segment lines. The pattern should detect shorted lines or defective flip-flops.

Press **[CW]**	
[SHIFT] [0] [0]	hex data mode
[2] [MHz] [0] [0]	address location 2d00 (U6)
[M2]	hex data write
[5][5] [.][.] [5][5] [.][.]	hex bytes: 55 AA 55 AA

The pattern seen in the plug-in display should match that shown in Figure 8-9. If the patterns match, the plug-in display is working properly, and any failures are probably due to the mainframe or plug-in ROM.

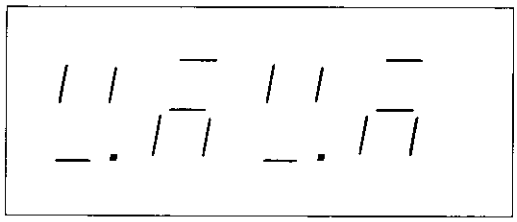


Figure 8-9. Display Test Pattern

If any of the digits in the display window appear to be stuck, or if the above test fails, remove the front panel and check the 200 kHz SCAN CLK signal at U6, pin 3. If no signal is detected, trace the line back through U4B to the A3 digital interface assembly.

Then, check the DIG1 through DIG4 lines for sequential low pulses. These can be accessed at the back of A1/A2 interconnect A2P1, pins 3, 5, 7, and 9. If they are absent, trace the problem back to U6.

The seven-segment lines, Ca through Cg, and Cdp, can be tested by programming the test pattern in Figure 8-9, then verifying activity at A2P1. Trace any problems back to U6.

To check for burned out display LEDs:

Press **[CW]**	
[SHIFT] [0] [0]	hex data mode
[2] [MHz] [0] [0]	address location 2d00 (U6)
[0][0] [0][0] [0][0] [0][0]	hex bytes: 00 00 00 00

All segments, with decimal points, should light up.

Display problems may be due to A3 digital interface failures. Check the L FP1 line at U6, pin 11, using hex data rotation write.

Press **[CW]**	
[SHIFT] [0] [0]	hex data mode
[2] [MHz] [0] [0]	address location 2d00 (U6)
[M4]	hex data rotation write

The data lines should also be checked in this mode. (Input and output patterns are illustrated in Figure 8-2.) Trace any problems back through A3.

ANNUNCIATORS

Check for burned out LEDs by pressing and holding the **[INSTR PRESET]** key. All LEDs should light, except for units indicator (dBm, dB/GHz, and dB/Swp), and UNLEVELED annunciators.

Use hex data write as follows, to check annunciator control capability.

Press **[CW]**	
[SHIFT] [0] [0]	hex data mode
[2] [dBm] [0] [0]	address location 2E00 (U7)
[M2]	hex data write
[5] [5]	hex data 55
[.] [.]	hex data AA

Alternate between 55 and AA, and check that each addressed annunciator is lit for one case and out for the other (excluding the UNLEVELED annunciator). Plug-in annunciators are controlled by two locations. Repeat the procedure for address location 2E80 (U5).

If these tests fail, remove the front panel assembly to expose the A2 assembly. Use hex data rotation write as follows:

Press **[SHIFT] [0] [0]**	
hex data mode	
[2] [dBm] [0] [0]	address location 2E00 (U7)
[M4]	hex data rotation write

Check the enable lines for activity. The data bus inputs and latched outputs should also be checked for the patterns illustrated in Figure 8-2. Units annunicators are buffered by inverters, and drive current through the LED to ground rather than sinking current from +5V. The outputs of these buffers can be checked during hex data rotation write.

The UNLEVELED light is driven by pulse-stretching timer, U12A, which is disabled by U9A during retrace. Check that U9, pin 3, is high during retrace (approximately +4 VDC), and low during forward sweep. The UNLEVELED light should be lit when the available power is insufficient for leveling to the desired reference level (typically several dB beyond specified maximum leveled power).

If the UNLEVELED light is not functioning properly:

Press **[RF BLANK]** (light on)
[RF] (light off)

In this mode, L UNLVL, J1-12, should be low during forward sweep, and high during retrace. Connect oscilloscope channel B to the HP 8350 SWEEP OUT, and select the A vs B mode to externally sweep the oscilloscope with the HP 8350 sweep output. Check the input (pin 6) and output (pin 5) of timer U12A. The output of U12 goes high for an initial low pulse at the TRIGGER input (T), and remains high for a period of approximately 50 milliseconds. Subsequent trigger pulses, occurring within the timing cycle, will not affect the output. However, if the TRIGGER input remains low for a longer duration than the timing cycle, the output will remain high for the duration of the TRIGGER signal. If no TRIGGER signal is present, check diodes CR6 and CR7, or trace the problem back to the A4 assembly.

KEYBOARD

The keyboard matrix is scanned continuously by U6. This LSI (large-scale integration) device continously strobes the column lines, senses the row lines for depressed keys, eliminates contact bounce, stores the key code internally, and flags the HP 8350 to recover the key code. Troubleshooting is difficult because the device is so complicated, but it is worthwhile to check all signals to and from U6, probing directly on the pins of the chip, before replacing it.

Error codes **E050** and **E051** generally indicate U6-related problems:

E050 occurs when the microprocessor receives a flag (L PIFLG) from the plug-in (indicating a front panel key was pressed), but cannot recover the keycode (indicating that the key was NOT pressed). Check the FLAG output from A2U6 (accessible at A3P1-42). It should be TTL low, approximately 0 volts. Pressing a front panel pushbutton should result in a very rapid pulse. If the line appears to be locked high, replace A2U6. If it is good, check inverter A3U10F (accessible at A3J1-39) to see if it is locked low.

E051 occurs when the key code received by the microprocessor cannot be decoded. This indicates a failure in A2U6 or a bad row sense line. If the row sense lines are good, troubleshoot the keyboard matrix with a continuity checker.

To troubleshoot the plug-in keyboard matrix, initiate the key code test. Press **[SHIFT] [0] [4]**. Thereafter, when pressing any plug-in front panel key, the appropriate hexadecimal key code should appear in the mainframe FREQUENCY/TIME display window. The key codes are given in Table 8-8.

Table 8-8. Plug-In Key Codes

Key	Code	Column	Row
POWER SWEEP	9b	0	0
POWER LEVEL	9A	0	1
SLOPE	99	0	2
RF	98	0	3
CW FILTER	92	1	1
NOT USED	91	1	2
NOT USED	90	1	3
NOT USED	8b	2	0
NOT USED	8A	2	1
NOT USED	89	2	2
NOT USED	88	2	3
INT	82	3	1
EXT	81	3	2
MTR	80	3	3

If depressing a key results in the wrong keycode being displayed, read the associated column and row lines. Troubleshoot with a continuity checker. If the matrix lines are good, suspect A2U6.

No keycode is defined for Row 0 at Column 1 or Column 3. A problem in this area of the matrix may result in Error Code E051.

If this test indicates further troubleshooting, remove the front panel to make A2 accessible while connections between the front panel, plug-in, and mainframe are still intact.

If the numerical display is blank, check power supplies on A2.

Check U6, pin 3, for the 200 kHz SCAN CLK signal. If it is missing, trace the problem back through U4B to the A3 digital interface assembly.

Initiate hex data rotation write and check the L FP2 line for activity:

Press **[SHIFT] [0] [0]**	hex data mode
[2] [MHz] [0] [0]	address location 2d00 (U6)
[M4]	hex data rotation write

The data line inputs should also be checked in this mode. The pattern should match that shown in Figure 8-2.

Check the COL0 through COL3 lines for sequential low pulses, as shown in Figure 8-10.

If the patterns are absent, but the 200 kHz clock is present, the problem is probably U6. Ensure that problems in U4B or the A1 assembly are not tying the lines down.

If the column strobes are present, probe both the column and row corresponding to the key in question at U6. Observe the traces while pushing the button. The two lines should track each other. If they track, but the microprocessor can't read the codes from U6, and the data bus is good, the problem is probably in U6.

If row and column do not track, separate the A1 and A2 assemblies and troubleshoot the keyboard matrix with a continuity tester.

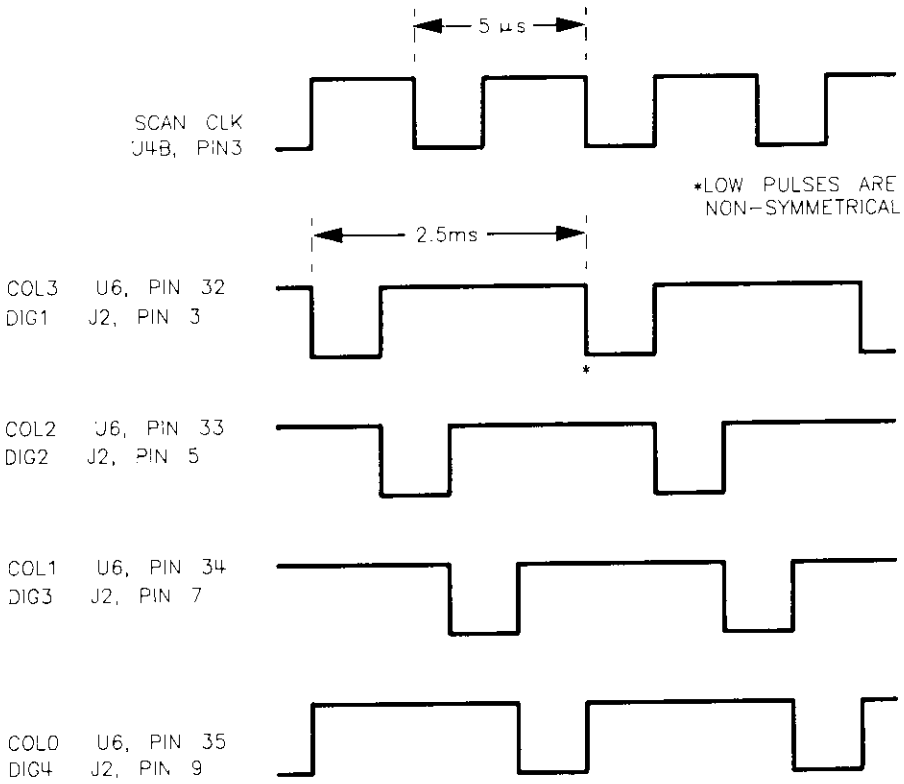


Figure 8-10. Column Strobing

ROTARY PULSE GENERATOR (RPG)

The RPG is a means of converting rotational information into digital signals which can be read by the microprocessor. The hardware components needed to decode the plug-in RPG (counter and sign latch) are located on the HP 8350 A2 front panel interface assembly. Some failures which appear to be in the plug-in RPG, (e.g., "run-away" POWER display or a locked-up sign) are likely to be caused by failures in the HP 8350.

If the plug-in RPG appears to be dead, remove the bottom cover of the HP 8350 and probe A10J1, pins 34 and 36. Check for the waveforms shown in Figure 8-11, while slowly rotating the RPG. If the signals are present, trace the PIRPGA and PIRPGB lines through the HP 8350 to the mainframe A2 assembly. Refer to HP 8350 A2 service information for more details.

If the signals are absent in the plug-in, check for the +5V at A10J1, pin 2. Then remove the front panel and check for +5 VR directly at the point where the RPG leads are soldered to the A1 front panel assembly. Then probe the two RPG output leads for the waveforms in Figure 8-11. If they are absent, check that the output leads are not shorted to ground. If not, replace the RPG.

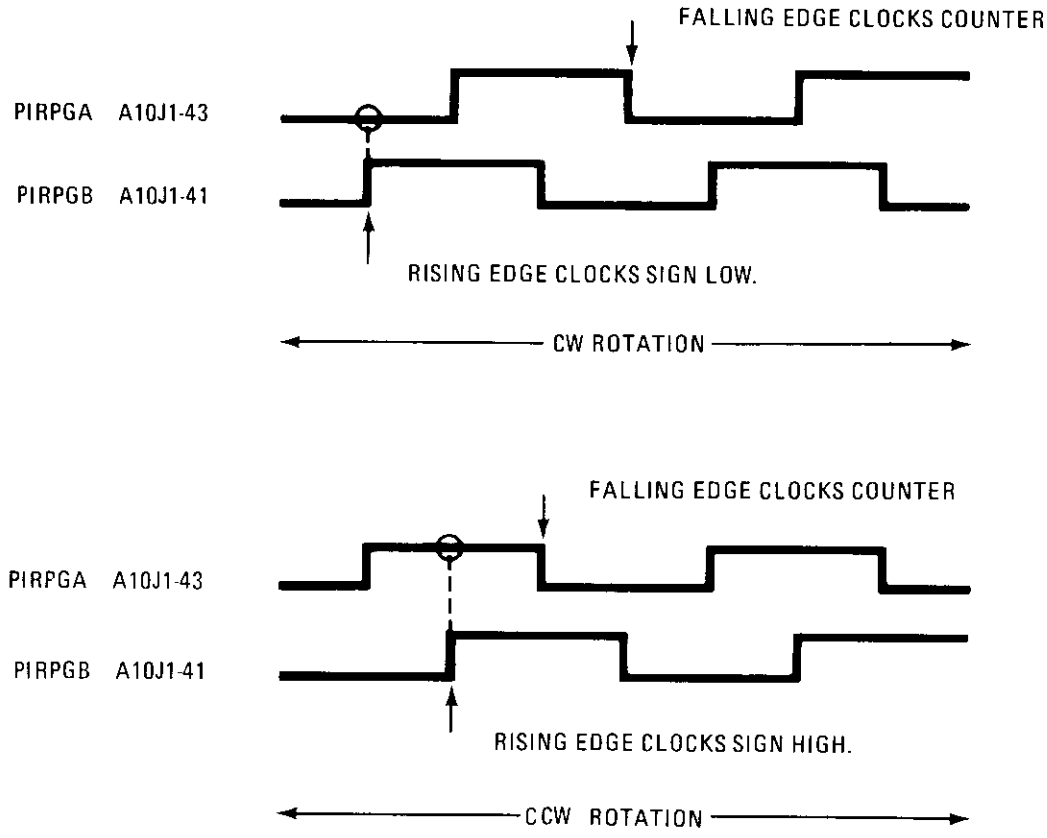


Figure 8-11. RPG Pulse Train

ANALOG CIRCUITRY

Analog circuitry on the A2 front panel interface processes the SYTM DRIVE V signal to produce the 1V/0.5V/GHz rear panel output and FREQ TRK V, used in the ALC loop.

Check that the SYTM DRIVE V signal is present at TP1. It should resemble the waveform shown in Figure 8-12. If it doesn't, trace the problem back to the A7 SYTM driver assembly.

If it is present, check TP3 for the waveform shown in Figure 8-13. If it is present on the A2 assembly, but FREQ TRK V is missing on the A4 and A5 boards, probe the emitter of Q3 for the same waveform offset by approximately 0.6 VDC.

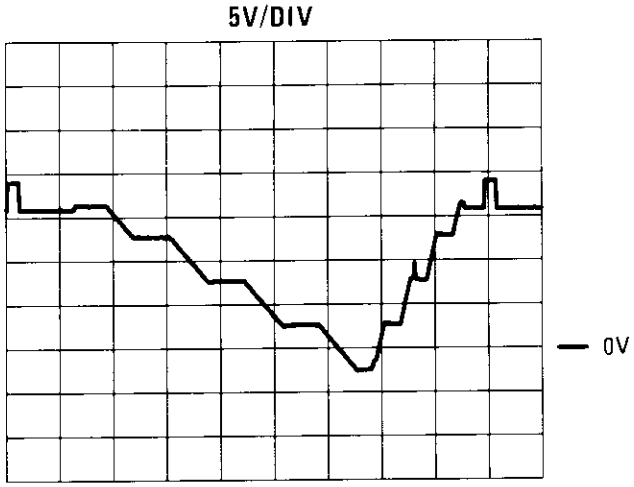


Figure 8-12. SYTM Drive V (A2TP1)

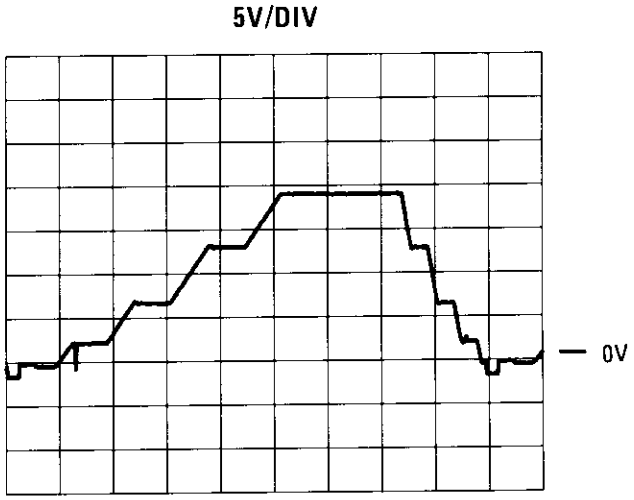


Figure 8-13. Frequency Voltage (A2TP3)

Analog switches U9B, U9C, and U9D are controlled by latch U8. These switches apply an offset to FREQ TRK V in band 0 only, and turn off FREQ TRK V when external leveling. These can be exercised by using a hex data write command.

Press **[CW]**	
[SHIFT] [0] [0]	hex data mode
[2] [BKSP] [0] [0]	address location 2F00 (U8)
[M2]	hex data write
[BKSP] [BKSP]	hex byte FF

Note that these switches are not identical. U9B is open for logic 0, while U9C and U9D are closed.

The 1V/0.5V/GHz amplifier adds one more stage of gain and offset to FREQ TRK V, producing a scaled tuning ramp to follow the RF output frequency at exactly 0.5 VDC per GHz or 1 VDC per GHz depending on the switch position of A2S1. Check the rear panel 1V/0.5V/GHz BNC output jack for a ramp. Be sure that A2S1 is in the open position. If it is absent, check TP2 for the waveform shown in Figure 8-14. If there is no signal at TP2 but there is a ramp at TP3, the problem is in U1A. Return A2S1 to its original configuration.

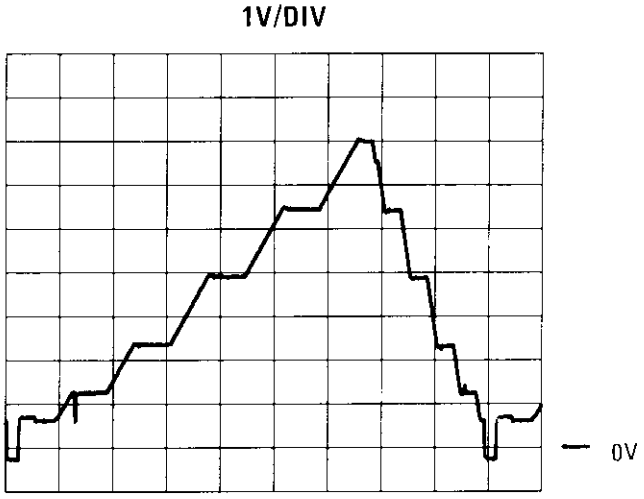


Figure 8-14. 1V/GHz Output Waveform

RF POWER CONTROL LATCH

U8 stores commands for the RF step attenuator (Option 002 only) and the RF ON line, which supplies −10V bias for components in the RF path. It also controls analog switches used for the signals mentioned above.

Hex data rotation write can be used to verify the outputs of U8.

CAUTION

In Option 002 plug-ins, disconnect the attenuator cable at A2J3 before hex data rotation write. The bit pattern shifts too fast to actuate the attenuator properly, and may damage it.

Initiate the check as follows:

Press **[SHIFT] [0] [0]**	hex data mode
[2] [BKSP] [0] [0]	address location 2F00 (U8)
[M4]	hex data rotation write

Check L FP5 line for activity. Check data lines for patterns illustrated in Figure 8-2.

To check the RF ON relay, K1, make the same key entries as above, except enter **[M2]** for hex data write. Then alternate between data inputs: **[0] [0]** and **[BKSP] [BKSP]** (FF). The RF ON line should toggle from 0 VDC to −10 VDC. If there is no change, check U8, pin 5, for high and low levels. If the output is locked high, check the protection diode, CR3, before replacing U8. However, if CR3 is open, U8 may be damaged by actuating the relay. If the output at pin 5 is locked low, replace U8. If U8 pin 5 changes levels properly, replace relay K1.

MISCELLANEOUS

The FREQ CAL and EXT/MTR ALC CAL offsets are generated by A1 potentiometers, with the wipers running between +10 VDC and −10 VDC. If the signals are absent, check for the +10V and −10V supplies. If the offset voltages still cannot be produced, replace the defective potentiometer, R3 or R4.

A1 Front Panel and A2 Front Panel Interface, Circuit Description

GENERAL

The A1 front panel and A2 front panel interface assemblies provide communication between the instrument and the user. Keyboard and RPG commands are transmitted to the HP 8350 microprocessor for appropriate action. The numerical power level and plug-in status information is displayed on front panel LEDs. External ALC power calibration and frequency calibration inputs are passed through the front panel to the plug-in. Also, the programmable step attenuator controls and the 1V/0.5V/GHz outputs are processed on the A2 assembly.

KEYBOARD

Push Button Switch Matrix A1, Block J
Keyboard/Display Interface A2, Block A

The push button keyboard is arranged in a column-row matrix. The column lines are sequentially strobed, while the row lines are simultaneously sensed to determine when a key is depressed. The matrix scanning and sensing, along with the debouncing functions, are performed by U6, the keyboard/display interface. U6 is a large-scale integrated device capable of monitoring the keyboard without continual attention from the HP 8350 microprocessor. When a key is depressed, U6 eliminates contact bounce, encodes and stores the column/row information in an internal register, and sets the FLAG line. When the microprocessor detects the flag, the keyboard codes are read from U6 and processed.

POWER DISPLAY

Power Display A1, Block K
Keyboard/Display Interface A2, Block A
Power Display Driver A2, Block D

The numerical power display is a four-digit, seven-segment LED configuration. Only one digit is enabled at any one time by the DIGn lines. These lines are continuously scanned by the buffered keyboard column lines from U6, providing a flicker-free display. The seven-segment and decimal point information corresponding to the enable digit is provided by buffered lines from U6. When the display is updated, data is sequentially written into U6 from the microprocessor and stored internally. U6 is then responsible for scanning the display without requiring constant attention from the HP 8350.

UNLEVELED ANNUNCIATOR DRIVER

LED Annunciators A1, Block H
Unleveled Annunciator Driver A2, Block F

U12B is one half of a dual timer serving as a triggered monostable, or one-shot. When the unleveled condition is detected, the trigger line pulses low. The monostable then goes high for a 50 millisecond period beginning at the trigger's falling edge. This ensures that the LED will stay lit long enough to be visible when triggered by a very narrow pulse. When L BP2 (Low=Blanking Pulse) is low and U9A is open, the trigger input is held high by CR6 so that the monostable cannot be triggered during retrace.

LED ANNUNCIATOR LATCH

LED Annunciators A1, Block H
LED Annunciator Latch A2, Block B

Octal latches U7 and U5 control the various front panel and push button LED annunciators. When clocked by the FP3 or FP4 line from the A3 digital interface assembly, the latches store a byte of data from the data bus, and light the LEDs determined by the bit pattern (Low=ON).

RF POWER CONTROL LATCH A2, Block C

U8 is an octal latch which stores six of eight data bits when clocked by the FP5 line from A3. These data lines control the programmable step attenuator (Option 002), RF on/off relay, and 1V/0.5V/GHz circuitry. The step attenuator has 5, 10, 20, and 20 dB pads internally, combining to provide up to 55 dB of attenuation in 5 dB steps. BD0, BD1, and BD2 are the data signals for U10. An extra inverting stage is provided by U13 so that the same data signals can be used to create the enable (ENn) and disable (DISn) signals. The attentuator is a latching relay type, so that current is drawn only during switching. When the plug-in RF OFF is selected, relay K1 opens and shuts down the RF path. When K1 is open, bias is removed from the low band RF amplifier (to increase on/off ratio), and the YIG oscillator and the RF is shut off. CR3 protects U8 from high transient voltages when K1 turns off.

1V/0.5V/GHz

Frequency Tracking Amplifier A2, Block E
1V/0.5V/GHz Amplifier A2, Block G

U1B scales and offsets the SYTM tuning voltage for the 1V/0.5V/GHz circuit, providing a 0 to 6 volt ramp proportional to frequency. Switch U9D introduces an additional offset in the low frequency band only, since the RF output frequency is mixed down from a higher YO frequency. When internal leveling is used, U9C passes this voltage through Q3 to the A4 ALC and A5 FM driver assemblies where it is used to compensate for frequency-dependent nonlinearities in various elements of the leveling loop. When external leveling is selected, U9B turns off Q3 to disable the compensation circuitry.

U1A further offsets and scales this voltage to provide either 0.5V/GHz or 1V/GHz. When A2S1 is closed 0.5V per GHz frequency reference output is selected. U1A is now scaled to provide 0.5V/GHz up to 26.5 GHz. When A2S1 is open 1V per GHz is selected up to 19 GHz. At this frequency U1A approaches the limit of its power supplies (current source Q2 increases this upper limit beyond the level U1A alone can produce). The output is scaled regardless of the band chosen.

RPG (Rotary Pulse Generator) A1, Block I
External Leveled Power Calibration Control A1, Block M
Frequency Calibration Control A1, Block L

The RPG provides control as selected by the keys below it (POWER SWEEP, POWER LEVEL, PEAK, SLOPE), and encodes rotation into digital form for the microprocessor to use, providing a digitally-compatible control with an analog "feel". The two RPG lines pass directly to the HP 8350's A2 front panel interface assembly, passing through both plug-in and mainframe motherboards. CAL adjustment introduces an offset to the leveling loop to match absolute RF power output to external leveling devices. The FREQ CAL adjustment is used to calibrate the RF frequency for band 0 (.01 to 2.4 GHz). This is accomplished by adding an offset to the A6 YO driver assembly when operating in band 0. This adjustment compensates for possible frequency changes in the A11 cavity oscillator, and provides improved frequency accuracy when operating at low frequencies (i.e. 10 MHz).

Table 8-9. A2J1 and A2P1 Pin-Outs

A2J1

A2J1 and A10J1 are pin-for-pin compatible, therefore, signal source and/or destination (TO/FROM**) points disregard the A10J1 connection.

PIN	SIGNAL	I/O	TO/FROM	FUNCTION
1 2	LFP5 +5V	IN IN	A3P1-30 A3P1-6,7	C 0
3 4	BD1 UNL LMP EN	I/O IN	A3P1-9 A6P1-16	ABC F
5 6	BD0 LFP4	I/O IN	A3P1-31 A3P1-26	ABC B
7 8	BD2 GND DIG	I/O	A3P1-32	ABC 0
9 10	BD3	I/O	A3P1-10 NOT USED	ABC
11 12	BA0 L UNLVL	IN IN	A3P1-33 A4P1-2	A F
13 14	BD5	I/O	A3P1-13 NOT USED	ABC
15 16	BD4	I/O	A3P1-35 NOT USED	ABC
17 18	BD7	I/O	A3P1-14 NOT USED	ABC
19 20	BD6	I/O	A3P1-36 NOT USED	ABC
21 22	LFP1	IN	A3P1-15 NOT USED	A
23 24	LFP2	IN	A3P1-37 NOT USED	A
25 26	LFP3	IN	A3P1-16 NOT USED	B
27 28	SCAN CLK	IN	A3P1-38 NOT USED	A
29 30	PWON	IN	A3P2-25 NOT USED	ABC
31 32	FLAG	OUT	A3P1-42 NOT USED	A
33 34	PIRPGB	OUT	NOT USED P2-61	
35 36	PIRPGA FREQ TRK V	OUT OUT	P2-60 A4P1-36, A5P1-24	E
37 38	FREQ CAL L RF ON	OUT OUT	A8P1-23 A10J4-6, A10J5-14	C
39 40	YTM DRIVE V −10V	IN IN	A7P1-23 P1-13	E 0
41 42	EXT CAL +20V	OUT IN	A4P1-24 P1-7	0
43 44			NOT USED NOT USED	
45 46	+10V	IN	NOT USED P1-8	0
47 48	GND ANLG		NOT USED	0
49 50	B VTUNE 1V/0.5V/GHz	IN OUT	A6P1-42 J4,A10J2-23	E G

Table 8-9b. A2J1 and A2P1 Pin-Outs

A2P1	A2P1 to A1J1 INTERCONNECT JACK				A1J1
PIN	**BLOCK**	**SIGNAL**	**TO/FROM**	**BLOCK**	**PIN**
1	D	Cb	→	K	1
2	D	Ca	→	K	2
3	D	DIG1	→	K	3
4	D	Cc	→	K	4
5	D	DIG2	→	K	5
6	A	COL2	→	J	6
7	D	DIG3	→	K	7
8	D	Cd	→	K	8
9	D	DIG4	→	K	9
10	A	COL1	→	J	10
11	A	COL0	→	J	11
12	A	COL3	→	J	12
13	D	Ce	→	K	13
14	D	Cdp	→	K	14
15	D	Cf	→	K	15
16	A	ROW2	←	J	16
17	D	Cg	→	K	17
18	A	ROW3	←	J	18
19	N	+5V	→	0	19
20	A	ROW0	←	J	20
21	N	GND DIG		F	21
22	A	ROW1	←	J	22
23		NOT USED			23
24		NOT USED			24
25	B	db/SWP	→	H	25
26		NOT USED			26
27		FREQ CAL	←	L	27
28		NOT USED			28
29	B	dBm	→	H	29
30		NOT USED			30
31	N	GND ANLG		0	31
32		NOT USED			32
33	B	dB/GHz	→	H	33
34		NOT USED			34
35	N	+10V	→	0	35
36	B	POWER SWP	→	H	36
37		EXT CAL	←	L	37
38	B	PWR SLOPE	→	H	38
39	N	−10V		0	39
40	B	CW FIL	→	H	40
41		PIRPGB	←	I	41
42	B	RF ON/OFF	→	H	42
43		PIRPGA	←	I	43
44		NOT USED			44
45		NOT USED			45
46	B	MTR ALC	→	H	46
47		NOT USED			47
48	B	EXT ALC	→	H	48
49	F	UNLEVELED	→	H	49
50	B	INT ALC	→	H	50

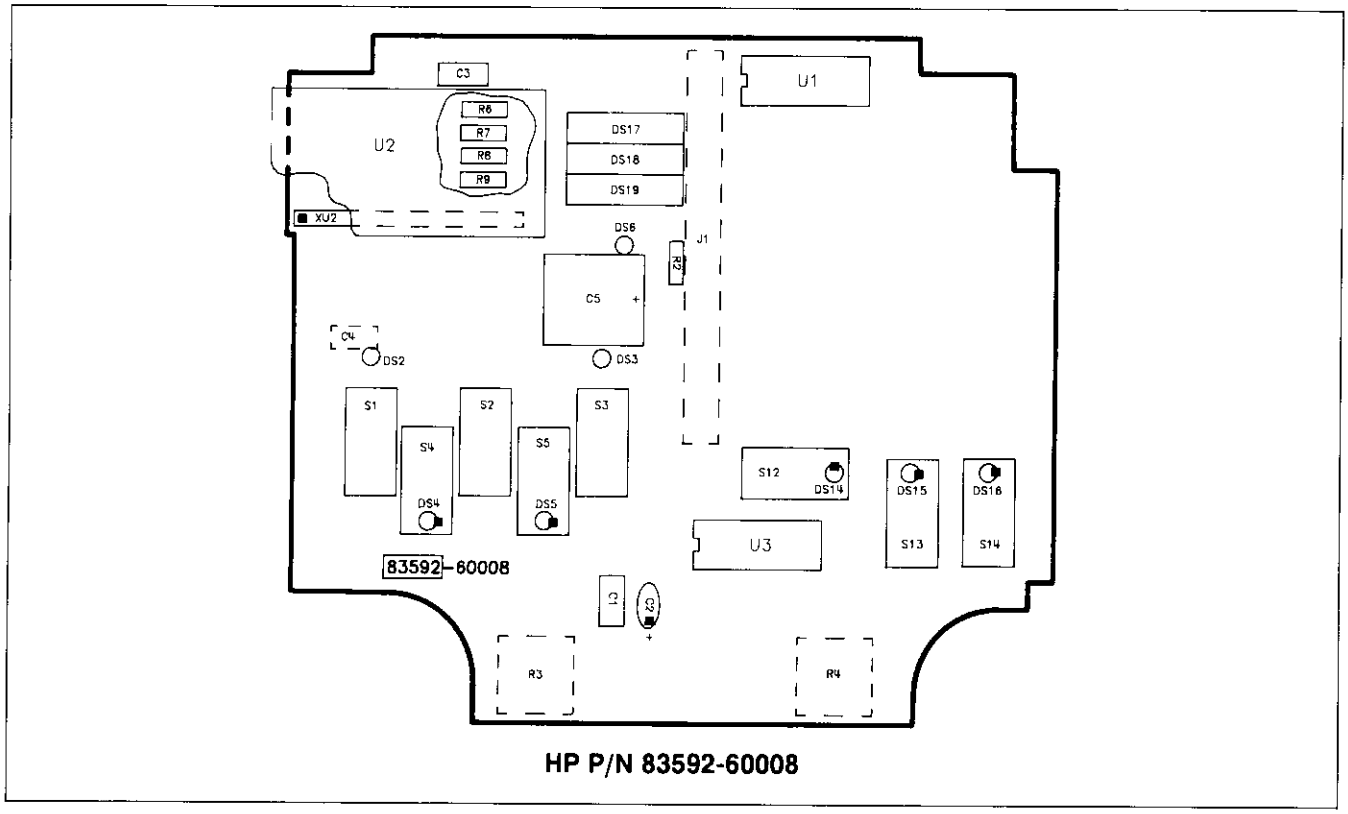


Figure 8-16. A1 Front Panel, Component Locations

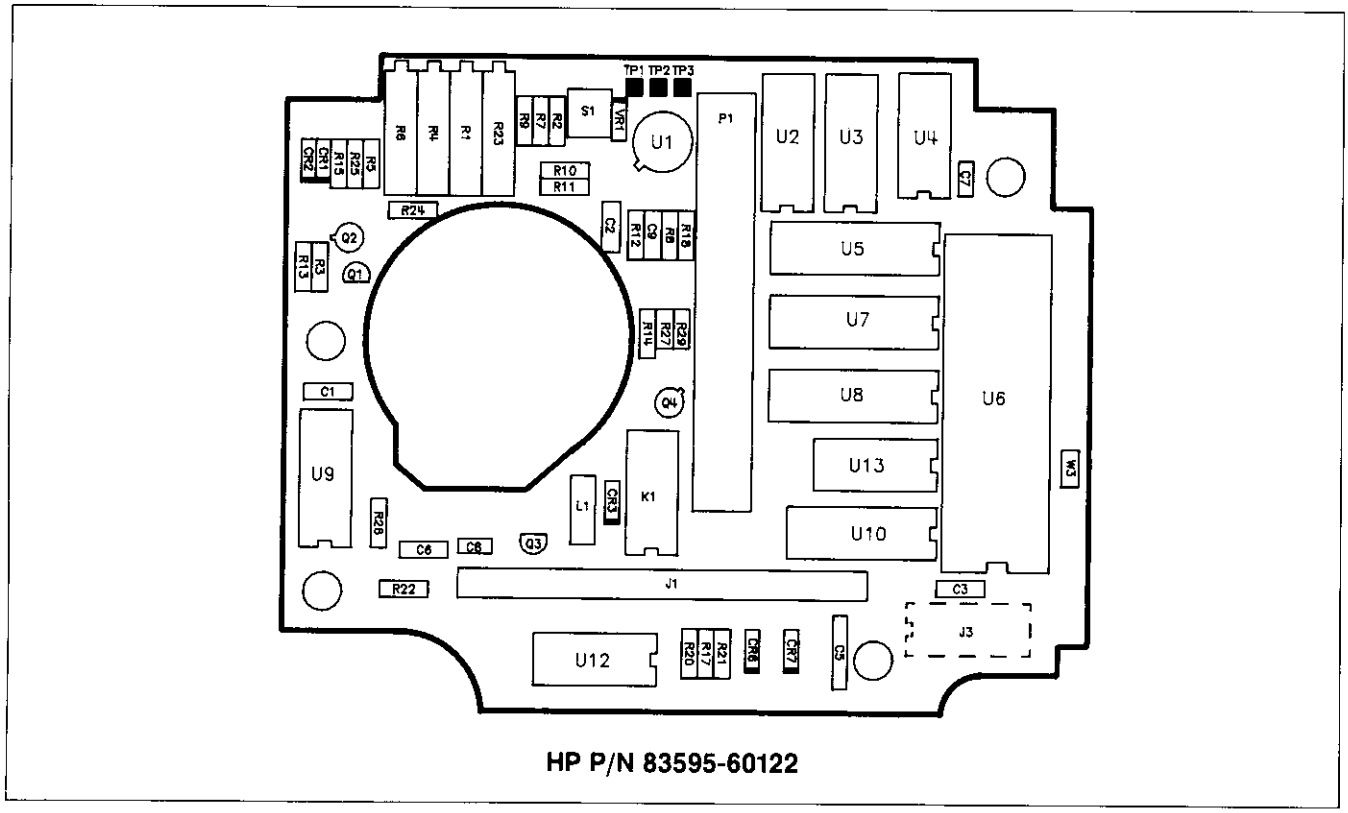


Figure 8-17. A2 Front Panel Interface, Component Locations

Troubleshooting the A3 Digital Interface Assembly

INTRODUCTION

The A3 digital interface assembly is the principle exchange for digital data, address, and timing signals used throughout the RF plug-in. The ROM on the A3 assembly contains software (firmware) and constants used for plug-in interrupt routines. Major enable lines used on the front panel and throughout the plug-in are decoded on this assembly. Note that some digital control lines (e.g. the Stop-Sweep Request (LSSRQ) and RPG lines) do not pass through the digital interface assembly.

A failure in the A3 digital interface typically disables the entire RF plug-in, and causes large errors in frequency, amplitude, and control. The front panel displays will probably be inoperative, and front panel controls will not produce any effect.

The HP 8350 sweep oscillator may or may not be disabled by a plug-in failure. A simple test to determine whether the HP 8350 is at fault is to remove the plug-in and press **[INSTR PRESET]** on the HP 8350. If **E001** is displayed, the HP 8350 is probably good. A different error code, especially **E005**, indicates problems in the HP 8350.

GENERAL TROUBLESHOOTING

Visually inspect the plug-in for damage, frayed cables, and loose connectors. Check ribbon cable W29 between the plug-in interface and A3 assembly. Check the ribbon cable in the HP 8350 leading from its motherboard to the plug-in interface.

Check the +5 VB line at A3J1 pins 35, 36, or 38, to make sure power is being supplied to the plug-in. The A3 assembly supplies +5V to the rest of the plug-in; check A3P1 pins 6 or 7 for +5 VDC.

Check configuration switch A3S1 and make sure that it corresponds to the model, options, and user-configurations as shown in Table 8-10.

The A3 digital interface assembly is made accessible for service with the following procedure:

1. Remove the RF plug-in from the HP 8350.
2. Disconnect W29P1 from A3J1, and remove the A3 assembly from the plug-in.
3. Replace the plug-in in the HP 8350.
4. Remove the top cover of the HP 8350.
5. Insert a 44-pin extender assembly into A10XA3.
6. Install the A3 assembly on the extender assembly, and reconnect W29P1.

Table 8-10. Configuration Switch on the A3 Digital Interface Assembly

Description	Switch Number							
	1	2	3	4	5	6	7	8
Plug-in: HP 83595A	x	x	x	x	x	x	x	x
Normal Sweep	0	x	x	x	x	x	x	x
Sequential Sweep Only	1	x	x	x	x	x	x	x
*No RF Power at Power-Up	x	x	x	1	x	x	x	x
Maximum RF Power at Power-Up	x	x	x	0	x	x	x	x
−6 MHz/V FM Sensitivity	x	x	x	x	1	x	x	x
−20 MHz/V FM Sensitivity	x	x	x	x	0	x	x	x
Direct-Coupled FM Modulation (−20 MHz/V)	x	x	x	x	x	1	x	x
Cross-Over Coupled FM Modulation	x	x	x	x	x	0	x	x
Step Attenuator Option	x	x	x	x	x	x	1	x
No Step Attenuator Option	x	x	x	x	x	x	0	x
AUX OUT Phase Lock	x	x	x	x	x	x	x	1
RF OUTPUT Phase Lock	x	x	x	x	x	x	x	0

NOTE

1 = Switch Open = High
0 = Switch Closed = Low (Ground)
x = Don't Care

*With the configuration switch set for an Instrument Preset condition of "RF Power OFF", bias is removed from A13 YIG oscillator. In addition, the HP 8350 microprocessor issues a blanking pulse to the plug-in. L RFB (Low = RF blank) biases the modulator on hard, closing off the RF signal path. When RF power is manually turned on, via the front panel pushbutton, L RFB remains low for a short period to allow the RF microcircuit components to reach full capacity before releasing the ALC amplifier. This prevents the ALC loop from correcting for a large error voltage at initial power up, thus preventing overshoot.

RF PLUG-IN SELF TEST

Major portions of the A3 digital interface assembly and the instrument bus connecting it to the HP 8350 are tested by the self test routine performed at INSTRUMENT PRESET or power-on.

The plug-in ROM is tested by reading a test pattern out of ROM, then performing a "checksum" on the entire range of ROM. If the test passes, this ensures that the data bus, address bus, and major timing lines to the A3 assembly, as well as the ROM address decoding and ROM itself, are good. If the test fails, error code **E001** appears, indicating a fault in these components or the instrument bus.

Other error codes (between **E050** to **E099**) indicate specific problems in the plug-in. These can occur either at INSTRUMENT PRESET or power-on, or during normal operation, and are discussed in greater detail below.

The L IRD, FLAG, and PIIRQ lines are not tested by the routine, nor are the internal data (BD0 − BD7) and address (BA0 − BA3) busses.

An error code indicates a failure in specific components. If the self test passes, these components are very probably working correctly. Hence, the troubleshooting information below is broken into three sections:

Error Code E001 "Plug-in Failure"

Other Error Codes

No Error Code Displayed

Refer to the appropriate section indicated by the self test results.

ERROR CODE E001

Error code **E001** indicates a failure in one or more of the following areas:

Connections between HP 8350/plug-in interface and instrument bus

HP 8350/plug-in interface

Connections between HP 8350/plug-in interface and A3 assembly

Plug-in buffers

ROM Address Decoding

ROM

The instrument bus internal to the HP 8350 is checked during self test and will produce error **E005** on failure. However, branches from the instrument bus leading to the plug-in are not tested.

In the HP 8350, check cables beween the motherboard and the HP 8350 chassis connectors J2 and J3 leading to the plug-in for damage or loose connections. Likewise, in the RF plug-in, check the cabling between chassis P1 and P2 and the A10 motherboard or A3 digital interface. Next, check the individual pins and sockets of the HP 8350/plug-in interface connectors for bent or missing pins. Make sure that the A3 assembly is firmly seated into its motherboard socket, and that ribbon cable connections are making good contact.

Perform the hex data read:

Press **[SHIFT] [0] [0]**	hex data mode
[4] [0] [0] [0]	address location 4000
[M3]	hex data read

The HP 8350 FREQUENCY/TIME display should indicate 55; increment the address to 4001 by pressing [▲], the FREQUENCY/TIME display should indicate AA. If these numbers are read, the data lines and the 4000H ROM enable line are functional.

If these tests do not execute, run the hex data rotate write:

Press **[SHIFT] [0] [0]**	hex data mode
[4] [0] [0] [0]	address location 4000
[M4]	hex data rotation write

Check the 4000H line to U1 for activity, and troubleshoot the address decoding circuitry if there is none. Repeat the above key sequence substituting address location **[5] [0] [0] [0]**. Check the 5000H line to U2 for activity.

The address lines can be checked by using the hex data write feature of the HP 8350. Alternate ones and zeros are written on the address lines when writing to address location 5555H or 2AAAH. By performing a hex data write to each address location, all thirteen address lines are pulsed high and low.

On the HP 8350:

Press **[SHIFT] [0] [0]**	hex data mode
[5] [5] [5] [5]	address location 5555
[M4]	hex data rotation write

Check that all even address lines (A0, A2,...A12) are pulsed high, and all odd address lines (A1, A3,...A11) are low.

On the HP 8350:

Press **[SHIFT] [0] [0]**	hex data mode
[2] [.] [.] [.]	address location 2AAA
[M4]	hex data rotation write

Check that all odd address lines are pulsed high and all even address lines are low.

OTHER ERROR CODES

Error codes **E052** and **E053** indicate a failure on the A3 digital interface assembly. These codes, along with troubleshooting hints related to that error, are listed below.

Error Code E052

Error code **E052** indicates a failure in triple programmable timer U5 or the 200 kHz clock. First check the 200 kHz clock. The SCAN CLK line is accessible at U3 pin 3, at the top of the A3 assembly, so it is not necessary to remove the A3 assembly to test it. The output frequency should be approximately 200 kHz. The pulse train is NOT symmetrical, and has TTL levels. If no clock signal is found, suspect U3.

If the SCAN CLK is present, yet **E052** occurs, then the failure is probably with U5. Press **[SHIFT] [5] [5]**, and check the LWR and LRD lines for the waveforms shown in Figure 8-19. If either control line is inactive, troubleshoot the address decoder U9. If the control lines are working, check the CTR 0 and CTR 1 waveforms as shown in Figure 8-19. If they are incorrect, replace U5.

Error Code E053

E053 generally indicates a failure in the PIA, U4. However, the problem might be in the output stages of U5. Enter **[SHIFT] [5] [5]**, and check CTR 0 and CTR 1 waveforms as shown in Figure 8-19. If they are correct, U5 is functional. Next, check the L PIAE line as shown in Figure 8-19, and make sure the L WRITE line shows activity. If not, troubleshoot the appropriate address decoding circuitry or buffer. Then, check L PIIRQ for the squarewave shown in Figure 8-19. If it is inactive, replace U4.

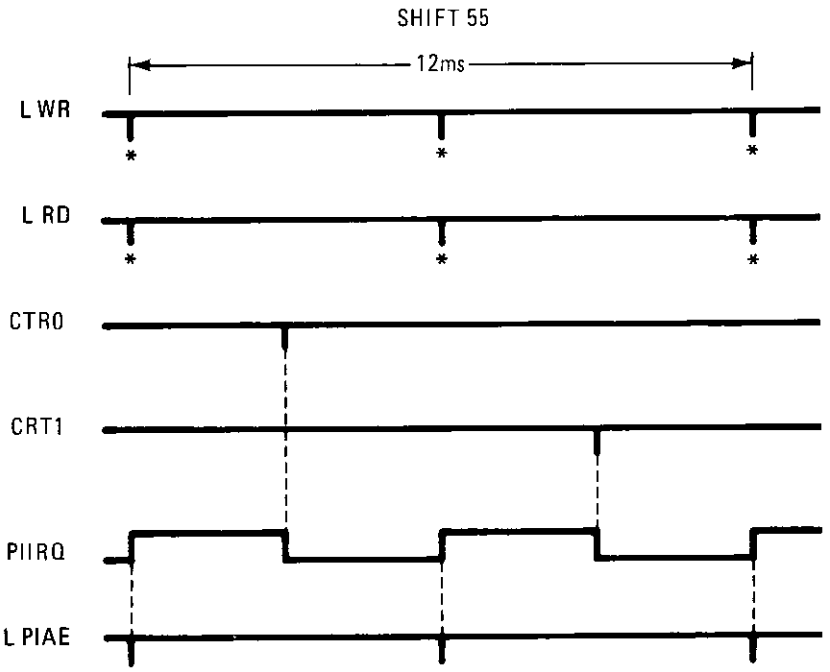


Figure 8-19. Interval Timer Self Test Timing Diagram

NO ERROR CODE

If no error code occurs and the HP 8350 displays show the correct start and stop frequencies of the plug-in, the plug-in self test passed successfully. This verifies the instrument bus to the plug-in, data and address busses on the A3 digital interface assembly, and plug-in ROM. Any plug-in failures which are traced back to the A3 assembly are due to failures in one or more of the following areas:

Address Decoding

Plug-in Buffers

Interrupt Control/Configuration Switch

Miscellaneous Control Lines

If problems occur only when performing a multiband sweep, suspect the programmable timer, U5. If the HP 8350 displays show the wrong frequencies, first check configuration switch S1 against Table 8-11, and then troubleshoot the PIA, U4.

ADDRESS DECODER

The primary address decoding for the plug-in occurs on the A3 assembly. The enable lines are then passed on to the rest of the instrument. The major address decoder test can be utilized to check all these lines.

Press **[SHIFT] [5] [3]**

Then check the outputs of U6B, U6C, U7B, U9, and U13 for the signals shown in Figure 8-20. The address lines have been verified by the self test. Therefore, if the L PIAE or ROM enable lines are faulty, troubleshoot the discrete address decoding logic involving U6, U7, U8, and U10, and replace the defective component. If other pulses are missing or displaced, replace the appropriate decoder, U9 or U13.

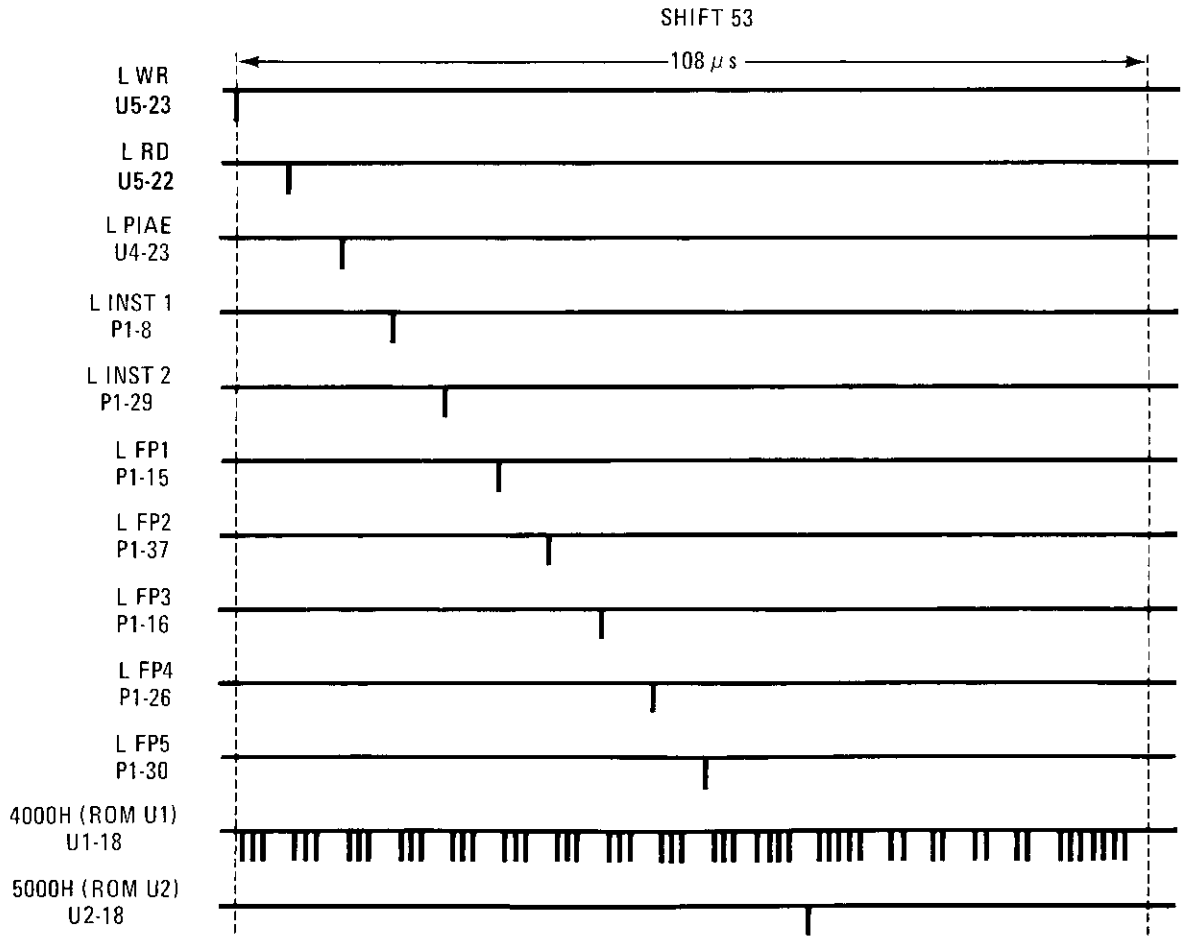


Figure 8-20. Major Address Decoder Timing Diagram

PLUG-IN INTERFACE

U14 and U17 buffer the address and data lines for use throughout the plug-in. The address and data busses on the A3 assembly have been verified by the INSTRUMENT PRESET self test. Therefore, if address or data is not being passed to another assembly, the fault lies with U14, U17, U6A, or a motherboard connection.

The address lines can be exercised by performing the minor address decoder test. On the HP 8350:

Press **[SHIFT] [5] [4]**	minor address decoder test

Verify activity on each of the buffered address lines (BA0 through BA3).

Data lines can be verified by performing a hex data rotation write to any address location between 2C00H and 2FFFH.

Press **[CW]**	
[SHIFT] [0] [0]	hex data mode
[2] [GHz] [0] [0]	address location 2C00
[M4]	hex data rotation write

Check for activity on each of the buffered data lines (BD0 through BD7), and check for shorts between lines.

INTERRUPT TIMER/PIA

The PIA is responsible for two functions:

Reading the configuration switch

Routing the interrupts from the triple timer

NOTE: Before changing the configuration switch settings, write down the switch positions and and return the switches to their original settings after troubleshooting.

The PIA's read capability can be checked.

Press **[CW]**	
[SHIFT] [0] [0]	hex data mode
[2] [9] [0] [0]	address location 2900
[M3]	hex data read

Watch the display change as the configuration switch is toggled.

The triple timer and PIA's interrupt masking capability are tested using a special routine at **[INSTR PRESET]** or power-on. Error codes **E052** or **E053** are displayed if a failure is detected. If these error codes are found, or if either U4 or U5 are suspect for other reasons, a special test pattern can be accessed.

Press **[SHIFT] [5] [5]**	interrupt control test

The waveforms shown in Figure 8-19 should be observed. Refer to paragraph, Other Error Codes for details on these errors codes and the **[SHIFT] [5] [5]** operator-initiated self test.

A3 Digital Interface, Circuit Description

GENERAL

The A3 digital interface assembly receives digital address, data, and control signals from the HP 8350 sweep oscillator. These signals are processed and then routed to the rest of the RF plug-in. The ROM (read only memory) contains software dedicated to the RF plug-in. The interrupt control circuit provides timing signals (which are controlled by the HP 8350 A3 microprocessor) during band-switching and at the beginning and end of each sweep. The A3 digital interface also provides data and timing information for the A2 front panel interface and A1 front panel assemblies, as well as data, address and control signals for the rest of the RF plug-in.

SWEEP OSCILLATOR INTERFACE, BLOCK A

The digital data, address, and control signals from the HP 8350 sweep oscillator pass through the RF plug-in interconnect and ribbon cable to J1 on the A3 digital interface assembly. They are buffered and inverted by Schmitt trigger inverters before passing on to the rest of the RF plug-in. 100-ohm resistors in series with each line are included to reduce ringing on the instrument bus. U7A and U7D enable the bi-directional data buffer when either the plug-in ROM (LB PIROME) or the plug-in itself (LB I/OE2) is enabled. Blanking pulse L BP2 passes directly through A3 and is not buffered. It is used on the A2 front panel interface for blanking the UNLEVELED light during retrace. Lastly, U10F receives the FLAG from the A2 front panel interface and passes it back to the sweep oscillator.

ADDRESS DECODER, BLOCK B

The address decoder decodes the address and control lines to provide control signals throughout the RF plug-in. Table 8-11 shows the decoded address lines and where they are used in the RF plug-in.

Table 8-11. Digital Interface Address Decoding

Mnemonic	Address	Address Decoder Components	Components Addressed	Read or Write	Description
L WR	2800H to 287FH	U9	A3U5	Write	Write data to programmable interval timer.
L RD	2880H to 28FFH	U9	A3U5	Read	Read data from programmable interval timer.
L PIAE	2900H to 29FFH	U7B, U7C, U8A, U10D	A3U4	RD/WR	Enable peripheral interface adapter. (Also addressed 2B00H to 2BFF.)
L INST1	2C00H to 2C7FH	U10D, U13	A4, A5, A6	Write	Write control for A4 ALC, A5 FM driver, and A6 sweep control.
L INST2	2C80H to 2CFFH	U10D, U13	A7, A8	RD/WR	Write to A7 SYTM driver and A8 YO driver. Control and read offset and gain switches.
L FP1	2D00H to 2D7FH	U10D, U13	A2	Write	Write to front panel displays.
L FP2	2D80H to 2DFFH	U10D, U13	A2	Read	Read front panel keyboard.
L FP3	2E00H to 2E7FH	U10D, U13	A2	Write	Write to front panel annunciators.
L FP4	2E80H to 2EFFH	U10D, U13	A2	Write	Write to front panel annunciators.
L FP5	2F00H to 2F7FH	U10D, U13	A2	Write	Write to RF control latch.
L ROM1	4000H to 4FFFH	U6C, U10A, U10B	A3U1	Read	Enable ROM U1.
L ROM2	5000H to 5FFFH	U6B, U10B	A3U2	Read	Enable ROM U2.

ROM, BLOCK C

The RF plug-in's ROM consists of two 4k by 8-bit ROMs. This memory contains all software program dedicated to the individual RF plug-in for use by the microprocessor in the HP 8350. Addresses 4000H through 4FFFH are read from U1, while 5000H through 5FFFH are found in U2. Address line A12 is decoded in the address decoder and selects which ROM is enabled. The remaining twelve address lines (A0 through A11) determine the individual ROM address being read.

200 kHz CLOCK, BLOCK D

U3 is a simple oscillator with external timing elements configured to provide a stable 200 kHz pulse train. This signal is used to clock the interrupt control counters in U5 for interrupt timing. The 200 kHz clock is also used on the A2 front panel interface to scan the keyboard and refresh the display.

INTERRUPT CONTROL/CONFIGURATION SWITCH, BLOCK E

Triple programmable counter U5 contains three programmable down-counters and control circuitry. The counters are preloaded by the data bus, then down-counted by the 200 kHz clock. When the count reaches zero, a pulse is produced on the corresponding output. In this way, the microprocessor can command a time interval of any duration, and will receive an interrupt when the count-down is complete.

U4 is a PIA (peripheral interface adapter) which controls the interrupts from U5 and reads the configuration switch, S1. As an interrupt controller, U4 can be microprocessor-programmed to mask or enable any of four possible interrupts. These interrupts mark the end of important timing intervals used during band-switching.

Configuration switch S1 is encoded with information about the type of RF plug-in and the options included, as well as operator-chosen parameters such as FM sensitivity and power-up conditions. (See Table 8-11 for details.) The microprocessor addresses U4 to read the switch status at power-on or when INSTRUMENT PRESET is initiated, and uses the information in subsequent calculations involving frequency range, power range, marker values, and many other plug-in dependent parameters.

RF PLUG-IN INTERFACE, BLOCK F

U17 and U14 buffer the address and data signals required throughout the rest of the RF plug-in. U17 is a bi-directional, 8-bit data buffer, enabled when signals B I/OSTB, A10, and B I/OE2 are all high. Its direction is controlled by the L WRITE line. U14 is enabled by LB I/OE2 to pass four address lines (A0 through A3) to the rest of the RF plug-in's circuitry.

Table 8-12. A3P1 and A3J1 Pin-Outs

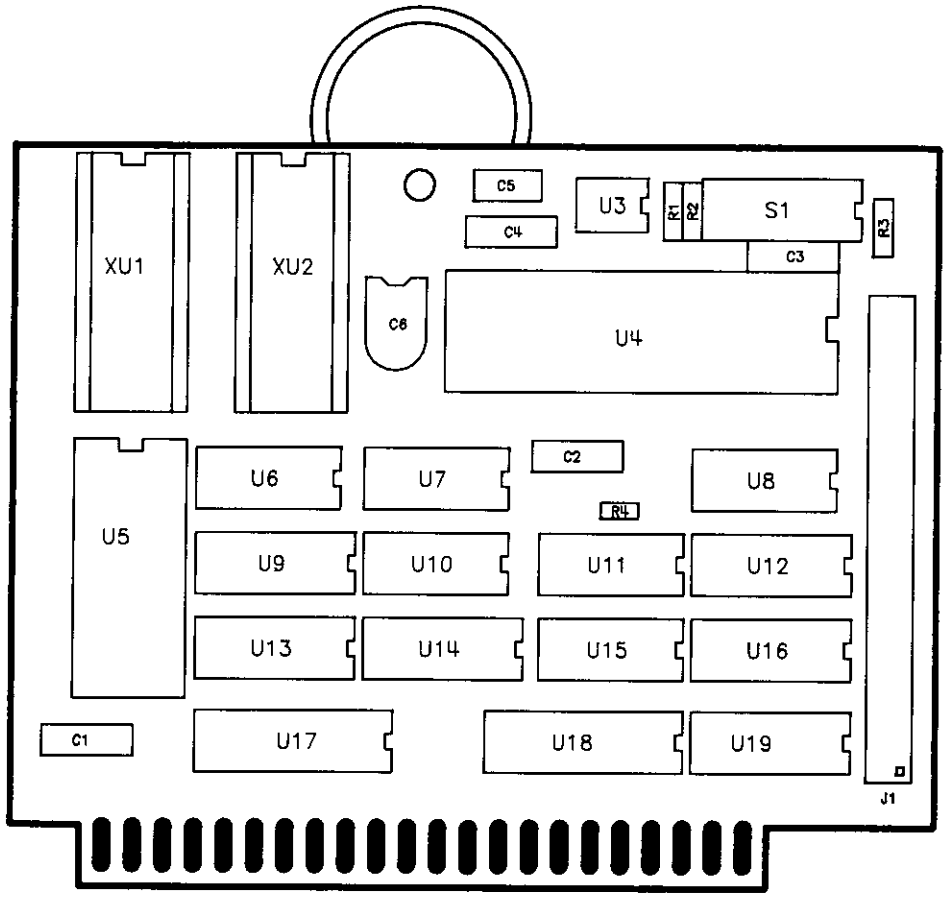
A3P1

PIN	SIGNAL	I/O	TO/FROM	FUNCTION
1 23			NOT USED NOT USED	
2 24			NOT USED NOT USED	
3 25			NOT USED NOT USED	
4 26	GND DIG L FP 4	OUT	A2J1-6	G B
5 27	GND DIG		NOT USED	G
5 27	GND DIG		NOT USED	G
6 28	+5V	OUT	NOT USED	G
7 29	+5V L INST2	OUT OUT	A7P1-18,A8P1-18	G B
8 30	L INST1 L FP5	OUT OUT	A4/A6P1-18,A5P1-5 A2J1-1	B B
9 31	BD1 BD0	I/O I/O		F F
10 32	BD3 BD2	I/O I/O		F F
11 33	BA1 BA0	OUT OUT		F F
12 34	BA3 BA2	OUT OUT		F F
13 35	BD5 BD4	I/O I/O		F F
14 36	BD7 BD6	I/O I/O		F F
15 37	L FP1 L FP2	OUT OUT	A2J1-21 A2J1-23	B B
16 38	L FP3 SCAN CLK	OUT OUT	A2J1-25 A2J1-27	B E
17 39			NOT USED NOT USED	
18 40	L SIRQ	IN	A6P1-3 NOT USED	E
19 41			NOT USED NOT USED	
20 42	FLAG	IN	NOT USED A2J1-31	A
21 43			NOT USED NOT USED	
22 44	PWON L BP2	IN OUT	P2-25 A6P1-15	E A

Table 8-12b. A3P1 and A3J1 Pin-Outs

A3J1

PIN	SIGNAL	I/O	TO/FROM	FUNCTION
1	GND DIG			G
2	ID0	I/O	P2-33	A
3	ID1	I/O	P2-2	A
4	ID2	I/O	P2-34	A
5	ID3	I/O	P2-3	A
6	ID4	I/O	P2-35	A
7	ID5	I/O	P2-4	A
8	ID6	I/O	P2-36	A
9	ID7	I/O	P2-5	A
10	GND DIG			G
11	GND DIG			G
12	L IA0	IN	P2-38	A
13	L IA1	IN	P2-37	A
14	L IA2	IN	P2-39	A
15	L IA3	IN	P2-8	A
16	L IA4	IN	P2-40	A
17	GND DIG			G
18	L IA5	IN	P2-41	A
19	L IA6	IN	P2-10	A
20	L IA7	IN	P2-42	A
21	L IA8	IN	P2-11	A
22	L IA9	IN	P2-43	A
23	L IA10	IN	P2-12	A
24	L IA11	IN	P2-44	A
25	L IA12	IN	P2-13	A
26	PIROME	IN	P2-45	A
27	GND DIG			G
28	GND DIG			G
29	L IRD	IN	P2-15	A
30	I/OE2	IN	P2-47	A
31	GND DIG			G
32	GND DIG			G
33	L I/OSTB	IN	P2-17	A
34	GND DIG			G
35	+5VB	IN	P2-18	G
36	+5VB	IN	P2-50	G
37			NOT USED	
38	+5VB	IN	P2-51	G
39	L PIFLG	OUT	P2-20	A
40	L PIIRQ	OUT	P2-52	E
41	GND DIG			G
42	L BP2	IN	P2-53	A
43			NOT USED	
44			NOT USED	



HP P/N 83525-60080

Figure 8-22. A3 Digital Interface Component Locations

Troubleshooting the A4 ALC Assembly

INTRODUCTION

Since the automatic level control (ALC) function of the RF plug-in includes many individual components arranged in a highly interdependent closed loop, the scope of the A4 ALC troubleshooting section extends well beyond the limits of the A4 assembly. Portions of the A5 FM driver assembly, and several microcircuit components which contribute to the power leveling function, are discussed below.

The ALC "loop" is a complex feedback loop which monitors the RF output power and continuously corrects for any deviation from the desired power level. Because it is a closed system, it is difficult to isolate cause from effect when a problem arises. The key to troubleshooting then, is to examine individual components, correlating the expected output for a particular input signal.

This troubleshooting outline is organized into two major sections: Troubleshooting Symptoms and Troubleshooting Procedures. The section titled, Troubleshooting Symptoms, characterizes possible failure modes, provides some general troubleshooting hints, and refers the reader to more detailed procedures found under the paragraphs titled, Troubleshooting Procedures.

NOTE: To ensure that Option 002 RF plug-ins remain in the same attenuator setting during troubleshooting, press **[SHIFT] [POWER SWEEP]**. This allows full ALC control without changing attenuator settings.

TROUBLESHOOTING SYMPTOMS

The procedures outlined below help to systematically characterize the failure as quickly as possible. The following failure symptoms are discussed:

RPG/Power Display Failure
Unleveled (LED)
Flatness/Oscillations (Power Drop-outs)
Full Unleveled Power
No Power (Single Band)
No Power (All Bands)
Power Sweep/Flatness

Evaluating the failure mode may require a power meter or a scalar network analyzer with a detector. (However, a crystal detector with an "A vs B" oscilloscope may often be substituted.) Figure 8-24 illustrates a typical test setup. Initiate all tests by pressing the **[INSTR PRESET]** key.

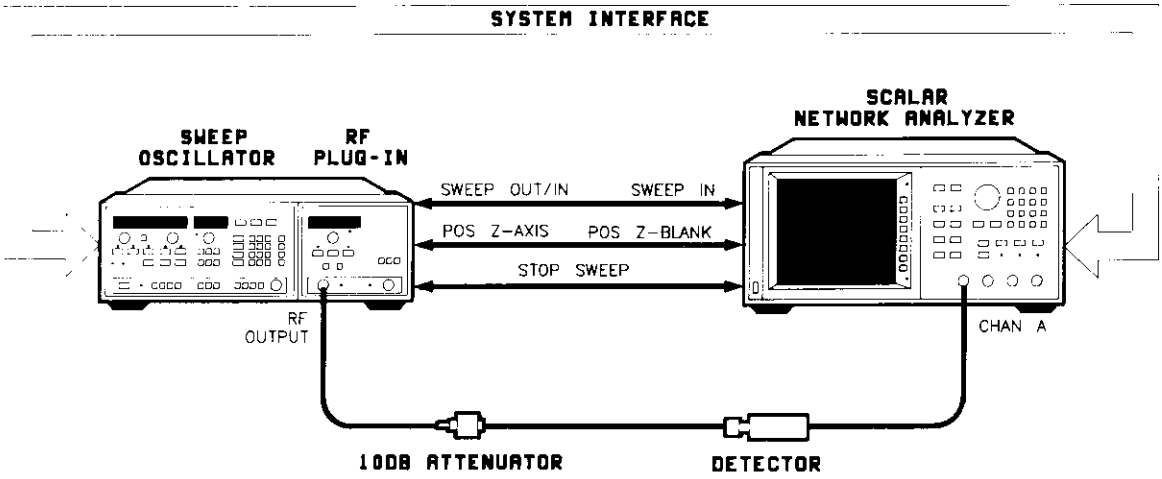


Figure 8-24. Typical ALC Troubleshooting Setup

RPG/Power Display Failure

Check that the POWER display changes when either the RPG is rotated or data is entered via the HP 8350 keyboard. This verifies that the digital information is reaching the mainframe, is properly processed, and is then displayed.

If the display is flashing rapidly or showing random patterns, refer to A1/A2 or A3 digital interface troubleshooting. If the RPG causes a change in the measured RF power level, but the POWER display remains the same, refer to A1/A2 troubleshooting. If the RPG produces no response whatsoever, or if the front panel display is blank, refer to A1/A2 troubleshooting, and trace the problem back to the HP 8350 mainframe.

Unleveled (LED)

If the UNLEVELED light turns on during the sweep, enter a sweep time of 20 seconds (i.e. one second per GHz). Observe the SWP light on the HP 8350 sweep oscillator, and determine at which times during the sweep the UNLEVELED light turns on.

If the UNLEVELED light remains lit during retrace, suspect problems in the front panel annunciator drivers. Refer to A1/A2 troubleshooting.

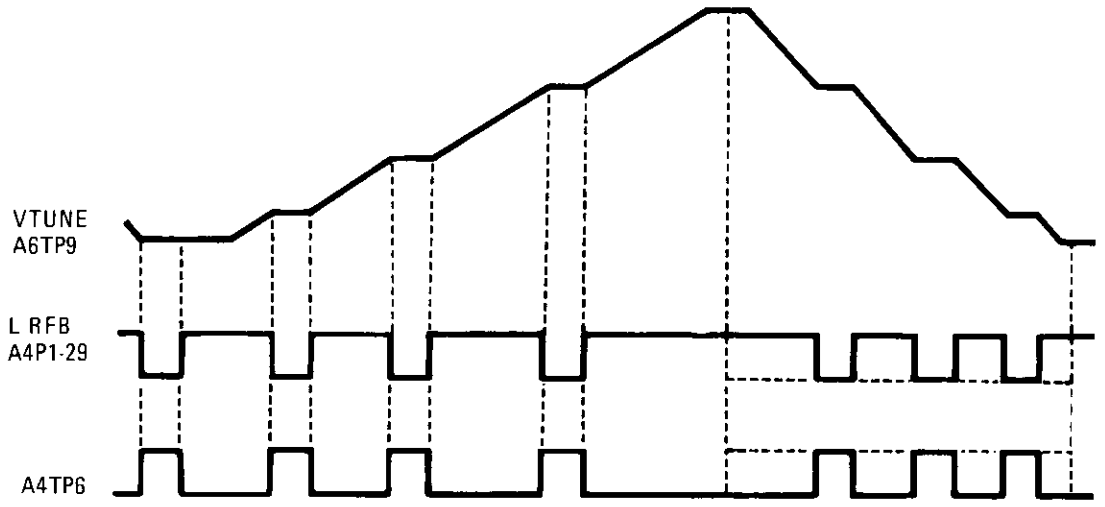
If the UNLEVELED light blinks briefly at the beginning of the sweep, the heterodyned band 0 may be sweeping through 0 Hz and causing an ALC drop-out. Check this by slowly increasing the start frequency. If the UNLEVELED light stops blinking, enter a CW frequency of 0 MHz and adjust the plug-in front panel FREQ CAL screw to the center of the adjustment range that keeps the UNLEVELED light on. Press **[INSTR PRESET]** and observe the UNLEVELED light. A frequency counter may be used to check frequency accuracy at 10 MHz or 50 MHz. If necessary, refer to Section 5, Adjustments, in this manual, and perform the frequency accuracy calibration procedure.

If the UNLEVELED light is on only during the first two seconds of the sweep (10 MHz to 2.4 GHz), the problem is in the band 0 loop. If it is lit after the first two seconds of the sweep but prior to retrace, the problem is band 1 through 4 related. In either case, the power level reference/summing circuits and those components common to all bands are probably NOT at fault. Check the appropriate detector, modulator, and detector selection switch.

If the UNLEVELED light is on during the entire forward sweep, suspect components common to all bands.

If the UNLEVELED light flashes briefly three times during the sweep (at 2, 7, 13.5, and 20 seconds into the trace), the problem occurs at the bandswitch points. Check for the RF blanking (L RFB) pulses during bandswitch at A4P1-29, as shown in Figure 8-25. If the signal is missing, trace the problem back through the HP 8350, to the blanking request (L RFBRQ) line on the RF plug-in A6 assembly. If L RFB is present, but A4TP5 does not clamp at greater than or equal to +4 VDC during blanking, suspect A4U2D or A4U9.

If the UNLEVELED light flashes briefly during the sweep, but does not imply any of the above failure modes, check power flatness. See below.



--- Shows ALC response to RF BLANK select (8350A front panel).

Figure 8-25. Bandswitch/Retrace Blanking Waveforms

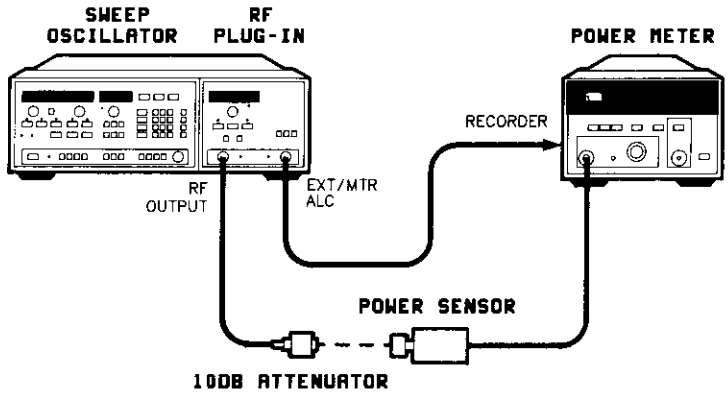


Figure 8-26. Power Meter Leveling Setup

Flatness/Oscillations (Power Drop-outs)

Monitor the RF output with a scalar network analyzer as shown in Figure 8-24. Optimize the output power with the front panel PEAK control.

If the power level is constant across the sweep and within approximately 5 dB of the programmed power level, then the plug-in may only require ALC flatness adjustments. Refer to Section 5, Adjustments, in this manual, for the ALC Internal Leveled Flatness adjustment procedure.

If the measured power level lies between +10 and −5 dBm, but can't be controlled via the front panel, refer to the Digital Control paragraph under Troubleshooting Procedures.

If the trace appears chopped or broken, the loop may be oscillating. Refer to Section 5, Adjustments, in this manual, and perform the ALC Gain adjustment procedure.

Full Unleveled Power (One or More Bands)

If power is unleveled in band 0 only or bands 1 through 3 only, select a sweep width within the unleveled band(s). If power is unleveled in all bands, continue to sweep the plug-in's full frequency range.

Attempt to level the power externally using a power meter as shown in Figure 8-26. Select **[MTR]** leveling, and enter a 100 second sweep time. If the RF power is now leveled then the failure is most likely in the detectors or the detector selection switch, A4U6. Refer to the following paragraph. If this does not prove to be the case, the problem may be in the two analog switches U4B and U6A. It may be necessary to perform the ALC adjustments in Section 5 of this manual.

Check the detector selection switch by entering a CW frequency within the band or leveling mode in question and trace the detector voltage through U6B. If the input to be selected doesn't match the output, check the MUX A0 and MUX A1 lines (see Table 8-13). Also check U12 and U13 as described under digital control.

Check the voltage at TP5. If it is greater than or equal to +5 VDC, suspect the mod drivers or modulators. If it is below −2 VDC, suspect the detectors and the feedback path components functional blocks E, F, and G.

Table 8-13. Leveling Control Lines

DATA BUS					Leveling Mode
Mux A0	Mux A1	Mux A0B	Mux A1B	PM	
H	H	H	H	L	INT 0
L	H	L	H	L	INT 1
H	L	H	L	L	EXT
L	L	H	H	H	PM 0
L	L	L	H	H	PM 1

No Power (Single Band Only)

If no power is detected in one band, but there is leveled power in another band, suspect the components of the RF path appropriate to the faulty band within the ALC loop.

NOTE: Turn off line switch before removing or installing any assembly.

NOTE: With the ALC assembly removed from the plug-in, 27.8 kHz square wave modulation from the HP 8350 is not available. However, the scalar network analyzer 27.8 kHz square wave can be connected to the rear panel PULSE IN connector to maintain scalar network analyzer compatibility.

To check the RF components, remove the A4 ALC assembly from its socket. This removes all bias from the modulators, and should allow maximum power through the RF path in all bands. If full power (over +12 dBm) is then detected in all bands, the RF amplifiers (A14 and A17), the cavity oscillator (A11), the DC return (A15), the isolator (AT1), and SYTM (A12) are verified. Suspect primarily the appropriate detector. Also inspect the appropriate modulator, as well as the A4 mod drivers and detector selection switch.

If the RF signal for bands 1 through 4 is missing, check the A6 SRD and PIN diode bias circuit. If the PIN diode switch bias signal is not getting through, or the B0 control line is missing, the switched YTM will come up in the band 0 position.

No Power (All Bands)

NOTE: Turn off line power before removing or installing any assembly.

If no power is detected in any band, remove the A4 ALC assembly. This removes all bias from the modulators, and should allow full RF power to be transmitted. If there is still no power, check the rear panel AUX OUTPUT for approximately 0 dBm to verify that the A13 YIG oscillator is providing an RF output. Refer to RF section troubleshooting for details.

If removing the A4 assembly causes full unleveled RF power to appear, reinstall the assembly and check A4TP5. If less than −2 VDC is present, verify that the voltage across R49 (Block L) is zero. If A4TP5 is greater than +5 VDC, suspect any circuitry between the detector selection switch and A4TP5, particularly the log amp.

Power Sweep/Flatness

If power increases smoothly with frequency, and POWER SWEEP is NOT selected, suspect problems with the A5 FM driver assembly.

NOTE: Turn off line power before removing or installing any assembly.

Remove the A5 assembly from the plug-in. If the situation improves, suspect a failure on the A5 assembly.

If the RF power is leveled within approximately 5 dB of the programmed power level, refer to Section 5, Adjustments, in this manual, and perform the ALC Internal Leveled Flatness adjustment procedure.

TROUBLESHOOTING PROCEDURES

The troubleshooting information below is organized into functional areas:

Digital Control, Block A
Power Level Reference/Summing, Blocks C and H
Detectors/Detector Selection Switch, Block B, DC1, and CR1
Feedback Path, Blocks E, F, G, and J
Error Sample and Hold and Main ALC Amp, Blocks I and L
Mod Drivers, Blocks N and O
Modulators, A17, and A13
Sample and Hold, Blocks E and K

Before continuing with the functional area troubleshooting information characterize the failure as much as possible. Some important information to know about the failure is:

Is the failure frequency mode related? (CW or swept mode)

Is the failure frequency band related? (band 0 only, bands 1 through 4 only, or common to all bands)

Does the failure affect RF output power? (maximum unleveled power, low power, or adjustable power not within specifications)

Is the unleveled light on?

Is the failure control related?

If after characterizing the failure, you suspect the A4 assembly to be at fault but still cannot determine the functional area, follow the open loop procedure detailed in Figure 8-28.

The open loop procedure allows the feedback path to be disconnected from the main signal path. By applying a known input to the ALC circuits, waveform measurements can be made at critical test-points isolating the three main functional areas of the A4 assembly: the power level reference, feedback path and main ALC amplifier.

Digital Control, Block A

Address decoder U12 and latch U13 control digital switches throughout the A4 assembly. Their operation can be confirmed by performing the hex data rotation write at address 2C07 hex.

Press **[SHIFT] [0] [0]** hex data mode
[2] [GHz] [0] [7] address location 2C07 (U13)
[M4] hex data rotation write

Check the outputs of U13 for the waveforms shown in Figure 8-2.

If any output signal is missing or misplaced, check the data lines against Figure 8-2. If no output is found, look for activity at U13 pin 11. Check for L INST1 and BA3 to pulse low, while BA0, BA1, and BA2 pulse high. If these pulses are missing, trace the problem back to A3 digital interface.

If the digital control section is working, the primary outputs of U13 are easily controlled by selecting the appropriate front panel function while in the CW sweep mode. (e.g., B1 is held high by selecting a CW frequency in bands 1 through 4; selecting **[MTR]** leveling holds the PM line high, etc.).

Power Level Reference/Summing, Blocks C and H

The power level reference and power level summing circuits produce a voltage proportional to the programmed power level. This signal is a summation of the absolute power reference, AM, detector compensation, and power sweep signals.

The detector compensation and power sweep signals are generated on the A5 FM driver assembly. If an A5 failure is suspected, refer to troubleshooting information in the A5 service information section. Unless A5 is suspect, simplify A4 troubleshooting by turning off the line power and removing the A5 assembly. Although power sweep will be disabled and the power flatness will be lost, the ALC loop should still level without the signals provided by the A5 assembly.

DAC U11 establishes the absolute power level. The −10V REF from the A6 assembly is scaled to yield from 0 VDC (−5 dBm displayed) to +10 VDC (+20 dBm displayed) at TP2. (This breaks down to a voltage step of 0.40 VDC per 1.0 dB of power over the dynamic range, or +6.00 VDC at +10 dBm.)

A self-test routine is available to exercise the ALC DAC.

Press **[SHIFT] [5] [0]**

The waveform in Figure 8-27 should be seen at TP2. Note that the exercise routine for the 12-bit DAC yields a staircased waveform with 13 levels. The first step shows the maximum +10 VDC output with all bits high. The following levels represent the voltage at TP2 with successive bits loaded high in order from the most significant bit to the least significant bit.

If the waveform at TP2 is not correct, check for −10V REF, and trace any problem back to the A8 assembly. Look for activity on L INSTR 1, BA0, and BA1. BA2 and BA3 should pulse high as each new DAC value is loaded, pulsing the CS line (U14 pin 8) low. If any of these lines, or a data line, appears dead, trace the problem back to the A3 assembly.

U2A adds PWR SWP/COMP and AM, and provides detector flatness compensation at higher power levels with CR2 and CR1. Use the EXT MTR mode to bypass these diodes while troubleshooting.

U2C adds the front panel amplitude adjustment (EXT CAL) used with external leveling. The following levels should be seen at TP1 with A5 removed and **[INT]** leveling selected: +0.3 VDC for −5 dBm, and +7.0 VDC for +20 dBm. An amplitude modulation (AM) signal of 1.0 Vp-p at the HP 8350 AM INPUT will produce roughly 260 mVp-p at TP1. (Note that U3A, CR2, and CR1 in the feedback path around U2A change the gain depending on the band and desired power level. This may result in a 1.0 VDC difference between bands at +20 dBm.)

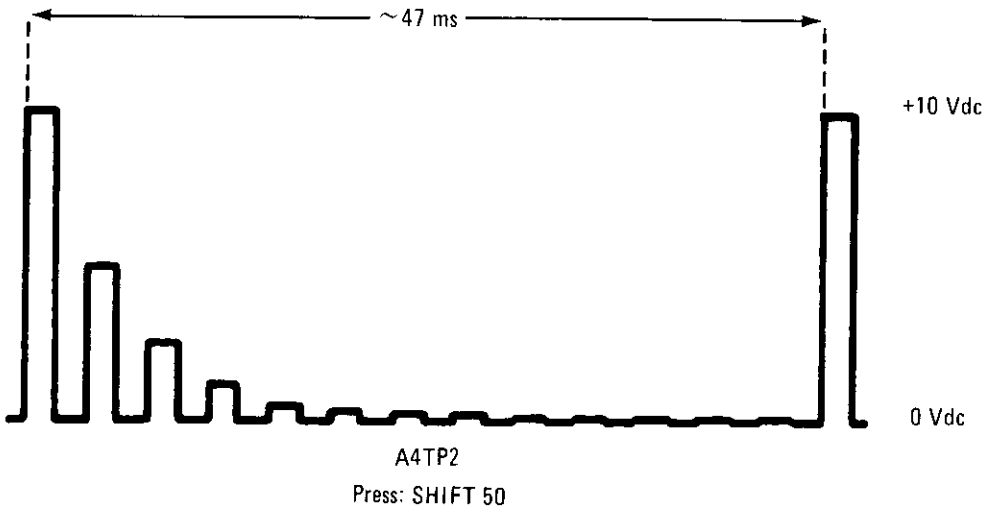


Figure 8-27. ALC DAC Test Waveform

Detectors/Detector Selection Switch, Block B, DC1, and CR1

The DC1 (band 0) and CR1 (bands 1 through 3) detectors are tested simply by checking their output voltages under full leveled power or full unleveled power conditions. The A4 assembly must be installed for troubleshooting in band 0 as it supplies bias current to the band 0 detector.

NOTE: The 27.8 kHz modulation signal required for scalar network analyzer compatibility is not available from the HP 8350 when the A4 assembly is removed from the plug-in and must be supplied from the scalar network analyzer through the rear panel PULSE IN connector.

If no power is measured in the suspected band, turn off the line power and remove the A4 assembly. Return power to the instrument. (If there is still no RF power, suspect components of the RF path. Refer to RF section troubleshooting.) If full unleveled RF power is obtained, apply two narrow strips of cellophane tape to the pin-edge connector to isolate the outputs of the modulator drivers from the modulators (P1-19 and P1-44). Reinstall the A4 assembly. This removes bias from the modulators, allowing full RF power transmission, while providing detector bias.

If full leveled power (+10 dBm from 0.01 to 18.6 GHz and +4 dBm from 18.6 to 26.5 GHz) or full unleveled power (at least 2 dB higher than leveled) is measured, sweep only the band in question and check the voltages at the detector inputs against the values shown in Table 8-14. (Use high-impedance 10:1 probes.)

Table 8-14. Detector Voltages

	Full Leveled +10 dBm	**Full Unleveled +20 dBm**
Band 0 (A4P1-21)	−150 to −299 mV	−300 to −400 mV
Bands 1 through 4 (A4P1-21)	−100 to −120 mV	−200 to −600 mV

If the detectors are working and the detector selection switch is suspected, sweep only in the faulty band and monitor TP12 for the voltages seen at the selected input of U6B.

If the EXT/MTR ALC INPUT circuits are suspected, select the EXT leveling mode and supply a test signal (low-level DC or sine wave) to the front panel BNC connector, and trace it through U6B at A4TP12.

NOTE: Remove any tape applied to edge connector pins in the previous procedure.

Feedback Path, Blocks E, F, G, and J

The feedback path of the ALC loop is composed of the components in functional blocks E, F, G, and J.

Before troubleshooting the feedback path be sure the detectors and detector selection switch are working correctly. See above.

The feedback path can be effectively tested by using the "open loop" method of troubleshooting. This procedure utilizes the external leveling mode **[EXT]** by supplying a sine wave to the EXT/MTR ALC INPUT connector. This method breaks the ALC loop and allows waveforms to be checked against known test signals. See Figure 8-28 for more details.

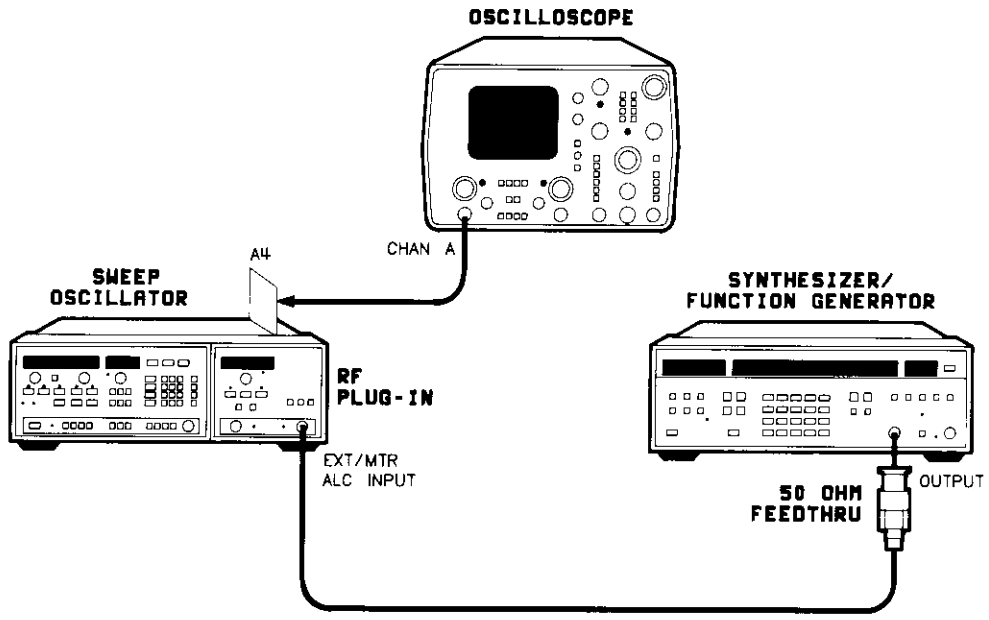
The open loop procedure will find the majority of the problems in the feedback path. A problem that will not normally be found using this method is, small voltage offsets caused by leakage through the MOS-FETS Q7, Q8, or Q16. The failure symptoms are as follows:

The instrument appears to be functioning correctly at high power levels but as programmed power is decreased the actual power output decreases in larger increments until the power output falls off completely.

Suspect MOS-FETS Q7, Q8, and Q16 as the failed components. Verify the failed component(s) by doing the following.

Press **[INT]**. Measure from P1-42 (INT DET RET) to the source of Q7 and Q16 (the pin designated as ground). If a small voltage is measured (greater than 1 mV) replace the defective MOS-FET.

Press **[EXT]**. Measure from P1-1 (EXT DET RET) to the source of Q8 (the pin designated as ground). If a small voltage is measured (greater than 1 mV) replace Q8.



EQUIPMENT

Function Generator/Synthesizer	HP 3325A
Oscilloscope	HP 1740A
50 Ohm Feedthru Termination	HP 10100C

PROCEDURE

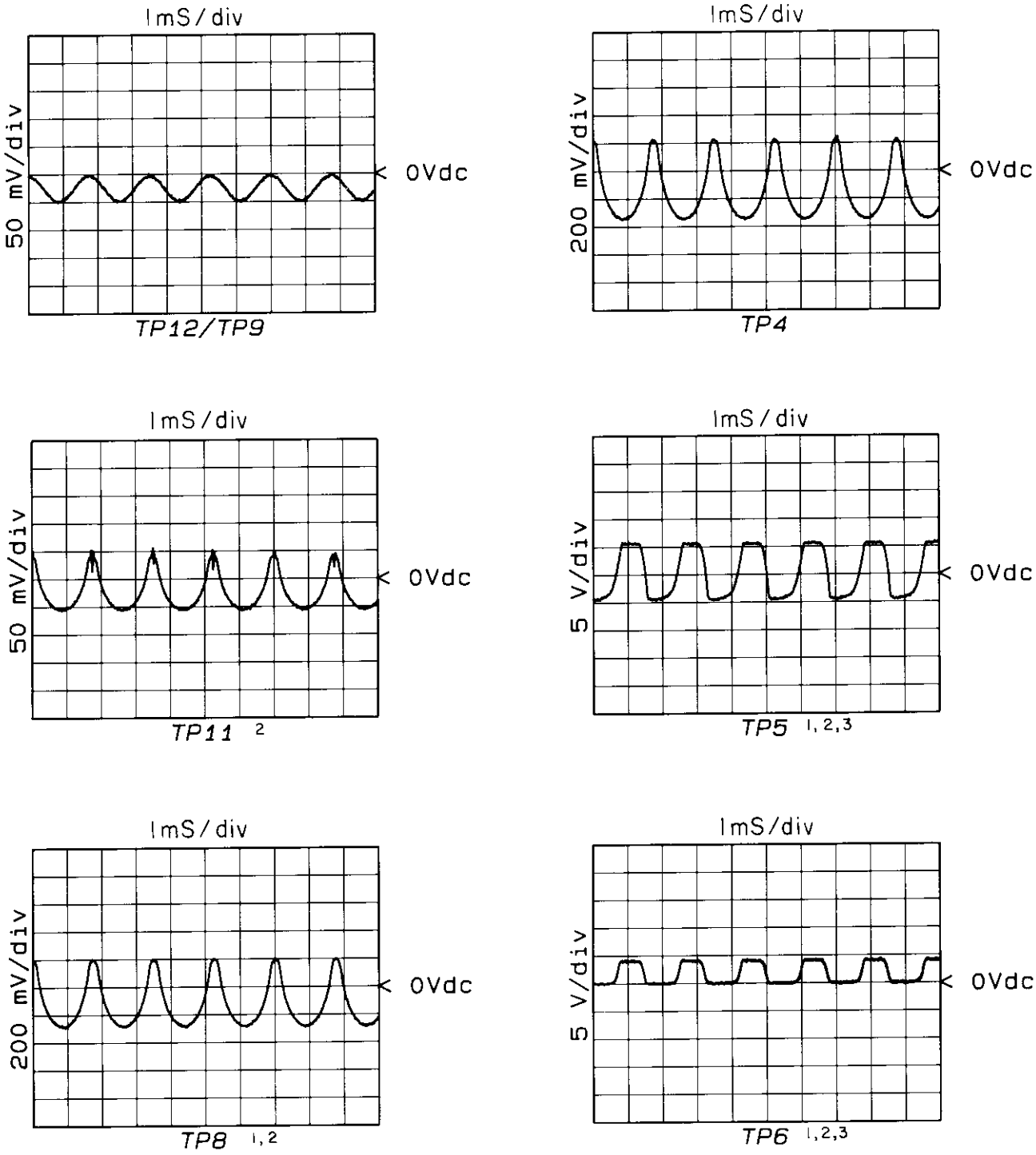
1. Turn the instrument off. Remove the A4 ALC assembly from its socket.
2. Locate and lift jumper J2. Reinstall the A4 assembly.
3. Turn the instrument on and press **[INSTR PRESET]**.
4. Press **[EXT]** ALC.
5. Adjust the function generator/synthesizer output for a 50 mV p-p sine wave at 500 Hz. Set the DC OFFSET for −25 mV.
6. Connect the function generator/synthesizer output to the EXT/MTR ALC connector.
7. Set the oscilloscope to DISPLAY and TRIGGER on channel A. Adjust the function generator/synthesizer DC OFFSET to ensure that the waveform at TP12 does not go positive. Check for the waveforms shown in Figure 8-29.

NOTE: The function generator/synthesizer DC OFFSET may have to be adjusted slightly to produce the waveforms given in Figure 8-29. If the EXT/MTR ALC input goes positive, the log amplifier will saturate.

Adjustment of the EXT/MTR ALC CAL screw will affect the waveforms at TP5, and TP8. Adjust the CAL screw until these waveforms are obtained.

Slight differences may be noted between the waveforms shown in Figure 8-29 and those obtained on individual ALC assemblies. This is due to the many adjustments on the A4 assembly. Insure that R81 (OFS 1), R82 (OFS 2) and R78 (OFS 3) are set for 0V as outlined in steps 1 through 3 of adjustment procedure 5-12. ALC Adjustment.

Figure 8-28. Open Loop Procedure



NOTES

1. Output power set at 10 dBm. Offset depends on power level and EXT/MTR ALC "CAL".
2. CW mode.
3. Adjust EXT/MTR ALC "CAL" to attain waveshape.

Figure 8-29. Open Loop Waveforms

Error Sample and Hold and Main ALC Amp, Blocks I and L

U2D is a non-inverting unity-gain summing amplifier. Under leveled conditions, both U2D pin 10 and TP8 should be nearly 0.0 VDC. Under any conditions (except during "hold"), U2D pin 10 and TP8 should be at the same voltage. If not, suspect U2D, Q5, or the sample and hold driver, Q11.

U9 forms an inverting integrator. When TP8 is positive, TP5 should be at −7 VDC. If not, suspect U1D, VR2, VR3, or U9. When TP8 is negative, TP5 should be at +5 VDC. If this is not the case, suspect U9.

The following procedure can be used to check U2D and U9:

1. Use a jumper to ground A4TP11.
2. Set power for −5 dBm at any CW frequency.
3. Press HP 83595A **[EXT]** ALC.
4. To check U2D, monitor U2D pin 10 and TP8 while adjusting the EXT/MTR ALC CAL screw between the extremes of its range. Both U2D pin 10 and TP8 should vary between approximately +0.5 and −0.5 VDC.
5. Verify U9 by adjusting the CAL screw as described above and monitoring TP5. Since U9 is an integrator, TP5 should saturate and clamp (due to VR2 and VR3) at −7 VDC and +5 VDC, respectively. (When sweeping across a bandswitch, RF blanking pulses will saturate TP5 at +5 VDC regardless of input.)
6. Remove jumper from A4TP11 to ground.

Q2 is an emitter-follower followed by a common-base stage (Q1), with two diodes in between. These transistors are acting as an exponential current driver. To verify the operation of these transistors and the subsequent components of the RF path do the following steps. For a quicker check, measure the biases and base-emitter voltages to check for damaged transistors.

1. Lift the U9 side of R54.
2. Inject a 1 to 10 Hz square wave signal through the lifted end of R54. The amplitude of the square wave signal should be approximately 3 Vp-p, offset from zero. The positive portion of the signal should not exceed +1.0V with the negative portion at approximately −2.0V.
3. Use a crystal detector, power meter or a scalar network analyzer to observe an inverted square wave at the RF output.

Further troubleshooting of these blocks can be continued by following the open loop procedure outlined in Figure 8-28 and checking for the waveforms provided in Figure 8-29.

Modulator Drivers, Blocks N and O

The voltage-to-current conversion and current gain needed to drive the modulators is provided by Q2 and Q1 on the output of the main ALC amplifier. As the voltage increases at TP5 so does the current to the modulators, shunting more RF energy to ground and allowing less to pass through. Since the modulators are essentially current-controlled, the voltages measured at TP5, P1-19, and P1-44 do not vary much over a wide range of modulator attenuations.

To establish a bias level for the mod driver stages, TP5 can be forced high (+5 VDC). Using a jumper, ground A4TP11. Press HP 8350 **[CW]** and select a CW frequency in the appropriate band. Select **[EXT]** ALC, and enter an RF power level of −5 dBm via front panel controls. Rotate the EXT/MTR ALC CAL knob fully counter-clockwise. Verify a signal level of approximately +5 VDC at TP5. Remove the jumper from A4TP11.

R101 should be selected so that the peaking in band 0 matches the peaking in bands 1 to 4. This peaking is due to the response of the ALC loop. R92 is adjusted for 50% duty cycle of the square wave.

Set the sweep oscillator for a CW frequency and SQ MOD on. Connect the RF output to a crystal detector and oscilloscope. Using a function generator, drive the AM input of the sweep oscillator with a sine wave swept in frequency from DC to 400 kHz (trigger the oscilloscope with the ramp from the function generator). The oscilloscope shows the response of the ALC loop. Vary the frequency and observe the peaking when in band 0 and in bands 1 to 4. Select R101 to match the peaking. Lower values tend to raise the gain in band 0. The minimum value is 2.7 kohms. Disconnect the function generator and press **[⊔⊓MOD]** to turn it on. While observing the square wave on the oscilloscope, adjust R92 for 50% duty cycle.

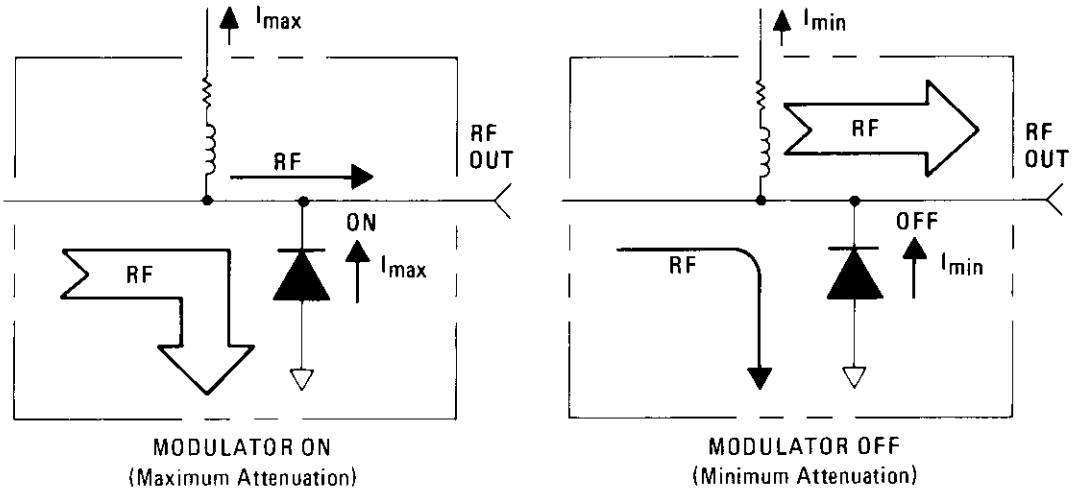


Figure 8-30. Simplified Modulator Schematic

Modulators A17 and A16

The two internal modulators for this plug-in are housed in combination microcircuit packages: A17 modulator/mixer (band 0), A16 modulator/splitter (bands 1 through 4). Figure 8-30 provides a simplified schematic for these positive-bias shunt-type attenuators. As more current is supplied through the modulator bias pin, the shunt diode turns on harder, sinking more RF power to ground and allowing less to reach the front panel.

The modulators are checked simply by noting whether the actual RF attenuation is appropriate to the modulation bias present.

NOTE: Turn off line power before removing or installing any assembly.

If low or no RF power is observed, remove all modulator bias currents simply by removing the A4 assembly from the motherboard. With no bias current, the RF power should pass through the modulator unhindered. If this is not the case, check the modulator diode as follows:

Set the RF plug-in for **[EXT]** ALC mode. Attach a jumper from A4TP11 to ground. Enter −2 dBm RF power, and select a CW frequency in the appropriate band. Rotate the EXT/MTR ALC CAL screw fully clockwise. This should result in −7 VDC at TP5, essentially removing bias from the modulators. Measure the voltage across R49. It should be 0V. If this is not the case, isolate each modulator from its drive circuitry by applying a piece of cellophane tape to the appropriate pin edge connector: P1-44 for band 0, or P1-19 for bands 1 through 4. If the voltage across R49 now measures 0V, the modulator diode is probably shorted. If the voltage across R49 still does not measure 0V, suspect the band blanking circuitry: U8B and Q15 for band 0, or U8C and Q14 for bands 1 through 4. Remove the jumper from A4TP11.

NOTE: Remove any tape applied to the pin edge connectors in the previous procedure.

If the modulators appear to be functioning properly, check the following RF levels with a power meter or spectrum analyzer. When checking power levels internal to the RF signal path, ensure that all critical ports are terminated in 50 ohms.

1. If power is low in all bands, check the RF level at the rear panel AUX OUT connector. Refer to the RF schematic diagram at the end of Section 8 for the proper levels.

2. If power is low in band 0 only, measure the RF levels around A18 modulator/mixer. With no modulation, approximately +13 dBm should be measured at the "LO" input of A18, with approximately −10 dBm at the output. If no output is measured, make sure the A11 cavity oscillator is yielding at least +8 dBm.

3. If the RF output for bands 1 to 4 is low, check the RF levels around power amplifier A14 with no modulation. A14 should output approximately +26 dBm with about +13 dBm at the input.

If maximum unleveled RF power is observed, attempt to achieve maximum attenuation (minimum RF transmitted). On the RF plug-in, press **[EXT]** ALC. Attach a jumper from A4TP11 to ground. Enter −2 dBm RF power, and select a CW frequency in the appropriate band. Rotate the EXT/MTR ALC CAL screw fully counter-clockwise. The voltage level at TP5 should be +5 VDC. Concurrently, the voltage levels at the output of the mod drivers, P1-44 (band 0) and P1-19 (bands 1 through 4), should be approximately +0.6 VDC to +0.8 VDC.

1. If the voltages are significantly higher than this, the modulator diode is probably open.

2. Check TP6 for approximately +2.0 VDC. The difference between the test point and the corresponding pin-edge connector gives an indication of how much current is flowing to the modulator.

Input Sample and Hold/Sample and Hold Drivers, Blocks E and K

There are adjustments to improve the shape of the square wave. C23 in block E and R99 in block K are used to eliminate offset in the input sample and hold, and sample and hold driver circuits respectively. They act to effectively cancel charge passed through the gate to source capacitance of the FET. Refer to 5-16. ALC Gain Adjustment in Section 5 of this manual.

A4 ALC (Automatic Leveling Control) Assembly, Circuit Description

INTRODUCTION

The A4 ALC (automatic leveling control) assembly is part of a closed loop power leveling function, designed to control the amplitude of the RF output power. The section below describes loop operation, including some components external to the A4 ALC assembly. The rest of this operational theory is devoted to detailed description of the circuits found on the A4 assembly.

GENERAL

The circuits which accomplish power control and power leveling can be broken into two categories: internal loop circuitry and external components of the loop. Figure 8-31 illustrates this theme.

The power level reference leg of the ALC establishes the desired power level. This is accomplished by pressing the plug-in **[POWER LEVEL]** key and rotating the RPG or entering the desired reference on the HP 8350 front panel data entry keys. This leg of the ALC is not an interdependent part of the loop as shown in Figure 8-31.

The feedback path of the ALC loop samples the actual RF output power and produces a voltage proportional to RF amplitude. This voltage is converted to log scale and compared with the power level reference signal. If the voltages at the summing junction are not of equal magnitude an error voltage is generated. This error voltage is amplified and converted to a current drive for the RF modulators which vary the transmitted RF power to correct the error and achieve the desired RF power level.

ADDRESS DECODER AND CONTROL LATCHES, BLOCK A

U12 is a 3-to-8 decoder, selecting address 2C07H when it is present on the address bus. This address serves as a chip enable for octal latch U13. Information on the data bus is then latched into U13 and used throughout the A4 assembly. U14 and U15 have been added to provide the proper outputs for all three ALC leveling modes.

DETECTOR INPUTS AND SELECTION SWITCHES, BLOCK B

Control lines MUX A0B and MUX A1B are encoded with leveling mode and band selection information. The lines are decoded in Table 8-13. U6 decodes these control lines to select the proper detector input for the desired operating mode.

R43 and R14 BIAS adjustment offset the band 0 internal detector so that 0 volts at TP7 corresponds to no RF power.

EXT/MTR ALC input provides external crystal leveling capability within the −10 to −200 mV range and power meter leveling capability within the 0 to +1V range. VR4 and VR5 provide protection against transients. Two Schottky diodes, CR1 and CR2, are mounted between the EXT/MTR ALC connector and the front panel casting for similar protection.

When **[MTR]** (power meter) leveling is selected, the power meter is used in conjunction with the internal leveling detector. U1A routes the power meter signal to a separate power meter log amplifier. The internal leveling detector is routed through U6B and the input sample and hold is routed to the main log amplifier. The internal leveling detector compensates for the reponse of the power meter and prevents instability while at the same time permitting reasonable sweep times.

SAMPLE AND HOLD DRIVER, BLOCK K

Q10 and Q11 act as complementary pairs, controlling the input sample and hold, and error sample and hold circuits respectively. The complementary pairs improve the action of the sampling FETS Q5 and Q6 by reducing the error signal passed through gate to source capacitance. The sample and hold function of the ALC loop is used in conjunction with pulse and square wave modulation. When L PULSE ENABLE is high, and either L PULSE or SQ MOD input is low, Q10A and Q11B turn on causing Q10B and Q11A to turn off, thereby initializing the hold mode.

The frequency of the sampling mode is dependent on the L PULSE or SQ MOD input. When the system is used with the HP 8756A or 8757A scalar network analyzer, the SQ MOD input is a 27.8 kHz square-wave, controlling the gates of Q5 (block I) and Q6 (block E). Refer to the *HP 8350 Operating and Service Manual*, Section 5, for the 27.8/1 kHz oscillator adjustment. A time delay set by R64 and C26 causes an approximate 5 usec delay, enabling the RF signal to come to full power before releasing HOLD and thus preventing overshoot. The sample level is maintained during the OFF pulse, thus preventing saturation of the log and main amplifiers.

INPUT SAMPLE AND HOLD, BLOCK E

The input sample and hold function prevents the log amplifier from saturating during square wave modulation.

U16 is a unity gain follower with internal feedback that buffers the detector input. R78 compensates for the offset voltage of the operational amplifier . Q6 and C21 perform the sample and hold function. C23 is used to reduce error due to the gate to source capacitance of Q6.

POWER METER LOG AMPLIFIER, BLOCK F

The power meter log amplifier is used in conjunction with the log amplifier in ALC **[MTR]** mode. The power meter log amplifier sets the power level and takes care of low frequency variations, while the log amplifer takes care of the high frequency variations.

U5B is unity gain follower which buffers the input of U5D. Logarithmic scaling is performed by Q3A in the feedback loop of U5D. The base-emitter voltage of Q3A is exponentially related to its collector current, hence the logarithmic action of the amplifier. Q3B compensates the log amplifier over temperature. U5A is a standard non-inverting amplifier, with its gain controlled by R33 and R32. CR3 prevents oscillation in the log amplifier.

LOG AMPLIFIER, BLOCK G

The logarithmic scaling function is performed by Q9A in the feedback loop of U17. Q9A collector current is proportional to the voltage at TP10 and exponentially related to its base-emitter voltage. Therefore, Q9A emitter voltage is logarithmically related to the input voltage at TP10.

Q9B compensates the log amplifier against changes in reverse saturation current with temperature.

CR9 clamps the output of U18 to 0.6V above the input voltage to U17, preventing oscillations.

U6A decodes MUX A0B and MUX A1B (Table 8-13) to select the proper offset voltage for power calibration at the low end of the plug-in power range. In EXTernal ALC, the power level calibration is set with the front panel EXT CAL potentiometer.

U18 amplifies the logged output for comparison with the power level summing signal. R9 and R10 adjust the gain of U18, and calibrate midrange power levels for their respective bands.

Guarded-gate FETs, Q7, Q8, and Q16, select the appropriate detector return for INTernal, EXTernal, and PM (power meter) leveling.

POWER LEVEL REFERENCE, BLOCK C
POWER LEVEL SUMMING, BLOCK H

U11 is a 12-bit microprocessor-compatible DAC, which latches data in three 4-bit nibbles. The −10V REF input sets the DAC for a maximum output (TP2) of +10V. The voltage at TP2 is the product of −10VREF and the fractional binary input of the DAC.

The voltage at TP1 is the sum of several voltages, depending on the operating mode of the plug-in. U2A sums PWR SWP/COMP and AM inputs. In addition, selected feedback resistors, R7 and R8, reduce gain to compensate for detector deviation from square-law at the upper limits of the plug-in power range.

The EXT CAL input is summed through amplifier U2C. R30, in the feedback loop of U2C, provides temperature compensation for the log amplifier and detectors.

ERROR, SAMPLE AND HOLD, BLOCK I

The error sample and hold function prevents the main ALC amplifier from saturating during pulse and square-wave modulation.

U2D pin 10 is the summing junction for the power level summing output, log amplifier output, and FREQ TRK V, which is a 0 to 5 volt ramp proportional to the SYTM DRIVE voltage. R1 (SLP) adjusts the overall slope of band 0.

Under leveled power conditions, the voltage at U2D pin is zero. A non-zero voltage represents an error and forces a change in modulator current until power is again level.

U2D buffers the error voltage. Q5 and the following integrating circuit (U9) perform the sample and hold. C7 eliminates error due to the gate-to-source capacitance of Q5.

LOG AMPLIFIER SELECTOR, BLOCK J

The log amplifier selector circuit selects a through path for the log amplifer, or combines its output with that of the power meter log amplifier (MTR). In MTR mode, R84 and C3 act as a high-pass filter, to shape the output of the log amplifier, which is then combined with the power meter log amplifier output. The combination of the two prevents instability when using certain power meters.

In switch U4, A and B are open, C is closed in INT or EXT DET mode. The opposite is true in MTR mode.

MAIN ALC AMPLIFIER, BLOCK L
UNLEVEL SIGNAL, BLOCK M

Both inputs to integrator U9 are at virtual ground under leveled power conditions, allowing for immediate response to an input error voltage.

R15 optimizes the speed at which the loop responds to power level changes.

L RFB goes low during bandswitching to blank the RF power, thus preventing the loop from saturating. When the HP 8350 **[RF BLANK]** key is pressed, L RFB goes low during retrace and U1D closes, pulling current through C4, forcing TP5 high and turning on the PIN modulators.

Under unleveled conditions, VR2 and VR3 will clamp the output of U9 at approximately +5 and −7 volts, preventing negative or positive saturation. When the output of U9 approaches −2 volts, comparator U10 activates the front panel LED indicating unleveled power.

U8D is not used.

Collector current in common-base transistor Q1 is exponentially related to the base-emitter voltage. PIN modulators are driven exponentially to maintain constant loop gain.

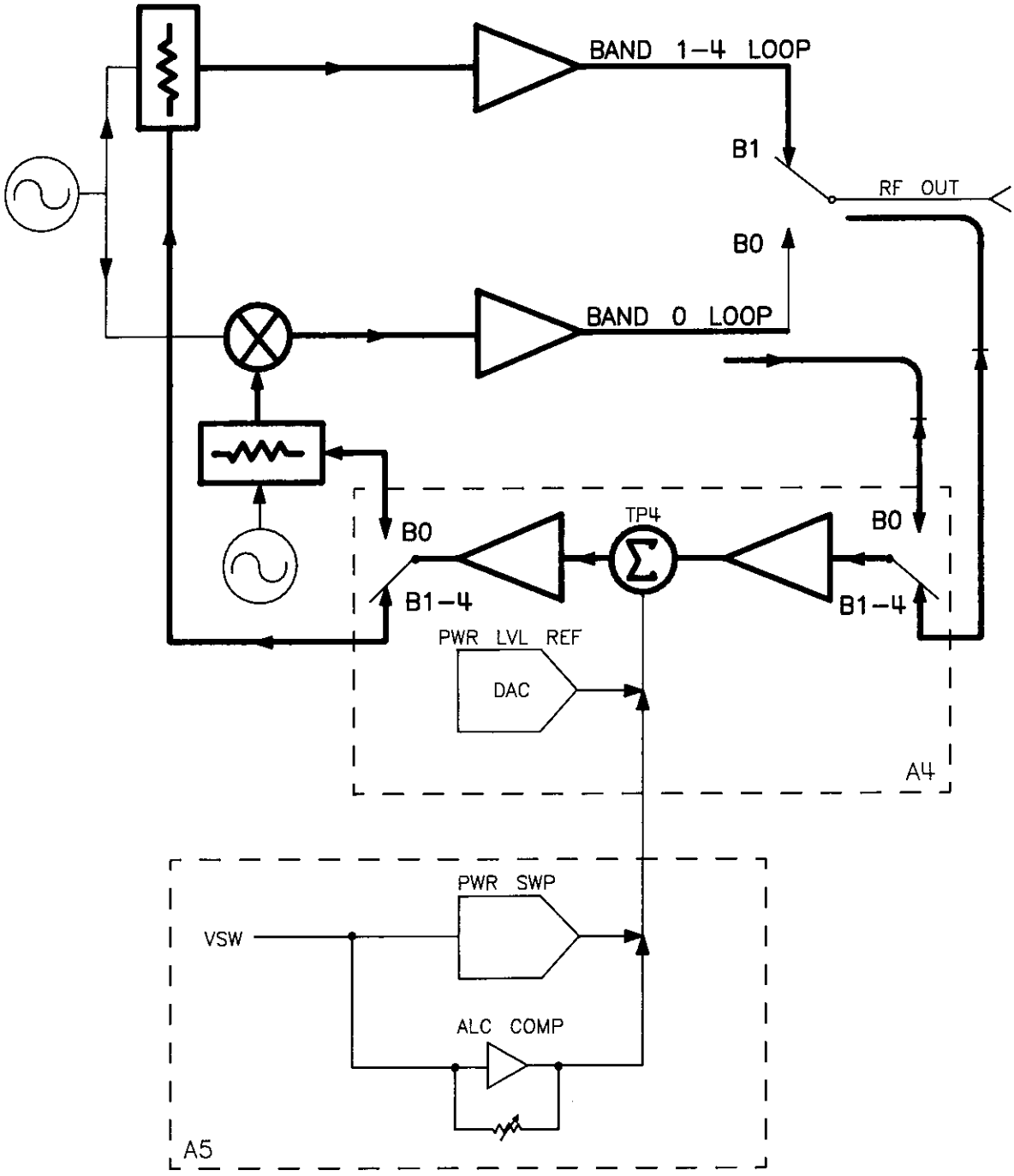
Emitter follower Q2, CR5, and CR4 control the gain of the exponential current drive.

PIN MOD 0 DRIVER, BLOCK O
PIN MOD 1 DRIVER, BLOCK N

R101 and R105 compensate for the loss of modulator sensitivity with decreasing bias current. R101 is factory selected to make the modulator characteristics for band 0 match the modulator characteristics for bands 1 through 4 as closely as possible.

Q15 (BLOCK O) or Q14 (BLOCK N) increase the isolation between band 0 and band 1 by shutting off the modulator in the inactive band. Q12 and Q13 provide square-wave modulation and RF blanking when selected.

R92 is factory selected to match the modulator for best square wave modulation symmetry.



NOTE

DARKER LINES REPRESENT THE BAND 0 AND BAND 1–4 LEVELING LOOPS. LIGHTER LINES REPRESENT CIRCUITRY WHICH CONTRIBUTES TO, BUT IS NOT CONTAINED WITHIN, EITHER LOOP.

Figure 8-31. Simplified ALC Block Diagram

Table 8-15. A4P1 Pin-Outs

A4P1

PIN	SIGNAL	I/O	TO/FROM	FUNCTION
1 23	EXT DET RET EXT DET	IN IN	J2 J2	P B
2 24	L UNLVL EXT CAL	OUT IN	A6P1-40, A10J1-12 A10J1-41	M H
3 25	PWR REF	OUT	NOT USED NOT USED	C
4 26	AM FREQ TRK V	IN IN	P1-A4 A10J1-36	C I
5 27	PWR SW/COMP +5V	IN IN	A5P1-23 A3P1-6,7	C P
6 28	 −15V	 IN	NOT USED P2-28	 P
7 29	+10V L RFB	IN IN	P1-8 P2-56	P L, O
8 30	GND DIG GND DIG			P P
9 31	BD1 BD0	IN IN	A3P1-9 A3P1-31	A, C A, C
10 32	BD3 BD2	IN IN	A3P1-10 A3P1-32	A, C A, C
11 33	BA1 BA0	IN IN	A3P1-11 A3P1-33	A, C A, C
12 34	BA3 BA2	IN IN	A3P1-12 A3P1-34	A, C A, C
13 35	BD5 BD4	IN IN	A3P1-13 A3P1-35	A A
14 36	BD7 BD6	IN IN	A3P1-14 A3P1-36	A A
15 37	GND ANLG GND ANLG			P P
16 38	+20V +15V	IN IN	NC P2-29	P P
17 39	−10V −40V	IN IN	P1-13 P1-11	P P
18 40	L INST1 SQ MOD	IN IN	A3P1-8 P2-26	A, C K, O
19 41	MOD 1 L PULSE	OUT IN	A10-E1 A6P1-25	N K
20 42	INT DET 1 INT DET RET	IN IN	CR1 CR1	B B
21 43	INT DET 0 −10V REF	IN IN	A10-E4 A8P1-3	B C
22 44	MOD DRIVE MOD 0	OUT OUT	NOT USED A10J5-16	L O

Troubleshooting the A5 FM Driver Assembly

INTRODUCTION

For troubleshooting purposes, the A5 FM driver is divided into three groups.

YO/SYTM main coil FM driver and YO FM coil driver circuits

FM configuration control circuits

Power sweep and ALC flatness adjustment circuits

YO/SYTM MAIN COIL FM DRIVER AND YO FM COIL DRIVER TROUBLESHOOTING

The most likely indication of a failure in these circuits is unpredictable or no FM operation. A failure in these circuits can also cause excessive residual FM or frequency offset.

Troubleshooting is divided into two ranges of modulation frequency. For FM frequencies less than or equal to 700 Hz, Table 8-16 provides voltages for troubleshooting. For FM frequencies greater than or equal to 700 Hz, Figure 8-36 provides waveforms for troubleshooting. The voltages and waveforms are arranged horizontally by test point and vertically by the FM input frequency. Figure 8-35 shows the test setup required to obtain the waveforms.

Table 8-16. LO Frequency FM Troubleshooting Voltages

Setup Condition	U7-7	TP2		TP3	
		20 MHz/V	6 MHz/V	20 MHz/V	6 MHz/V
FM INPUT = 100 Hz A5TP11 = 1Vp-p F.P. Phaselock (A3S1-8 Closed)	0.8Vp-p All Bands	0.8Vp-p All Bands	0.48Vp-p All Bands	Band 0=0.8Vp-p Band 1=0.8Vp-p Band 2=0.4Vp-p Band 3=0.28Vp-p Band 4=0.24Vp-p	Band 0=0.48Vp-p Band 1=0.48Vp-p Band 2=0.24Vp-p Band 3=0.16Vp-p Band 4=0.06Vp-p
FM INPUT = 100 Hz A5TP11 = 1Vp-p AUX OUT Phaselock (A3S1-8 Open)	0.8Vp-p All Bands	Band 0=0.8Vp-p Band 1=0.8Vp-p Band 2=3.2Vp-p Band 3=4.8Vp-p Band 4=3.3Vp-p	Band 0=0.48Vp-p Band 1=0.48Vp-p Band 2=0.96Vp-p Band 3=1.44Vp-p Band 4=0.94Vp-p	0.8Vp-p All Bands	0.48Vp-p All Bands
FM INPUT = 700 Hz A5TP11 = 1Vp-p F.P. Phaselock (A3S1-8 Closed)	0.64Vp-p All Bands	0.64Vp-p All Bands	0.2Vp-p All Bands	Band 0=0.64Vp-p Band 1=0.64Vp-p Band 2=0.32Vp-p Band 3=0.22Vp-p Band 4=.16Vp-p	Band 0=0.2Vp-p Band 1=0.2Vp-p Band 2=0.1Vp-p Band 3=0.07Vp-p Band 4=0.05Vp-p
FM INPUT = 700 Hz A5TP11 = 1Vp-p AUX OUT Phaselock (A3S1-8 Open)	0.64Vp-p All Bands	Band 0=0.64Vp-p Band 1=0.64Vp-p Band 2=1.28Vp-p Band 3=1.9Vp-p Band 4=2.5Vp-p	Band 0=0.2Vp-p Band 1=0.2Vp-p Band 2=0.4Vp-p Band 3=0.6Vp-p Band 4=0.74Vp-p	0.68Vp-p All Bands	0.2Vp-p All Bands

NOTE: Before altering the switch settings on A3S1, write down the present configuration. Return the switches to their original status after troubleshooting.

Prior to performing the test procedure, preset the A3S1 configuration switch sections 5, 6, and 8 to the closed (0) position. Several of the troubleshooting waveforms require different switch settings. A description of each switch setting follows.

For 6 MHz/V sensitivity – set A3S1-5 to the open (1) position.

For 20 MHz/V sensitivity – set A3S1-5 to the closed (0) position.

For DC coupled mode – set A3S1-6 to the open (1) position.

For cross-over coupled mode – set A3S1-6 to the closed (0) position.

For front panel phaselock mode – set A3S1-8 to the closed (0) position.

For the AUX OUT phaselock mode – set A3S1-8 to the open (1) position.

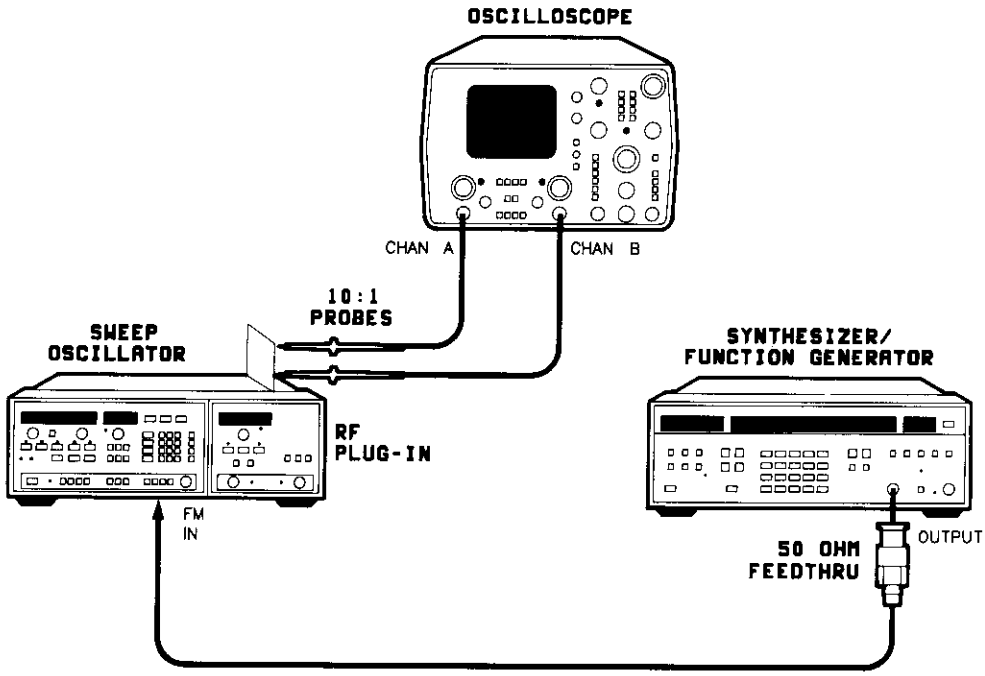


Figure 8-35. A5 Troubleshooting Test Setup

NOTE: The HP 8350 front panel **[INSTR PRESET]** key must be pressed after each switch position change in order for the selection mode to take effect.

1. Adjust the function generator frequency and amplitude controls to obtain a 1 volt peak-to-peak waveform at TP11 for the frequency tested.
2. Verify the waveforms and voltages in the corresponding row.

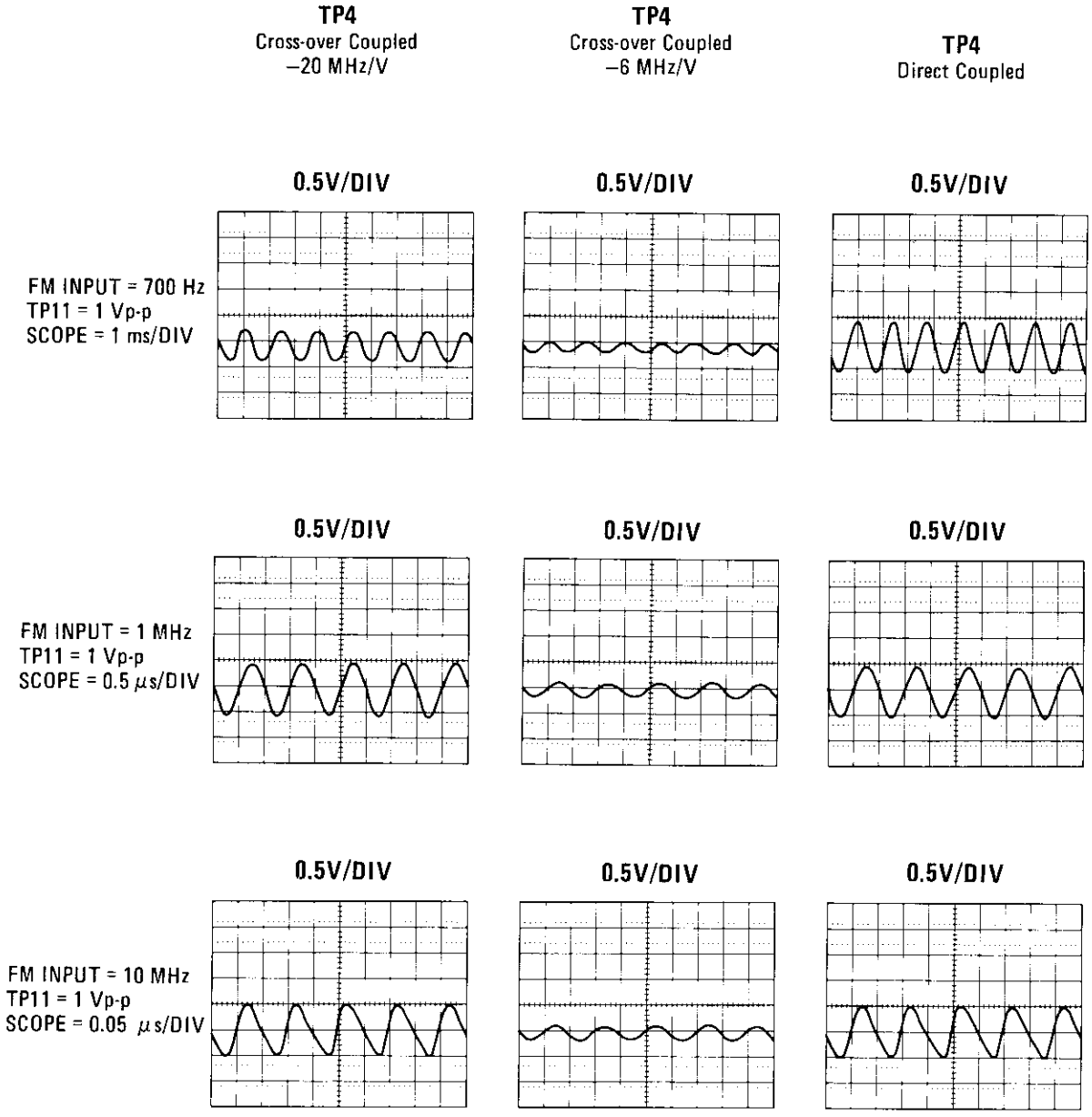


Figure 8-36. A5 Troubleshooting Waveforms (1 of 2)

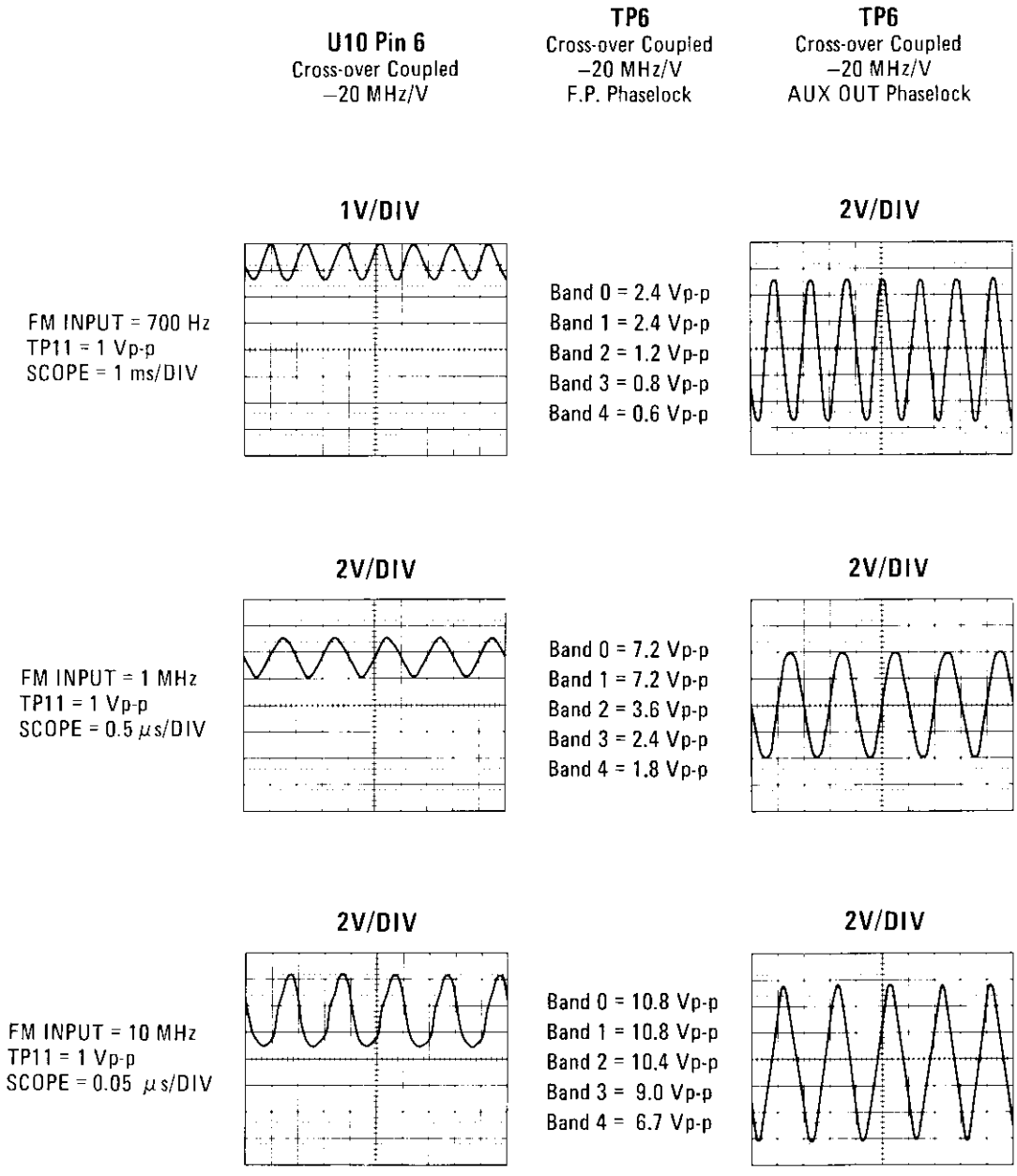


Figure 8-36. A5 Troubleshooting Waveforms (2 of 2)

FM CONFIGURATION CONTROL CIRCUITS TROUBLESHOOTING

The FM configuration control circuits include the address decoder, control latches, relays K1 and K2, and analog switches U3C and U11. Incorrect or no operation in a specific configuration mode is the most likely result of a failure in these circuits.The troubleshooting procedure for these circuits uses several of the HP 8350 sweep oscillator operator initiated self tests. Separate tests for each section of the configuration control circuits are provided in the following paragraphs.

Address Decoder

Check proper address decoder operation by performing a minor address decoder self test.

Press **[SHIFT] [5] [4]** minor address decoder test

Check the address decoder outputs LEN4, LEN5 and LEN6 as shown in Figure 8-37.

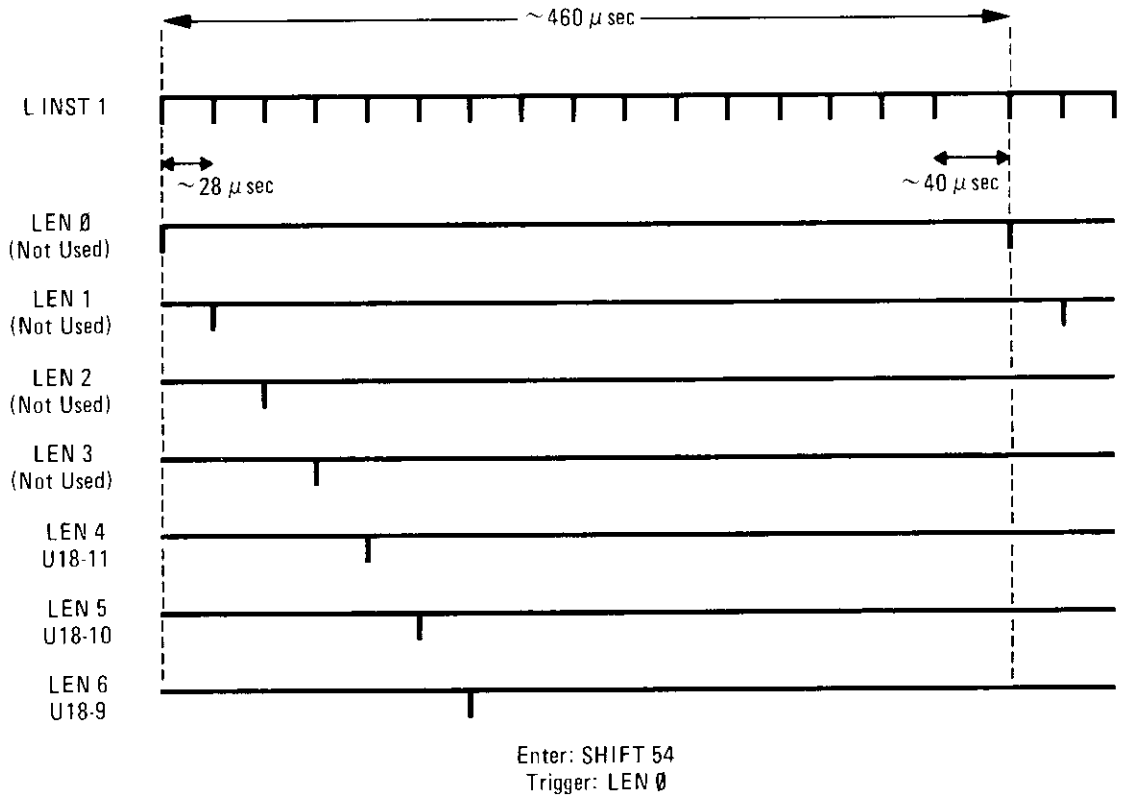


Figure 8-37. Address Decoder Timing Diagrams

Control Latches

Control latches U6 and U16 are checked by performing a hexadecimal data rotation write to U6 and U16, and then checking the outputs for the waveforms shown in Figure 8-2. The oscilloscope should be triggered from pin 15 of the addressed data latch.

Exercise U16 with hex data rotation write.

Press **[SHIFT] [0] [0]**	hex data mode
[2] [GHz] [0] [4]	address location 2C04 (U16)
[M4]	hex data rotation write

Check the outputs of U16 against waveforms shown in Figure 8-2.

To check control latch U6, press **[INSTR PRESET]** then repeat the above key entry sequence using address location 2C06.

Relays K1 and K2

A known FM input is applied and the waveform at TP4 is monitored. The hex data write feature of the HP 8350 is used to control relays K1 and K2. Connect the equipment as shown in Figure 8-35. Adjust the function generator for a 500 Hz, 1 V peak-to-peak output with a +0.5 VDC offset (use function generator offset control).

To check relay K1:

Press **[SHIFT] [0] [0]**	hex data mode
[2] [GHz] [0] [4]	address location 2C04 (U16)
[M2] [.] [8]	hex data write A8

Relay K1 should be open. Verify that there is a signal centered around 0 VDC at TP4.

Press **[M2] [8] [8]**	hex data write 88

Relay K1 should now be closed. Verify that the signal at TP4 is offset from being centered around 0 VDC.

To check relay K2:

Press **[M2] [BK SP] [8]**	hex data write F8

Relay K2 should be closed. Note the level of the signals at TP3 and TP4.

Open relay K2:

Press **[M2] [dBm] [0]**	hex data write E8

Relay K2 should now be open. Verify that the level of the signals at TP3 and TP4 is less than previously noted.

High/Low FM Switching

Analog switches U3C, U13A, and U11 are checked by using the hex data write feature of the HP 8350 to control the switches. A known FM input is applied and switch operation is verified.

Connect equipment as shown in Figure 8-35. Adjust the function generator for a 500 Hz, 1V peak-to-peak output.

Press **[SHIFT] [0] [0]**	hex data mode
[2] [GHz] [0] [4]	address location 2C04 (U16)
[M2] [dBm] [8]	hex data write E8

Analog switches U3C and U13A should be closed. Verify there is a signal at TP3 and TP2.

Press **[M2] [dBm] [0]** hex data write E0

Analog switches U3C and U13A should be open. Verify that there is no signal at TP3 and TP2.

Press **[M2] [dBm] [8]** hex data write E8

Analog switch U11 should be set to the zero position. Verify that a signal is present at TP6.

Press **[M2] [dbm] [GHz]** hex data write EC

Analog switch U11 should be set to the one position. Verify that no signal is present at TP6.

POWER SWEEP/ALC ADJUSTMENTS TROUBLESHOOTING

The most likely indication of a failure in these circuits is either incorrect or no operation of the power sweep function or inability to adjust the output power flatness. The power sweep DAC U17 is exercised by initiating the power sweep DAC self test, and the DAC output is checked at TP8.

Press **[SHIFT] [5] [1]** power sweep DAC self test

Verify that the waveform at TP8 corresponds with the waveform in Figure 8-38.

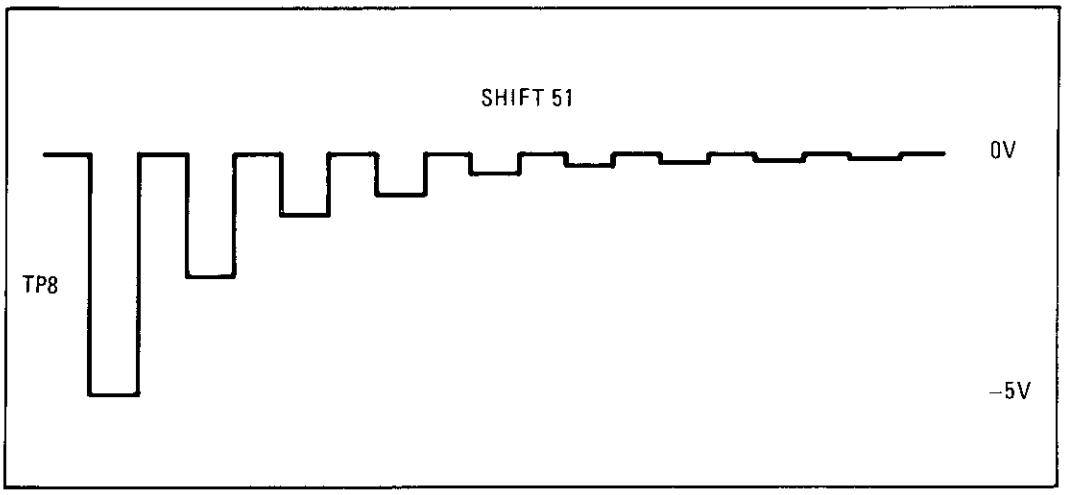


Figure 8-38. Power Sweep DAC Self Test Waveform

A5 FM Driver, Circuit Description

GENERAL

The A5 FM driver is divided into three major sections: the YO/SYTM main coil FM drivers, the YO FM coil driver, and the ALC flatness adjustments and power sweep circuits for the A4 ALC assembly.

The FM input signal from the rear panel of the HP 8350 sweep oscillator provides the input to both the YO/SYTM main coil and FM coil driver circuits. For low frequency FM inputs, the YO and SYTM band select amplifiers scale and buffer the FM signal to produce outputs that are summed with the tuning voltage on their respective driver boards assemblies (A7 SYTM driver and A8 YO driver). Thus, these low frequency FM outputs are an extra tuning voltage input to the YO and SYTM drivers, and may be used for phase locking, frequency offsetting, or low frequency FM applications (where up to 75 MHz deviations are required). The FM coil driver scales and buffers the FM input signal to produce the current drive for the FM coil in the YIG oscillator for smaller deviation but wideband (up to 10 MHz) FM applications. A current drive for the SYTM is not necessary because the SYTM bandwidth is wide enough to pass small frequency variations. Relay switches provide the option of selectable sensitivities of −6 or −20 MHz/Volt and/or DC coupling the FM input to the FM coil driver circuits. In the DC coupling mode, the main coil driver is shut off and the FM coil driver operates over the frequency range of DC to 10 MHz with −20 MHz/Volt sensitivity. The relay switches are controlled by the state of the configuration switch on the A3 digital interface assembly.

The ALC flatness adjustments circuit is used to flatten output power versus frequency by introducing an error voltage into the ALC reference channel. The power sweep circuit is activated by the front panel POWER SWEEP pushbutton and produces a scaled ramp that is summed with the ALC reference voltage causing the output power to increase level versus sweep (the amount of which is selected on the front panel).

YO AND SYTM MAIN COIL FM DRIVERS, BLOCKS C, D, and H

The YO and SYTM main coil FM drivers scale and buffer the HP 8350 rear panel FM input signal for FM frequencies between DC and 700 Hz to produce two outputs which are summed with the tuning voltage for the YO main coil on the A8 YO driver assembly and the SYTM on the A7 SYTM driver assembly. Low frequency amplifier/filter and the YO and SYTM band select amplifiers make up the YO and SYTM main coil FM driver. The FM input signal is filtered by 700 Hz low-pass filter R2/C1 and buffered by difference amplifier U7A. The gain of U7A is approximately 1.4. The output of U7A drives both the YO and SYTM band select amplifier circuits. Relay K2 is used to control the overall gain of inverting amplifiers U7B and U14D for the two sensitivities by changing the value of the input resistance. Relay K2 is either open or closed (shorting across parallel resistors R8 and R78) according to the state of control line 6 MHz/V SEL (1 = −6 MHz/Volt, 0 = −20 MHz/Volt sensitivity). The state of control line 6MHz/V SEL is determined by the position of the configuration switch on the A3 digital interface assembly. Since the SYTM may be tuned to the second or third harmonic of the YO, the LO FM outputs to the YO and SYTM drivers must be scaled according to the band of operation. This scaling is accomplished by the YO and SYTM band Select adplifier circuits. The gain of each amplifier is set by the YO and SYTM SEL inputs to the analog switches in their feedback paths. Table 8-17 lists the logic levels of these lines for each band. The YO band select amplifier output (TP3) is summed directly with main coil tuning voltage on the A8 YO driver assembly and the SYTM band select amplifier output (TP2) is summed directly with the SYTM tuning voltage on the A7 SYTM driver assembly. The YO and SYTM band select amplifiers are shut off with analog switches U3C and U13A when the DC coupling mode is selected (on the A3 assembly configuration switch) causing control line L LO FM OFF (Low = Low Frequency FM OFF) to be true.

Table 8-17. YO and SYTM Gain Select Truth Table

	Front Panel Phase Lock (A3S1-8=0)				Aux Out Phase Lock (A3S1-8=1)			
	B0	**B1**	**B2**	**B3**	**B0**	**B1**	**B2**	**B3**
YO SEL 1	0	0	1	1	0	0	0	0
YO SEL 2	0	0	0	1	1	1	1	1
YO SEL 3	0	0	0	0	0	0	0	0
SYTM SEL 1	1	1	1	0	1	1	0	0
SYTM SEL 2	0	0	0	0	0	0	1	0
SYTM SEL 3	0	0	0	0	0	0	0	1

YO FM COIL DRIVER, BLOCKS E, F, and I

The YO FM coil driver scales and buffers the HP 8350 rear panel FM input for frequencies between DC and 10 MHz to produce an output current that drives the YO FM coil. The FM coil driver is made up of a high-pass filter, buffers Q5A and Q5B, video amplifier U10, operational amplifier U19, and unity gain follower U20. The high pass filter is made up of capacitors C2 through C6 and resistors R11 and R12. The filter has a 3 dB cutoff frequency of about 700 Hz. When the FM driver is configured for the "crossover" mode as determined by the position of the configuration switch on the A3 digital interface assembly, the FM coil driver passes FM input signals above 700Hz and the low-pass filter in the main coil driver circuits will pass signals below 700 Hz. If the DC coupling mode is selected, the main coil driver is shut off and control line L DC COUPLE is true, activating relay K1. This shorts the high pass filter network, and the FM driver is active for frequencies of DC to 10 MHz.

Selectable sensitivities of −6 MHz/Volt and −20 MHz/Volt are available and determined by the state of control line 6MHz/V SEL (1 = −6 MHz/V, 0 = −20 MHz/V). When 6 MHz/V SEL is high, relay K2 is open and the FM input is scaled by a resistive divider made up of R11 and R12. When 6 MHz/V SEL is low, relay K2 is activated, shorting capacitors C4-C6 and resistor R11. The combination of C2, C3 and R12 still form a high pass filter with a cutoff of 700 Hz. Note that in the DC coupled mode the sensitivity is always −20 MHz/Volt.

The output of the filter network is limited to about ± 3V with a network made up of VR1, VR2, R14, R15, CR3, and CR4. Q5A and Q5B are connected as emitter followers and buffer the output of the filter network to video amplifier U10. Analog switch U11 is always set to switch position zero. Frequency response shaping to compensate for the roll-off versus frequency of the FM coil is produced by the network made up of C11, C12, C14, R21, R22, R23, R75, and L1 connected across pins 9 and 4 of U10. This network is actually in the emitter of the input differential amplifier of U10 producing greater gain with decreasing impedance. Figure 8-39 shows the approximate response versus frequency of the YO FM coil and the compensation network. Adjustments R19 (FM OFFSET), R75 (H1), and C14 (LO) adjust the shape of the compensation network response.

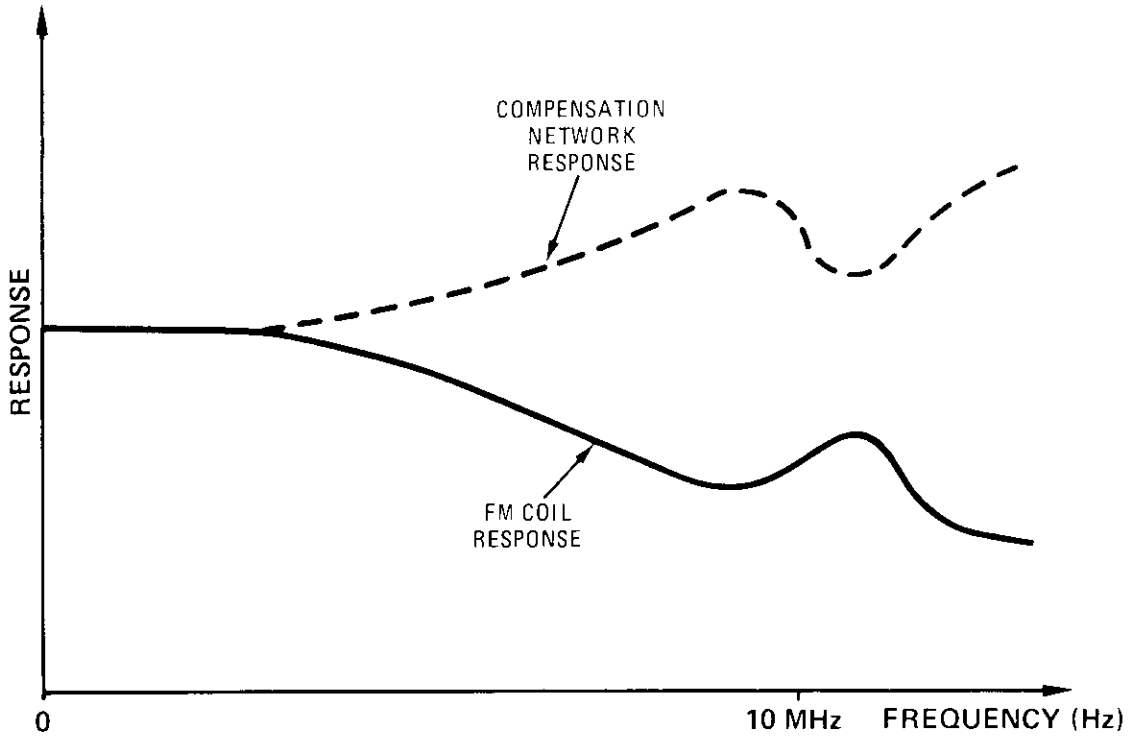


Figure 8-39. Plot of FM Coil Response Versus Frequency

The differential output of U10 drives the wideband output current driver, U19 and U20. The voltage difference between the outputs of U10 at pins 6 and 7 is converted to a proportional current which directly drives the YO FM coil. The overall voltage gain of the output current driver is determined by the YO SEL inputs to analog switches U12B, C and D and is selected according to the frequency band of operation. Resistive divider R30 through R32 sets the FM coil drive scale factor.

ADDRESS DECODER, BLOCK A

Address decoder U18 generates three control lines (LEN 4, LEN5 and LEN 6) by decoding the state of address lines BA0-3 and control line L INST 1. LEN 4 (Low Enable 4) and LEN 6 (Low Enable 6) load data into the control latches and LEN 5 (Low Enable 5) loads data into the power sweep DAC.

CONTROL LATCHES, BLOCK C

Control latch U6 stores the state of six control lines that are used to control the amplification factor of the FM input signal according to the frequency band of the RF output (bands 0 through 4). The control lines are loaded into U6 from data bus lines BD0 through BD5 when the LEN 6 signal from U18 makes a low to high transition.

Control latch, U16, stores the state of four control lines that are used to set the signal path and amplification factor of the FM input signal. The state of the control lines is determined by the position of switches 5 and 6 of the configuration switch on the A3 digital interface assembly. The control lines are loaded into U16 from data bus lines BD2 through BD5 when the LEN 4 signal from U18 makes a low to high transition.

ALC FLATNESS ADJUSTMENTS, BLOCK I

The purpose of the ALC flatness adjustment circuit is to produce an RF OUTPUT signal that is as flat as possible across the entire frequency band. The input of the ALC flatness circuit is a 0 to 5 Volt ramp (in full sweep) labeled FREQ TRK V (frequency tracking voltage). This ramp is dependent on the START and STOP frequency settings, so it will always be at least a portion of the 0 to 5 volt range.

The FREQ TRK V ramp is applied to four parallel circuits, each one adjusted to take effect at a different frequency (i.e., voltage threshold of FREQ TRK V) as the sweep progresses from START to STOP. Since the four circuits are identical (Q1, Q2, Q3, Q4), only the Q1 circuit will be discussed. Q1A is connected as a diode, is always conducting, and is in the circuit for temperature compensation of Q1B. The setting of adjustment BP1 (R34) determines at what point on the input ramp Q1B will conduct. When the summing point at the junction of U2C and R33 is at zero volts or greater, Q1B will conduct. The junction of resistors U1B and U1A form another summing point. U1B applies a positive-going ramp from Q1B to this summing point, and a negative-going ramp comes through U1A from the output of U14C. Slope adjustment SL1 adjusts the amount of negative-going ramp contributed to the summing junction through U1A, and thus determines the resultant contribution of the Q1 circuit to the input of U14A. That is, the resultant signal may be either a positive-going ramp or a negative-going ramp as required to make the RF OUTPUT signal flat over that frequency segment.

The composite correction signal from the four flatness adjustment circuits (Q1 through Q4) are summed at the input of U14A. This composite correction signal, PWR/SWP COMP, is then applied to the power level reference circuit of the A4 ALC assembly. TP1 shows this composite correction signal. Overall tilt is adjusted by SLP (slope) adjustment R48.

POWER SWEEP, BLOCK H

When POWER SWEEP mode is selected at the front panel, LEN 5 (Low Enable 5) is generated by U18, enabling U17 on. This allows power sweep data from data lines BDO through BD7 to be loaded into U17. This data selects the gain of U14B by connecting or removing resistors in series with the input to U14B. The signal path of VSW (0 to +10V) is through the selected gain resistors in U17 to the input, pin 6, of U14B. The feedback resistor for U14B is also within U17 and is internally connected to the input of the amplifier stage. The output of U14B is summed with the ALC flatness signal at the input of U14A and then goes to the power level reference circuit of the A4 ALC assembly.

When the plug-in front panel SLOPE key is depressed, data lines BD0 through BD7 redefine the gain of the power sweep circuit to compensate the slope of the RF output in dB/GHz.

Table 8-18. A5P1 Pin-Outs

A5P1

PIN	SIGNAL	I/O	TO/FROM	FUNCTION
1 23	SYTM LO FM PWR SW/COMP	OUT OUT	A7P1-1 A4P1-5	H J
2 24	YO LO FM FREQ TRK V	OUT IN	A8P1-1 A2J1-36	D J
3 25	VSW	IN	NOT USED P2-64	G
4 26			NOT USED NOT USED	
5 27	L INST1 +5V	IN IN	A3P1-8 A3P1-6,7	A K
6 28	−15V	IN	NOT USED P2-28	K
7 29	+10V	IN	P1-8 NOT USED	K
8 30	GND DIG GND DIG			K K
9 31	BD1 BD0	IN IN	A3P1-9 A3P1-31	B,G B,G
10 32	BD3 BD2	IN IN	A3P1-10 A3P1-32	B,G B,G
11 33	BA1 BA0	IN IN	A3P1-11 A3P1-33	A A
12 34	BA3 BA2	IN IN	A3P1-12 A3P1-34	A A
13 35	BD5 BD4	IN IN	A3P1-13 A3P1-35	B,G B,G
14 36	BD7 BD6	IN IN	A3P1-14 A3P1-36	G G
15 37	GND ANLG GND ANLG		NOT USED	J
16 38	+20V +15V	IN IN	NOT USED P2-29	K
17 39	−10V FM RET	IN IN	P1-13 P1-A3	K C,E
18 40	FM IN	IN	NOT USED P1-A3	C,E
19 41	FM RET	IN	NOT USED P1-A3	C,E
20 42	HI FREQ FM RET	OUT	A13A1J1 NOT USED	I
21 43	HI FREQ FM	OUT	A13A1J1 NOT USED	I
22 44	HI FREQ FM RET	OUT	A13A1J1 NOT USED	I

Troubleshooting the A6 Sweep Control Assembly

INTRODUCTION

The A6 sweep control assembly inverts and scales the tuning voltage (VTUNE) from the HP 8350 for use by the A7 SYTM driver and A8 YO driver. The A6 assembly also initates all bandswitch sequences.

NOTE: Unless specifically stated otherwise, the troubleshooting waveforms and voltages described below occur when the plug-in is sweeping across its full range (INSTR PRESET conditions).

BUFFERED TUNING VOLTAGE

NOTE: The BVTUNE output is normally scaled by the variable gain amplifier only for multiband (sequential) sweeps (with the TV buffer output used for single band sweeps). However, the A3S1 configuration switch (position 1) may be set to disable the selection of the TV buffer output for single band sweeps. This procedure assumes that A3S1 switch position 1 is set to the open position, thus enabling the A6 assembly to change scaling of the BVTUNE signal for single band and multiband sweeps.

A failure with the BVTUNE signal may cause both the YO and SYTM to sweep between improper frequency endpoints, or not sweep at all. For a full band sweep (0.01 to 26.5 GHz), the BVTUNE output at TP8 should be a series of 0 to −10V ramps (See Figure 8-44) For a single band sweep (i.e. 0.01 to 2.4 GHz), BVTUNE should be a single 0 to −10V ramp.

1. If both waveforms are incorrect, verify the TV buffer output at TP5 (Figure 8-44).
2. If BVTUNE is incorrect for only the full band sweep, the problem is most likely with the bandswitch DAC, variable gain amplifier, or the bandswitch circuitry. (The TV buffer is verified in single band sweep.)
   a. Check the bandswitch DAC output at TP1 as shown in Figure 8-44. If this signal is incorrect, run the bandswitch DAC test by entering **[SHIFT] [5] [6]**. Then check TP1 for the waveform shown in Figure 8-43.
   b. Verify correct operation of the variable gain amplifier by checking waveforms at TP4 and TP7 according to Figure 8-44. If any of the voltage levels are slightly out of tolerance, perform the sweep control and band overlap adjustments in Section 5. If the voltage at TP4 is 0V, verify that analog switch U10D is open.
   c. Verify operation of the bandswitch circuitry. Refer to the paragraphs titled Interrupt Control.
3. If BVTUNE is incorrect only for single band sweeps, verify that the SEQ BAND input to analog switch U10B,C is a logic low when sweeping only a single band. Also verify that configuration switch A3S1 switch number 1 is in the open position.

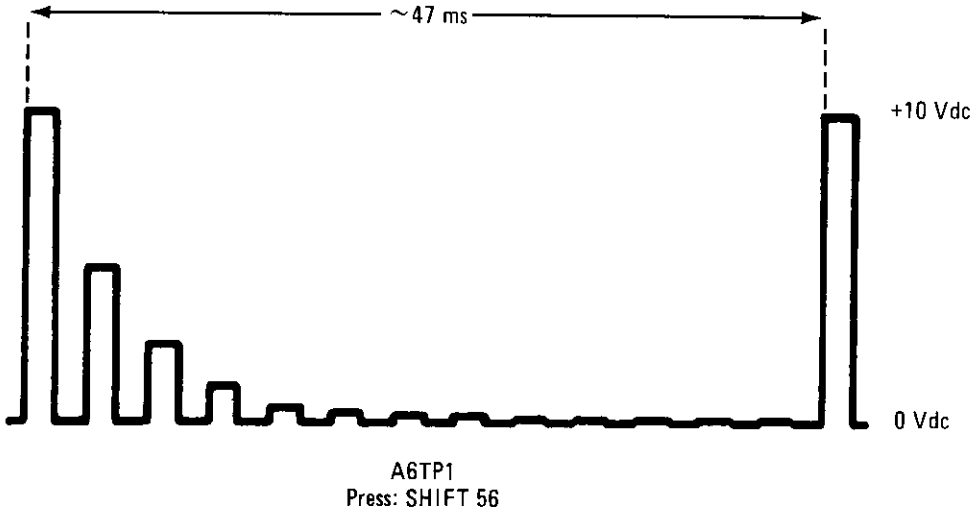


Figure 8-43. Bandswitch DAC Test Waveform

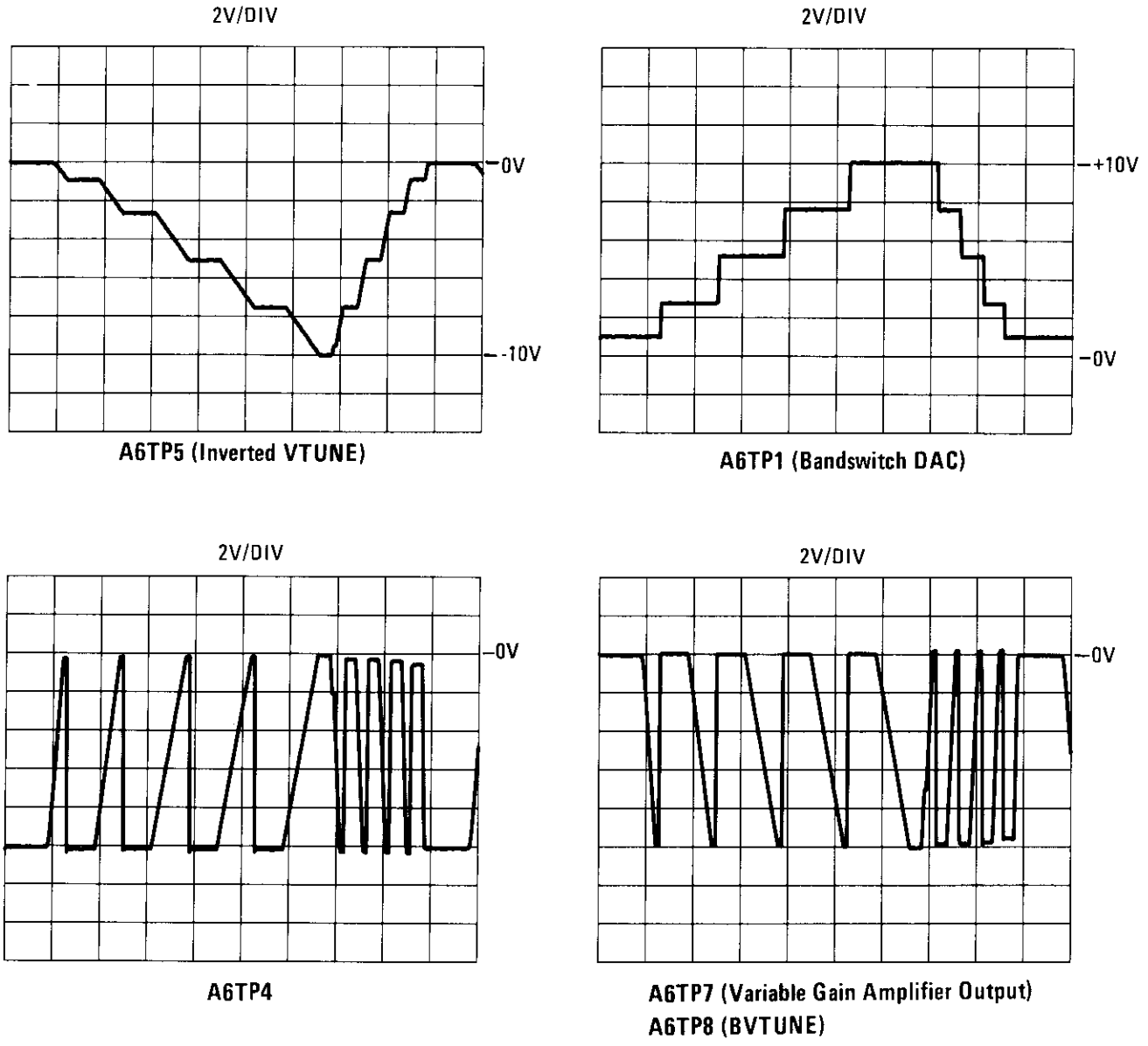


Figure 8-44. Buffered Tuning Voltage Waveforms

INTERRUPT CONTROL

Symptoms of an interrupt failure may include loss of sweep, portions of the sweep trace missing, or failure to sweep across a bandswitch.

1. Verify operation of the bandswitch comparator by checking the FWD SWP BSW (U23 pin 7) and RTC BSW (U14 pin 7) waveforms as shown in Figure 8-45.

   a. If the FWD SWP BSW signal is not correct, check the bandswitch DAC output at TP1 and the TV buffer output at TP5 as shown in Figure 8-44.

   b. If the RTC BSW signal is incorrect, check the variable gain amplifier output at TP7. Also verify that the non-inverting input to U14 is about 0V during a sweep retrace.

2. With an oscilloscope, check the following edge-connector pins: P1-3 (L SIRQ), P1-1 (L RTS), and P1-23 (L SSRQ) The appropriate waveforms are shown in Figure 8-45.

   a. L RTS should go low at the end of each forward sweep. If it does not, trace the problem back through the plug-in interconnect to the HP 8350.

   b. L SIRQ should pulse low briefly for end-of-sweep interrupts. If these pulses are missing, but L RTS is present, suspect U2A, U8B, U16C, or control lines from U3.

   c. L SIRQ should also pulse low for bandswitch interrupts. If these pulses are missing, but FWD SWP BSW and RTC BSW show the proper waveforms, suspect U2C/D, U8A, U16C, or control lines from U3.

   d. If L SIRQ stays low, or the pulses are exceptionally wide, check U3 with the procedure outlined in paragraphs titled Digital Control. If U3 is functioning, the HP 8350 microprocessor probably did not receive the interrupt. Trace this signal back to the HP 8350.

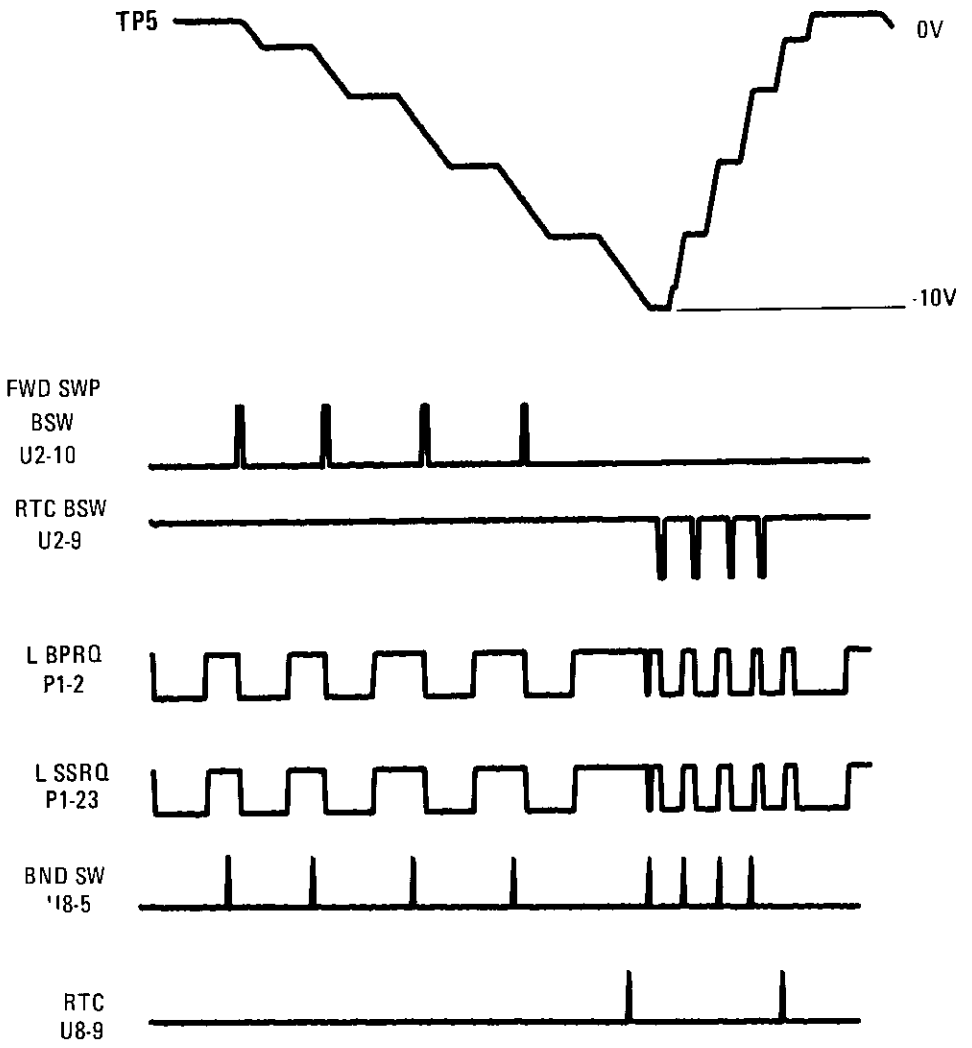


Figure 8-45. Sweep Control/Interrupt Logic Waveform

DIGITAL CONTROL

The address decoder and the data latches and output data buffer comprise the digital control for the A6 assembly. A failure in these components usually results in large frequency errors, and will often disable the bandswitch circuitry.

To check the address decoding circuitry enter **[SHIFT] [5] [4]** and perform the following:

1. Examine L INST1 (P1-18) for activity. If none is found, troubleshoot the A3 assembly.
2. If L INST1 is functional, check each of the LENn lines (U17) for the pulses shown in Figure 8-46. If these are incorrect, but the address lines show activity, replace U17. If the address lines seem locked high or low, troubleshoot the address buffer on the A3 assembly.

3. To check output buffer U13, press **[INSTR PRESET]**. Set the HP 8350 for a 5-second sweep rate and make the following key entry:

Press **[SHIFT] [0] [0]**	hex data mode
[2] [GHz] [0] [2]	address location 2C02 (U13)
[M3]	hex data read

The hex digits displayed in the HP 8350 front panel FREQUENCY/TIME window should change as the status read by U13 changes between forward sweep and retrace. Raising the power level until the UNLEVELED light comes on should also change the status bit being read by U13.

4. Exercise U3 and U9 with hex data rotation write. Enter:

Press **[SHIFT] [0] [0]**	hex data mode
[2] [GHz] [0] [0]	address location 2C00 (U3)
[M4]	hex data rotation write

Check the outputs of U3 against the waveforms shown in Figure 8-2. Verify operation of U9 by substituting hex address 2C01 (U9) in the procedure above.

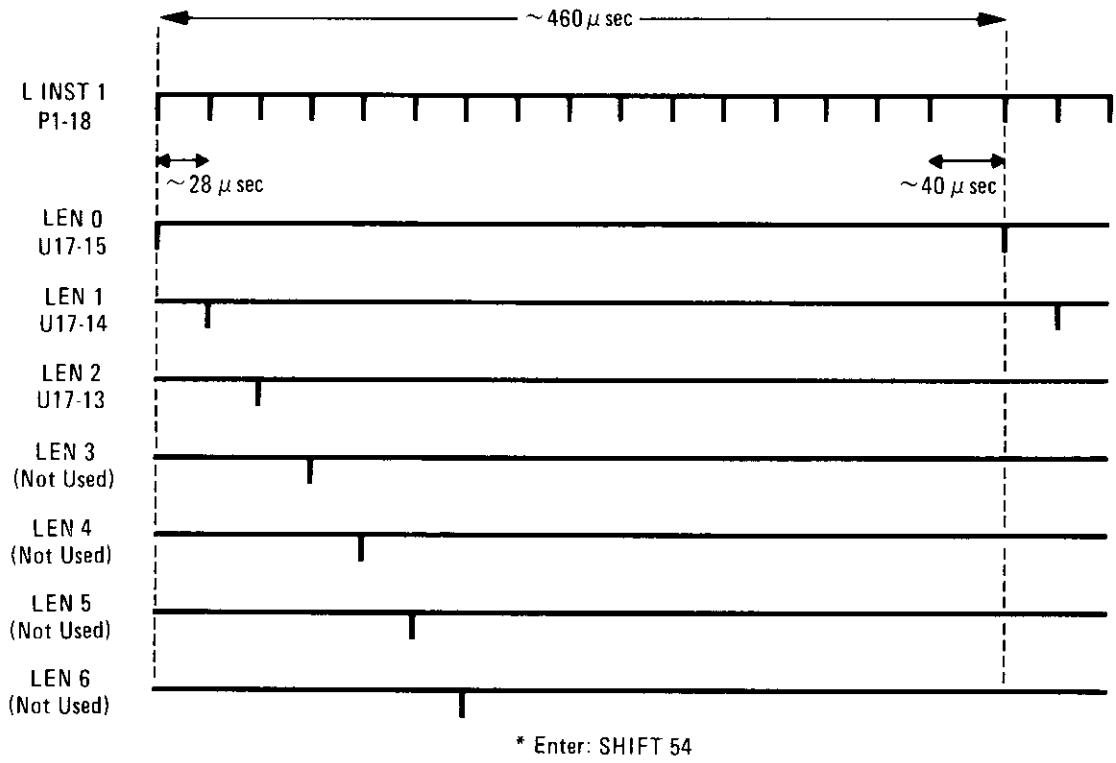


Figure 8-46. A6 Address Decoder Timing Diagrams

SRD AND PIN DIODE BIAS

A failure in the PIN diode bias circuit is indicated by a decrease or complete loss of RF output power for band 0 or bands 1 through 4. Check that the voltage at TP6 is +10V for band 0, and −4.8V for bands 1 through 4.

A failure in the SRD bias circuit is usually indicated by low RF output power in bands 1 through 4. Check the voltage at TP3 is +5V for band 0 and −5V for band 1. If these voltages are correct, perform the SRD bias adjustment in Section 5.

PULSE MODULATION

The pulse modulation circuit can be checked by entering an amplitude marker on the HP 8350 and checking for activity on the L PULSE and PULSE MOD outputs. If L PULSE has activity, but PULSE MOD does not, disconnect W6 at A16J4 to eliminate the possibility of the modulator loading down the signal.

A6 Sweep Control, Circuit Description

GENERAL

The sweep control assembly buffers and scales the VTUNE (tuning voltage) from the HP 8350 mainframe for use by the A7 SYTM and A8 YO driver assemblies. The A6 assembly also controls each bandswitch sequence. The SRD (step recovery diode) and PIN (positive-intrinsic-negative) diode bias circuit provides optimum biasing of the SYTM SRD for the frequency band selected and also biases the SYTM PIN diode switch to select the SYTM RF input for band 0 or bands 1 through 4. The pulse modulation circuit provides a drive current (PULSE MOD) to pulse modulate the RF output power. This modulation is initiated by the rear panel PULSE IN input or the amplitude marker from the HP 8350 mainframe.

ADDRESS DECODER, BLOCK A

The A6 sweep control uses hexadecimal address locations 2C00 through 2C0B. L INST1, BA0, BA1, and the L DAC EN output of U8D are decoded by the bandswitch DAC as hexadecimal addresses 2C08 through 2C0B. U17 is a 3-to-8 decoder that is enabled when L INST1 and address line BA3 are both low. U17 decodes address lines BA0 through BA2.

DATA LATCHES AND OUTPUT DATA BUFFER, BLOCK D

Two octal latches (U3 and U9) store various signals including the digital data for controlling the bandswitch comparator and sweep control/interrupt logic circuits. Each latch is clocked by a separate line from the address decoder to store the byte of data appearing on the data bus. The data is latched into U3 and U9 when their respective LEN clock inputs pulse low. Refer to the various circuit function blocks for detailed descriptions of these control lines.

Output buffer U13 outputs data to the HP 8350 microprocessor that relates to the current status of the sweep. Data is output when the LEN2 clock input to U13 is pulsed low.

TUNING VOLTAGE BUFFER AMPLIFIER, BLOCK B

U6 receives the tuning voltage from the HP 8350 mainframe and buffers it for use on the rest of the assembly. The circuit is arranged as a differential amplifier, with the tuning signal appearing at the inverting input and the cable shield at the non-inverting terminal. This provides good common mode rejection to eliminate noise picked up on the cable. The waveform at TP5 is an inverted ramp, ranging from 0 to −10V for single band sweeps (band 0, 1, 2, 3, or 4), or for sweeping the full frequency range of the plug-in. However, if the configuration switch (A3S1) in the A3 digital interface is selected for sequential sweep mode only, the tuning voltage (VTUNE) is not rescaled to a 0 to +10V ramp for single band sweeps. Figure 8-44 shows the tuning voltage waveform for a 0.01 to 26.5 GHz sweep.

BANDSWITCH DAC, BLOCK C

Bandswitch DAC U18 provides an offset voltage at TP1 that is proportional to the next bandswitch point. This voltage is used as a reference voltage by the bandswitch comparator for initiating the next bandswitch sequence. This voltage is also summed with the output of the TV buffer in the variable gain amplifier.

U18 is a 12-bit multiplying DAC which scales a stable −10V REF voltage according to the binary pattern loaded at its inputs. Inverting amplifier U19 works with the DAC's internal feedback resistor to provide a programmable offset voltage between 0 and +10V at TP1. CR2 protects the DAC from turn-on transients. C20 and the DAC's internal feedback resistor determine the bandwidth of the circuit.

For single band sweeps, the DAC is held in a reset condition by a logic low on the SEQ BAND input. This causes the voltage at TP1 to be held at 0 volts.

VARIABLE GAIN AMPLIFIER, BLOCK E

The purpose of the variable gain amplifier is to scale the tuning voltage input into a series of 0 to −10V ramps, with each ramp corresponding to a frequency band (band 0, 1, 2, 3, or 4). The bandswitch DAC output is summed in as an offset voltage to set the amplifier output to 0V at the beginning of each band. Amplifier gain is changed by analog switch U4 selecting a different feedback resistor for each band. Potentiometers B0 through B4 set the amplifier gain for each band. Analog switch U10D shorts across the feedback resistors for single band sweeps to disable the amplifier.

Figure 8-44 shows the relationship between the TV buffer output, bandswitch DAC output and the resultant variable gain amplifier output for a 0.01 to 26.5 GHz sweep.

SINGLE BAND SWITCHING, BLOCK G

The single band switching circuit selects between the variable gain amplifier output and the TV buffer output to provide BVTUNE (buffered tune voltage) to the YO and SYTM driver assemblies. The SEQ BAND (sequential band) input to analog switch U10B determines which input is used for BVTUNE. When the RF plug-in is sweeping a single band only, SEQ BAND is a logic low, and the TV buffer output is selected. When the RF plug-in is in a multiband sweep or the configuration switch on A3 is set for sequential sweep mode only, SEQ BAND is a logic high, and the output of the variable gain amplifier is selected. U20 is a non-inverting voltage follower.

BANDSWITCH COMPARATOR, BLOCK F

The bandswitch comparator circuit generates a FWD SWP BSW output to initiate each bandswitch during forward sweeps, and RTC BSW to generate each bandswitch during a sweep retrace.

A bandswitch point during a forward sweep is initiated by comparator U23. The buffered tuning voltage (TP5) appears at the inverting input of comparator U23. When the tuning voltage reaches a bandswitch point (as determined by the reference voltage applied to the non-inverting input of U23), the output of U23 changes. R42 provides hysteresis feedback to U23. If the selected frequency sweep does not require changing bands, switch U11D is opened, and R36 pulls the input to the comparator to +10V disabling the bandswitch circuitry. The reference voltage for comparator U23 (TP2) is supplied by the bandswitch DAC through operational amplifier U24A. This reference voltage is set during retrace or a bandswitch point to correspond to the next bandswitch point. The SP adjustment provides an offset to set accurate bandswitch points. During a sweep retrace, L RTS goes low to turn off Q7. This places a positve offset voltage at the inverting input of U24A and effectively disables comparator U23 during sweep retrace by offsetting the reference voltage beyond any bandswitch points generated by retrace comparator U14. FET Q1 is turned on when band 3 is selected; this grounds the comparator output to disable a bandswitch at the end of a sweep.

Retrace comparator U14 initiates a bandswitch during a sweep retrace each time the variable gain amplifier output (TP7) equals 0V. During sweep retrace, the L RTS input (inverted by U22A) turns on FET Q3 to set a 0V reference at the non-inverting input of comparator U14. The inverting input comes from the variable gain amplifier. Each time the amplifier output reaches 0V, comparator U14 outputs a logic high to initiate a bandswitch. During a forward sweep, FET Q3 is turned off, and a positive offset voltage is applied through R56 and R57. This offsets the reference input beyond any bandswitch points generated by the forward sweep bandswitch comparator (U23). When band 0 is selected, Q2 is turned on to disable comparator U14 from initiating a bandswitch at the end of a sweep retrace.

NOTE: Most of the signals discussed in this section are illustrated in Figure 8-45.

SWEEP CONTROL/INTERRUPT LOGIC, BLOCK H

The sweep control/interrupt logic circuit provides the stop sweep (L SSRQ), blanking request (L BPRQ) and sweep interrupt (L SIRQ) signals at bandswitch points. End of sweep interrupt circuitry (U8B) provides requests for interrupts at the beginning or end of sweep.

Whenever the bandswitch comparator outputs an active FWD SWP BSW or RTC BSW the output of U2C goes high. Pin 13 of U2D is prevented from tracking pin 12 by C16. Consequently, the output of the EXOR, U2D, will go high everytime U2C changes states. Each pulse from U2D clocks flip-flop U8A.

The high output at U8A performs three functions:

1. U16B issues a L SSRQ (Low=stop sweep request) to halt the sweep ramp generator in the HP 8350 mainframe
2. U16A issues a L BPRQ (Low=blanking pulse request) for display blanking during bandswitching
3. U16C issues a L SIRQ (Low=sweep interrupt request) to alert the HP 8350 microprocessor that a bandswitch needs to be made.

The microprocessor now takes over control of the bandswitch by writing command bits to data latch U3. First, the SSHOLD (stop sweep hold) line goes high, maintaining the stop sweep (L SSRQ) and blanking (L BPRQ) requests. Simultaneously, the L SSRES (Low=stop sweep reset) line goes low, resetting U8A and clearing the interrupt request (L SIRQ). The microprocessor now reads buffer U13 to determine what caused the sweep interrupt request (forward sweep bandswitch, retrace bandswitch, start or end of retrace, or the unleveled indicator turned on). Based on this information, the microprocessor blanks the RF power (when L RFBRQ goes low), updates the DACs, change the variable gain amplifier gain, changes various band-dependent control lines, and readies the plug-in for sweeping the new band. After the YO has settled, the RF power is turned back on. After the RF power has come up, the sweep is resumed and the display is unblanked by releasing the SSHOLD line. The time intervals required for YO settling and RF power-up are provided by the programmable counter on the A3 digital interface assembly.

In addition to bandswitch points, the microprocessor is also interrupted at the beginning and end of each sweep. Each time L RTS (Low=retrace strobe) changes from high to low, or low to high, U2A pulses high. (Pin 2 of U2A is prevented from tracking pin 1 by C17. Consequently, the output of EXOR U2A will pulse high everytime L RTS changes states). Each pulse from U2A clocks flip-flop U8B. The non-inverting output of U8B is ORed together with the bandswitch interrupt to pull L SIRQ low and request microprocessor attention. L RTS is read through U13 to determine whether the forward sweep is beginning (L RTS=high) or ending (L RTS=low). U8B is then reset by L ES RES, and the microprocessor services the interrupt.

L RFBRQ goes low during bandswitch and sends an RF blank request to the HP 8350 to produce the blanking signal L RFB for the A4 ALC assembly.

SRD AND PIN DIODE BIAS, BLOCK I

The SRD and PIN diode bias circuit provides two bias voltages for the switched YTM. The PIN SW output biases the PIN diode in the SYTM to select either the band 0 RF or the bands 1 through 4 RF as the input to the SYTM. In band 0, analog switch U11C is opened to apply positive bias to the diode and enable band 0. For bands 1 through 4, analog switch U11C is closed, and a negative bias is applied to the diode, enabling bands 1 through 4.

The step recovery diode in the SYTM is biased by SRD BIAS. This bias is optimized for each band and changes in power level. Voltage follower/subtractor U24 provides a voltage for optimum biasing of the SRD for each frequency band. BVTUNE is applied to both inverting and non-inverting inputs. If only BVTUNE was applied (and both inputs have the same gain) the U24 output would always be zero volts. Analog switches U11A and U11B sum in offset voltages for band 1 resulting in a large negative bias to ensure maximum feedthrough of the fundamental oscillator frequency. Analog switches U1D, U1B and U1C provide an offset and affect the non-inverting input gain. As a result, the U24 output for bands 2 through 4 is offset from 0V (as determined by the two band "L" adjustments) with the slope determined by the two band "H" adjustments.

U26 is a variable gain differential amplifier that provides an output current for bands 2, 3 and 4 for controlling the SRD BIAS. The amplifier gain is determined by the U24 output applied through analog switch U1A through Q10 to U26 pin 5. Analog switch U1A is open for band 1, so the SRD BIAS for this band is determined only by the output of U24. Threshold adjustment A6R78 (T) determines at what modulator drive voltage (MOD 1) that power level compensation is provided. CR12 prevents U26 from affecting SRD BIAS when MOD 1 is more positive than the threshold voltage set by R78 (T).

PULSE MODULATION, BLOCK J

The pulse modulation circuit provides a PULSE MOD output to the A16 modulator/splitter that is used to pulse modulate the RF output. The L PULSE output is used on the A4 ALC assembly in a sample and hold circuit to maintain a leveled power condition (refer to the A4 circuit description for more details). The L PULSE output goes active low when either the L RFM (Low= RF marker from the HP 8350) or PULSE IN (from the rear panel PULSE IN connector) go low. If the PULSE IN input from the rear panel exceeds a TTL level, it is translated to a TTL level by the resistor diode network on the U21A pin 13 input. When the L PULSE output is active low (switching RF power off), Q4 is biased on and Q6 is biased off; this provides a positive bias to the PIN diode in the modulator and attenuates the RF output power. When L PULSE is a logic high, Q6 is biased on and Q4 is biased off; this provides a negative bias to the PIN diode in the modulator so that it has no effect on the RF power level.

Table 8-19. A6P1 Pin-Outs

A6P1

PIN	SIGNAL	I/O	TO/FROM	FUNCTION
1 23	LRTS LSSRQ	IN OUT	P2-57 A7P1-5, A8P1-5, P2-32	D,F,H H
2 24	LBPRQ LRFBRQ	OUT OUT	P2-55 P2-54	H H
3 25	LSIRQ L PULSE	OUT OUT	A3P1-18 A4P1-41	H J
4 26	L UNLVL PULSE IN	IN IN	A4P1-2 J5	D,H J
5 27	PWON +5V	IN IN	P2-25 A3P1-6,7	D K
6 28	MOD 1 −15V	IN IN	A4P1-19 P2-28	I K
7 29	+10V PIN SW	IN OUT	P1-8 A10J4-15	K I
8 30	DIG GND DIG GND	IN IN		K K
9 31	BD1 BD0	I/O I/O	A3P1-9 A3P1-31	C,D C,D
10 32	BD3 BD2	I/O I/O	A3P1-10 A3P1-32	C,D C,D
11 33	BA1 BA0	IN IN	A3P1-11 A3P1-33	A,D A,D
12 34	BA3 BA2	IN IN	A3P1-12 A3P1-34	A A
13 35	BD5 BD4	I/O I/O	A3P1-13 A3P1-35	D D
14 36	BD7 BD6	I/O I/O	A3P1-14 A3P1-36	D D
15 37	LBP2 GND ANLG	IN	A3P1-44	H K
16 38	UNL LMP EN +15V	IN IN	A2J1-4 P2-29	H K
17 39	−10V −10V REF	IN IN	P1-13 A8P1-3	K C
18 40	LINST 1 L RFM	IN IN	A3P1-8 P2-24	A J
19 41	BAND0 AMP GND ANLG	OUT	A10J5-7	D K
20 42	VTUNE BVTUNE	IN OUT	P1-A1 A7P1-25, A8P1-25	B G
21 43	VTUNE RET GND ANLG	IN	P1-A1	B K
22 44	SRD BIAS PULSE MOD	OUT OUT	A10J4-14 A10-E8	I J

Troubleshooting the A7 SYTM Driver/A9 Reference Resistor Assemblies

NOTE: All reference designators refer to the A7 assembly, unless otherwise noted.

INTRODUCTION

The A7 SYTM driver and A9 reference resistor assemblies are primarily responsible for controlling the SYTM bandpass frequency. A failure in these assemblies usually results in a low RF power output. (Power losses that change with sweep time are usually related to delay compensation.) Power losses that may be corrected with the front panel PEAK control may be due to improper calibration. The problem may be relieved by performing the frequency accuracy adjustment in Section 5.

GENERAL

Check that all power supply voltages are present. +20V (on the A7 assembly) and −40V (on the A12A1 assembly) supply the SYTM. Ensure that cable plugs are correctly seated over the correct jacks throughout the plug-in. With the line power off, remove and reseat the A7 assembly to assure good motherboard contact.

NOTE: Unless specifically stated otherwise, the troubleshooting waveforms and voltages described below occur when the plug-in is sweeping across its full range (INSTR PRESET conditions).

SWEEP CIRCUITRY

A failure in the sweep circuitry may cause the SYTM to tune between improper frequency endpoints, or not sweep at all. If the SYTM drive voltage is incorrect or missing, the instrument will have low RF output power for bands 1 through 4.

1. Check the SYTM DRIVE V (TP6) for the waveform shown in Figure 8-50. If this waveform is correct, troubleshooting should continue with the SYTM current driver section below.

   a. If SYTM DRIVE V is incorrect, check BVTUNE (A6TP8) for a series of 0 to −10V ramps. If they are missing or of the wrong amplitude, refer to the A6 sweep control service sheet for further troubleshooting.

   b. If the waveform at TP6 appeared to be level-shifted, check −10V REF (A8TP12) for exactly −10 VDC. Next, with the plug-in sweeping its entire range, check TP1 for the waveform in Figure 8-51. If this signal is incorrect, select a CW frequency of 20.0 GHz and press **[SHIFT] [5] [2]** to test DAC U13. Check TP1 for the waveform shown in Figure 8-52. If this test fails, check address decoding using the digital control troubleshooting procedure described below.

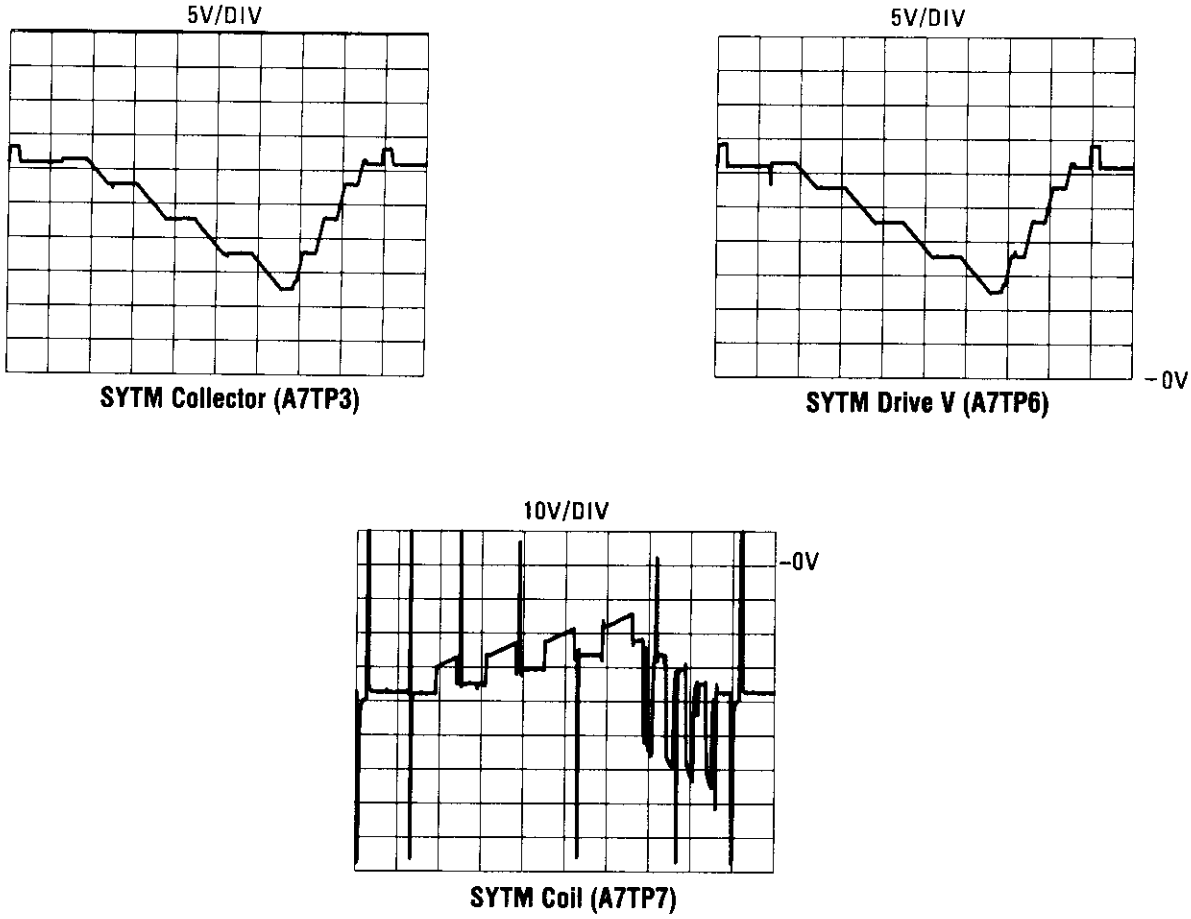


Figure 8-50. SYTM Coil Current Source Waveforms

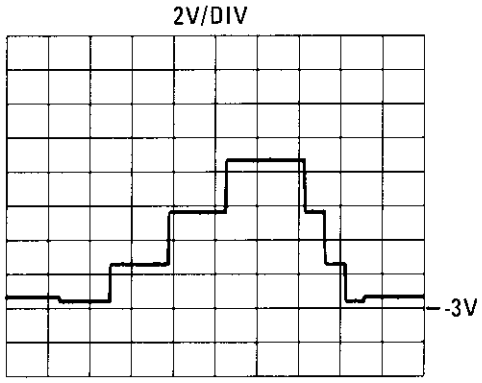
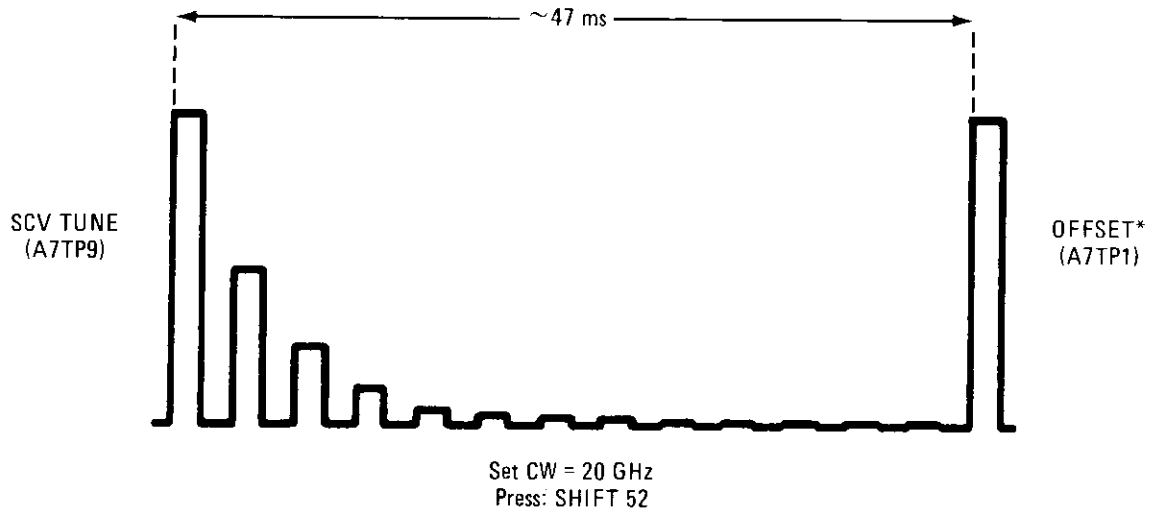


Figure 8-51. Offset Voltage (A7TP1)

2. If BVTUNE is correct, check SCVTUNE (TP9) against the waveform shown in Figure 8-53. If it appears to be bad, run the scale DAC test by setting a CW frequency of 20.0 GHz and pressing **[SHIFT] [5] [2]**. Check that U17 pin 15 is at −10 VDC. Then check TP9 for the waveform shown in Figure 8-52. If U17 fails, check address decoding using the digital control troubleshooting below.

3. Check +20V FREQ REF (TP8) for +20 VDC ±10 mV. If it is not, trace the supply voltage back to the HP 8350. Then check that SUPPLY VOLTAGE CORRECTION (U15 pin 6) is at approximately −10 VDC. If it is not, troubleshoot U15.

4. Finally, check that the summing junction, U21 pin 2, is at 0 VDC. If it is not, troubleshoot U21.



*Waveform at TP1 will have slightly rounded edges due to larger feedback capacitor.

Figure 8-52. DAC Test

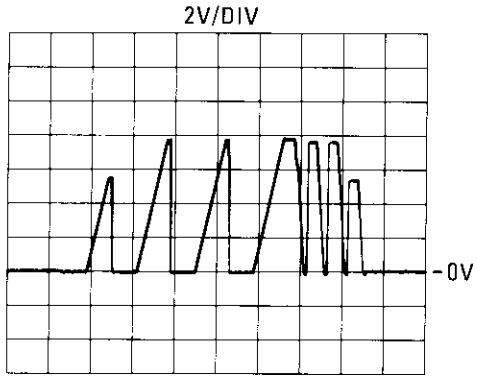


Figure 8-53. Scaled Tuning Voltage (A7TP9)

DELAY COMPENSATION

A failure in the delay compensation circuit is usually indicated by RF output power variations that change with sweep time. The delay compensation has little effect at sweep times greater than 100 milliseconds. On the HP 8350 enter **[INSTR PRESET]** and check waveforms in Figure 8-54.

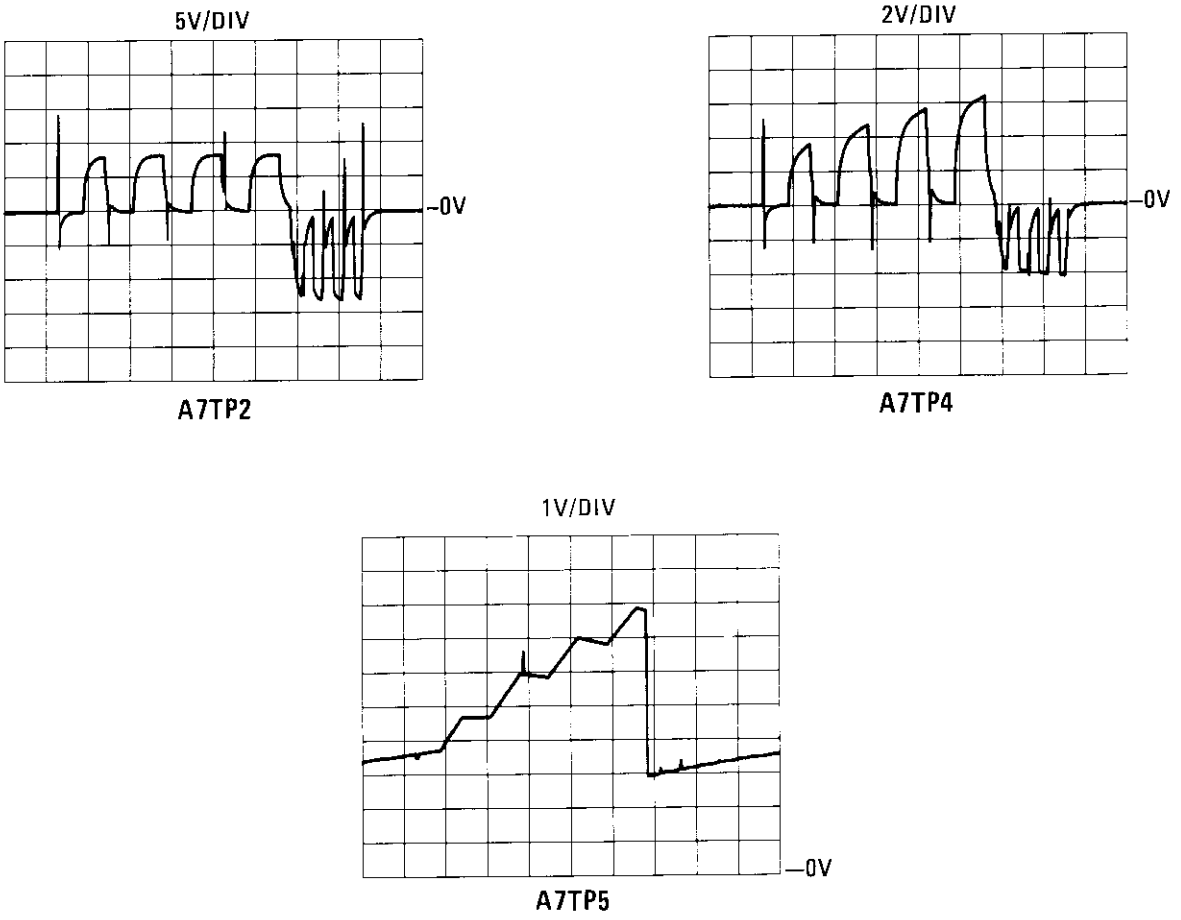


Figure 8-54. SYTM Delay Compensation Waveforms

SYTM DRIVE CIRCUITS

1. Check +20V FREQ REF at TP8 for +20V ±10 mV. If it is not, troubleshoot back to the mainframe supply.

The circuitry surrounding U22 and A9Q2 is responsible for converting the SYTM DRIVE V to a drive current for the SYTM coil. A failure here will usually result in extreme RF power losses for bands 1 through 4.

2. Press **[INSTR PRESET]** to sweep the entire range of the plug-in. Check TP7 for the waveform shown in Figure 8-50. This represents the voltage (not the current) across the SYTM's main coil, and will give an indication as to whether current is passing through the coil. If this waveform is correct, suspect the A12 SYTM or the SRD bias circuit on the A6 sweep control assembly. Refer to the RF section troubleshooting information.

3. Check TP3. This voltage should track the SYTM DRIVE V (Figure 8-50). If it does not, troubleshoot U22, Q1, Q2, chassis mounted R2, and A9Q2.

    a. Chassis-mounted R2 should be checked by removing the A9 assembly from the instrument. The ohmmeter reading should be approximately 59 ohms.

    b. While the A9 assembly is removed from the instrument, check the collector-base and base-emitter junctions of A9Q2 with an ohmmeter. These junctions should show only a few hundred ohms when forward biased, and a high impedance in the reverse direction. If A9Q2 is found to be shorted or opened, make sure that protection diodes VR1 and CR5 are good before replacing the transistor.

    c. Q1 and Q2 can be checked, using the procedure above, while they are still in the circuit. The line power should be off.

    d. If the above checks find that the components are good, replace U22.

DIGITAL CONTROL

The address decoder and data latch, and frequency cal switches comprise the digital control for the A7 assembly. A failure in these components usually results in large power losses for bands 1 through 4, and will often cause an unleveled power condition.

To check the address decoding circuitry enter **[SHIFT] [5] [4]** and perform the following:

1. Examine L INST2 (P1-18) for activity. If none is found, troubleshoot the A3 assembly.

2. If L INST2 is functional, check each of the LENn lines (U16) for the pulses shown in Figure 8-55. If these are incorrect, but the address lines show activity, replace U16. If the address lines seem locked high or low, troubleshoot the address buffer on the A3 assembly.

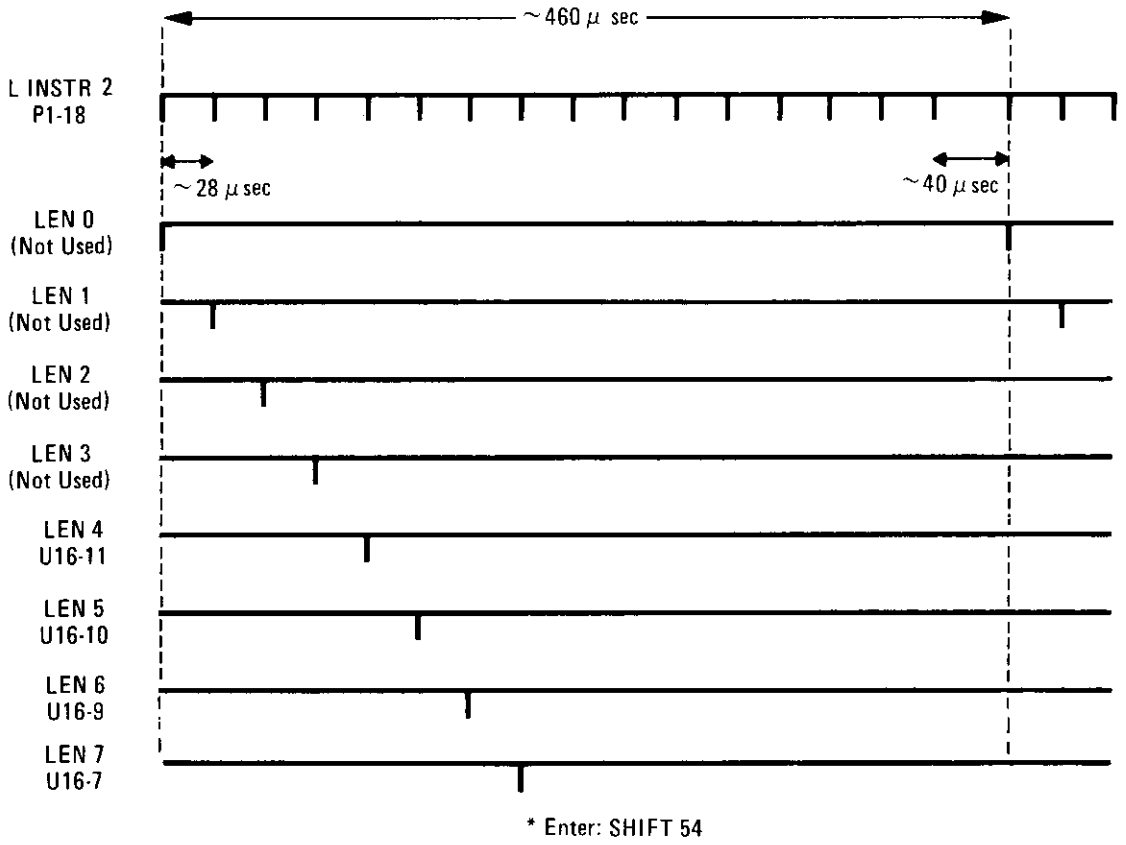


Figure 8-55. A7 Address Decoder Timing Diagram

NOTE: U3, U4, and U7 are checked by reading data while changing switch settings. Before altering the switch settings on A7S1 and A7S2, write down the present configuration. Return the switches to their original status after troubleshooting. If this is not done, the frequency endpoints will have to be recalibrated.

3. To check output buffer U7, press **[INSTR PRESET]**, and make the following key entry:

Press **[SHIFT] [0] [0]**	hex data mode
[2] [GHz] [8] [dBm]	address location 2C8E (U7)
[M3]	hex data read

The hex digits displayed in the HP 8350 front panel FREQUENCY/TIME window should change when the S1 and S2 switch positions 8 and 9 are toggled.

4. U3 and U4 can each be checked with hex data read (see above) at address 2C8C or 2C8D. The hex digits should change when the corresponding freq cal switches are changed.

5. Exercise U12 with hex data rotation write. Enter:

Press **[SHIFT] [0] [0]**	hex data mode
[2] [GHz] [8] [BKSP]	address location 2C8F (U12)
[M4]	hex data rotation write

Check the outputs of U12 against the waveforms shown in Figure 8-2.

A7 SYTM Driver/A9 Reference Resistor, Circuit Description

NOTE: All reference designators refer to the A7 assembly unless otherwise noted.

GENERAL

The A7 SYTM driver assembly converts the buffered tuning voltage from the A6 sweep control assembly into a drive current. The A9 reference resistor assembly provides the current driver to control the frequency of the SYTM.

Multiplying digital-to-analog converters (DACs) scale and offset the buffered tuning voltage to the frequency end-points in each band. Delay compensation is generated and summed with the tuning voltage. Also summed with the tuning voltage are low frequency external FM, and a band 1 offset. The resultant waveform at TP6 is then converted to a current-drive for the SYTM's main coil.

ADDRESS DECODER AND DATA LATCH, BLOCK A

The A7 SYTM driver uses hexadecimal address locations 2C8C through 2C8F, decoded by U16 from signals BA0, BA1, and BA2. U16 is a 3-to-8 decoder that is enabled when L INST2 is active low and address line BA3 is active high. L INST2, BA0, BA1, and the L DAC EN output of U8C are used by the scaled voltage tune and offset DACs.

U12 is a control latch which stores commands from the HP 8350 for the control lines used on the A7 SYTM driver assembly, primarily for delay compensation. The command byte is latched into U12 when LEN 7 pulses low. Refer to the delay compensation, and summing amplifier sections for detailed descriptions of these control lines.

SCALED VOLTAGE TUNE DAC, BLOCK B
OFFSET DAC, BLOCK C

The scaled voltage tune and offset DACs function together to determine the bandpass frequency of the SYTM. The offset DAC determines the start frequency of each band while the scaling DAC scales the BVTUNE input to tune the SYTM over the required frequency range for each band.

U17 and U13 are 12-bit microprocessor compatible DACs, which latch data in three four-bit nibbles. These DACs share the same address locations, but are loaded by different data lines (D0 through D3 load U13 and D4 through D7 load U17).

BVTUNE is a series of 0 to −10V ramps with each ramp corresponding to a frequency band. DAC U17 scales each ramp differently according to the frequency range the SYTM must sweep to cover the frequency range of the band. (See SC VTUNE waveform at TP9 in Figure 8-53.) Since the SYTM is not used as a filter for band 0, the DAC output is set to 0V for band 0.

U17 scales the buffered tuning voltage (BVTUNE) according to the binary pattern loaded at its inputs. Inverting amplifier U18 is included in the feedback path to convert the current output of the DAC to a voltage. CR1 prevents transients from damaging the DAC during turn-on. C18, along with the DAC's internal feedback resistor, determine the bandwidth of the circuit. The waveform at TP9 is a scaled ramp (sawtooth waveform for multiband sweeps), with a maximum range of 0 to +10 VDC. See Figure 8-53.

U13 scales a stable −10V REF voltage according to the binary pattern loaded at its inputs. Inverting amplifier U14 works with the DAC's internal feedback resistor to provide a programmable offset voltage between 0 and +10 VDC at TP1. See Figure 8-51. CR7 protects the DAC from turn-on transients. C15 and the DAC's internal feedback resistor determine the bandwidth of the circuit.

DELAY COMPENSATION, BLOCK E

The delay compensation circuit is used to compensate the A12 SYTM for the inherent inaccuracy caused by delay in the magnets at fast sweeps. SC VTUNE (a scaled ramp from the scaled voltage tune DAC), OFFSET (an offset voltage that sets the start frequency of each band), and SYTM LO FM (a voltage proportional the low frequency FM applied to the HP 8350 rear panel FM INPUT) are summed by U19 to provide a voltage with a slope proportional to the change in SYTM frequency. This voltage ramp is sent to two separate signal processors:

1. A voltage follower/subtractor whose output is equal to zero at start of sweep and at the band switch points. The amplitude is proportional to sweep width.
2. A differentiator whose output is proportional to the rate of frequency change while sweeping. These two signals are then mulitiplied in the analog multiplier U20. The delay compensation is summed into the main coil driver voltage in the summing amplifier.

During retrace, and momentarily during bandswitching, analog switch U10B closes. In this condition, U11C together with R6, R8, R9, and R7 form a subtractor circuit. Both inputs are the input signal so they cancel in the operational amplifier and the resulting output is 0V, regardless of the input level. With U10B closed, C4 charges to one half the value of the input signal (R8 and R9 form a voltage divider). UI0B opens again during the sweep which leaves only C4 in the feedback path of U11C. Since there is no discharge path with U10B and U10A open, C4 remains charged to the level it had just before U10B was opened. U11C now operates as a voltage follower, with the output level shifted by the voltage across C4. Therefore, the output of U11C has one half the slope of the input signal and returns to 0V whenever U10B is closed during retrace and bandswitching. Two sets of scaling (HI) and offset (LO) adjustments on the output of U11C accurately scale and offset the voltage follower/subtractor output for both a single (SGL) and sequential band (SEQ) sweep. Analog switches U10D and U10C select the correct input for inverting amplifier U11D. The output generated at TP5 is one input to the analog multiplier

If the sweep is stopped momentarily, such as when an external counter is used, L SSRQ is pulled low by the HP 8350 mainframe. When U10A is closed by a low on the L SSRQ control line to U8A, C4 slowly recharges through R62. Thus when L SSRQ is pulled, the output of U11C will begin to go to zero volts, but may or may not reach zero volts depending on the length of time L SSRQ was pulled low. When L SSRQ goes high again and the sweep continues, U9A opens and U11C resumes its voltage follower operation.

The U19 summing amplifier output is also applied to a differentiator (U11B) with a time constant that is selected by analog switches U9A and U9B. By selecting either C6 (for sequential sweep) or C13 (for single band sweep) in parallel with C3, the U11B output is scaled for either single or multiband (sequential) sweeps. The output is amplified and inverted by U11A and is applied at TP2 to the second input of the analog multiplier. The output at TP4 is connected to U20 pin 7 to provide feedback for an operational amplifier internal to U20. The Z adjust at U20 pin 6 allows nulling of the offset voltage appearing at DLY COMP. This is done when in CF ΔF mode where ΔF equals zero.

During sweep retrace, the SYTM must change frequency rapidly from the high end of its range to the low end, and does not have enough time to naturally settle to the proper start frequency. Unless the SYTM is forced to the low end of its range, this could result in a frequency tracking error, and a resultant loss of output power, at the start of each sweep. In order to force the SYTM to settle quicker, C17 is charged during the SYTM retrace by the differentiator output through CR2. Timer U5 is triggered by L RTC COMP at the end of sweep retrace. The timer pulse output momentarily closes analog switch U9C, and C17 discharges through R57 and is applied as retrace compensation to the summing amplifier. This compensation voltage forces the SYTM to the low end of its range to avoid frequency tracking errors after a retrace. The amount of compensation applied is proportional to the pulse width of the timer output, and is adjusted by R55.

+20V TRACKING, BLOCK F

Inverting amplifier U15 monitors the +20V line used to supply current to the SYTM. If the +20V supply becomes loaded down or drifts, the SYTM main coil current and, consequently, the SYTM bandpass frequency will try to change. However, U15 senses any drift in the +20V FREQ REF line, and provides a correction signal so that the resultant SYTM DRIVE voltage (TP6) is compensated for the drift. ZRO adjustment R22 compensates for inaccuracies between U15 and summing amplifier U21.

SUMMING AMPLIFIER, BLOCK G

U21 provides the summing point for the scaled tuning and offset voltages, and provides a drive voltage (SYTM DRIVE V) for the current driver. Several correction signals are summed at this junction:

SC VTUNE provides the scaled ramp portion of the SYTM DRIVE voltage. R19, GAIN, fine-tunes the range of the scaling DAC.

OFFSET adjusts the SYTM DRIVE voltage so that the SYTM coil is driven between the proper end points, as determined by the front panel controls. R24, "OFS", fine-tunes the range of the offset DAC.

SUPPLY VOLTAGE CORRECTION provides a compensation signal, from the +20V tracking amplifier, to offset changes in the reference supply.

DLY COMP, from the delay compensation circuit, is added to correct for lags in the response time of the SYTM. This compensation is derived from SC VTUNE.

RTC COMP, from the delay compensation circuit, is a momentary correction voltage that forces the SYTM to the low end of its frequency range after a sweep retrace. This compensation is derived from SCVTUNE.

B1 OFS is summed in through U9D when the BAND 1 line from U12 is high.

SYTM LO FM sums low frequency components of external FM signals onto the drive voltage when crossover-coupling of the FM signal is selected. (Configuration switch A3S1 provides this adjustment. Refer to the A3 service section for further detail.) Due to the response time limitations of the YIG oscillator's main coil, only frequencies below 700 Hz are passed from the A5 FM driver assembly to the A7 SYTM assembly.

FREQUENCY CAL SWITCHES/OUTPUT DATA BUFFERS, BLOCK D

DIP (dual-inline package) switches S1 and S2, with their corresponding data bus buffers, are used to digitally calibrate the low and high end frequencies in band 2. The data on these switches is read by the microprocessor during power-up and INSTR PRESET and is used to calculate the settings for the scale and offset DACs. S1, with pull-up resistor package U1, is read through U3 when enabled by LEN4. S1 determines the value of the offset DAC and calibrates the low end frequency. S2, with pull-up resistor package U2, is read through U4 when enabled by LEN5. This establishes the scale DAC values, and calibrates the high end frequency. The ninth and tenth bits from S1 and S2 are read through U7.

S1 and S2 switch positions encode binary numbers to set up the offset and scaling DACs. Refer to the frequency accuracy adjustment procedure in Section 5 for instructions. Figure 8-56 illustrates the switch configurations.

SYTM COIL CURRENT SOURCE, BLOCK H
SYTM COIL CURRENT DRIVER A9, BLOCK I

The SYTM coil current driver works with the chassis-mounted reference resistor R2 and SYTM coil driver A9Q2 to drive a current proportional to the drive voltage through the SYTM's main tuning coil.

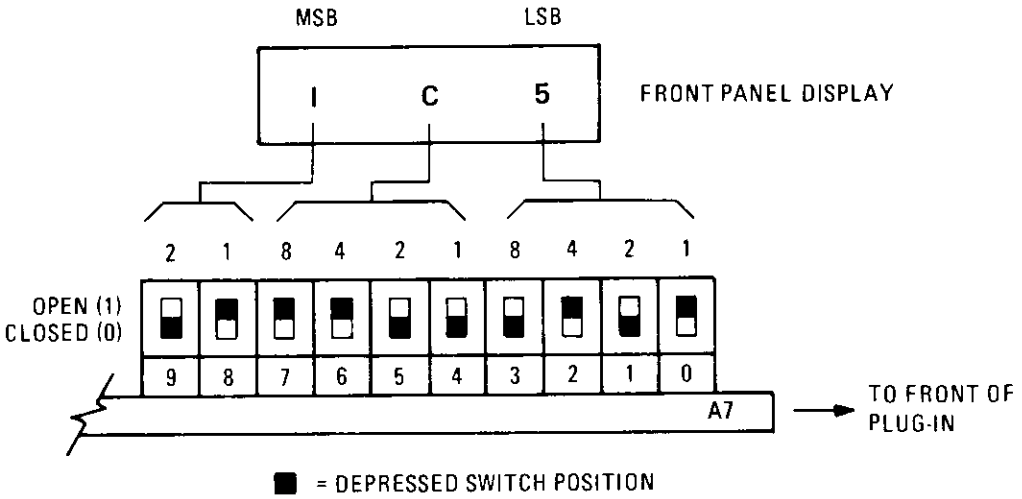
U22, Q1, Q2, and A9Q2 comprise a voltage-to-current converter and current driver for the SYTM's main coil. The non-inverting input of U22 receives the SYTM DRIVE voltage signal. The inverting input of U22 monitors the voltage drop across reference resistor R2, which is directly proportional to the coil current. If the drive current is not tracking the drive voltage, U22 will produce an error voltage to correct the difference. Emitter-follower Q2 and common-emitter-stage Q1 provide the current gain needed to drive A9Q2. Q2 and Q1 emitter currents are also drawn through chassis mounted R2, and therefore, sensed by U22. VR1 and CR5 protect the current drive transistors by limiting voltage spikes due to sudden changes in the coil current. R33 helps to dampen ringing caused by the parasitic capacitance and the inductance of the SYTM coil.

CR3, CR4, CR6, CR8, and their associated factory-select resistors provide a four break-point compensation network to correct for non-linearities in the SYTM characteristics.

NOTE: The values of the factory-select resistors are stamped on a label, attached to the RF casting. Matching resistor sets (mounted on a header) are supplied with replacement SYTMs and must be installed on the A7 SYTM assembly. The new label, indicating the replacement resistor values should be attached to the RF casting.

If the A7 SYTM driver assembly is replaced, the shaping resistors from the defective assembly (which are mounted on a header) must be reinstalled in the new assembly.

NOTE: If the SYTM needs little or no compensation, some or all of the factory-select resistors may be omitted.



Hexadecimal	Binary	Decimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
A	1010	10
b	1011	11
C	1100	12
d	1101	13
E	1110	14
F	1111	15

Figure 8-56. A7S1/S2 Switch Configuration

Table 8-20. A7P1 and A9P1 Pin-Outs

A7P1

PIN	SIGNAL	I/O	TO/FROM	FUNCTION
1 23	SYTM LO FM SYTM DRIVE V	IN OUT	A5P1-1 A10J1-39	E,G G
2 24	GND ANLG		NOT USED	J
3 25	−10VREF BVTUNE	IN IN	A8P1-5 A6P1-42	C B
4 26	GND ANLG		NOT USED	J
5 27	L SSRQ +5V	IN IN	A6P1-23 A3P1-6,7	E J
6 28	−40V −15V	IN IN	P1-11 P2-28	J J
7 29	+10V GND ANLG	IN	P1-8	J
8 30	GND DIG GND DIG			J J
9 31	BD1 BD0	I/O I/O	A3P1-9 A3P1-31	A,C,D A,C,D
10 32	BD3 BD2	I/O I/O	A3P1-10 A3P1-32	A,C,D A,C,D
11 33	BA1 BA0	IN IN	A3P1-11 A3P1-33	A,B,C A,B,C
12 34	BA3 BA2	IN IN	A3P1-12 A3P1-34	A A
13 35	BD5 BD4	I/O I/O	A3P1-13 A3P1-35	A,B,D A,B,D
14 36	BD7 BD6	I/O I/O	A3P1-14 A3P1-36	B,D B,D
15 37	GND ANLG GND ANLG			J J
16 38	+20V +15V	IN IN	P1-7 P2-29	J J
17 39	−10V −40V	IN IN	P1-13 P1-11	J J
18 40	LINST 2	IN	A3P1-29 NOT USED	A
19 41	GND ANLG		NOT USED	J
20 42	SYTM COLLECTOR		A9P1-10 NOT USED	H
21 43	SYTM BASE	OUT	A9P1-9 NOT USED	H
22 44	SYTM COIL +20V FREQ REF	IN	A9P1-8 A9P1-15	H H

Table 8-20b. A7P1 and A9P1 Pin-Outs

A9P1

PIN	SIGNAL	I/O	TO/FROM	FUNCTION
1 7	YO BASE +5V REG	IN OUT	A8P1-21 A10J4-7,A10J5-3,11	
2 8	YO COLLECTOR SYTM COIL	OUT OUT	A8P1-1 A7P1-22,A10J4-8	I
3 9	+20V SYTM BASE	IN IN	P1-7 A7P1-21	I I
4 10	YO COIL SYTM COLLECTOR	OUT IN	A8P1-22 A7P1-20	 I
5 11	+20V FREQ REF +20V	OUT IN	A7P1-44,A8P1-44 P1-7	I I
6 12	GND ANLG +5V UNREG	 IN	P2-27,58-59 P2-63	I

Troubleshooting the A8 YO Driver/A9 Reference Resistor Assemblies

NOTE: All reference designators refer to the A8 assembly, unless otherwise noted.

INTRODUCTION

The A8 YO driver and A9 reference resistor assemblies are primarily responsible for controlling the RF output frequency. A failure in these assemblies usually results in large frequency errors that may, or may not, be independent of sweep time. (Frequency errors that change with sweep time are usually related to delay compensation.) Frequency errors on the order of 500 MHz or less may be due to improper calibration. The problem may be relieved by performing the frequency accuracy adjustment in Section 5.

GENERAL

Check that all power supply voltages are present. +20V (on the A8 assembly) and −40V (on the A13A1 assembly) supply the YO. Ensure that cable plugs are correctly seated over the correct jacks throughout the plug-in. With the line power off, remove and reseat the A8 assembly to assure good motherboard contact.

NOTE: Unless specifically stated otherwise, the troubleshooting waveforms and voltages described below occur when the plug-in is sweeping across its full range (INSTR PRESET conditions).

SWEEP CIRCUITRY

A failure in the sweep circuitry may cause the YIG to sweep between improper frequency endpoints, or not sweep at all. If the YO drive voltage is missing, the instrument may toggle between two or more CW frequencies.

1. Check the YO DRIVE V (TP10) for the waveform shown in Figure 8-61. If this waveform is correct, troubleshooting should continue with the YO current driver section below.

   a. If YO DRIVE V is incorrect, check BVTUNE (A6TP8) for a series of 0 to −10V ramps. If they are missing or of the wrong amplitude, refer to the A6 sweep control service sheet for further troubleshooting.

   b. If the waveform at TP10 appeared to be level-shifted, check −10V REF (TP12) for exactly −10 VDC. Next, with the plug-in sweeping its entire range, check OFFSET (TP3) for the waveform in Figure 8-62. If this signal is incorrect, select a CW frequency of 20.0 GHz and press **[SHIFT] [5] [2]**. Check TP3 for the waveform shown in Figure 8-63. If this fails, check address decoding and the DAC latches using the digital control troubleshooting procedure described below.

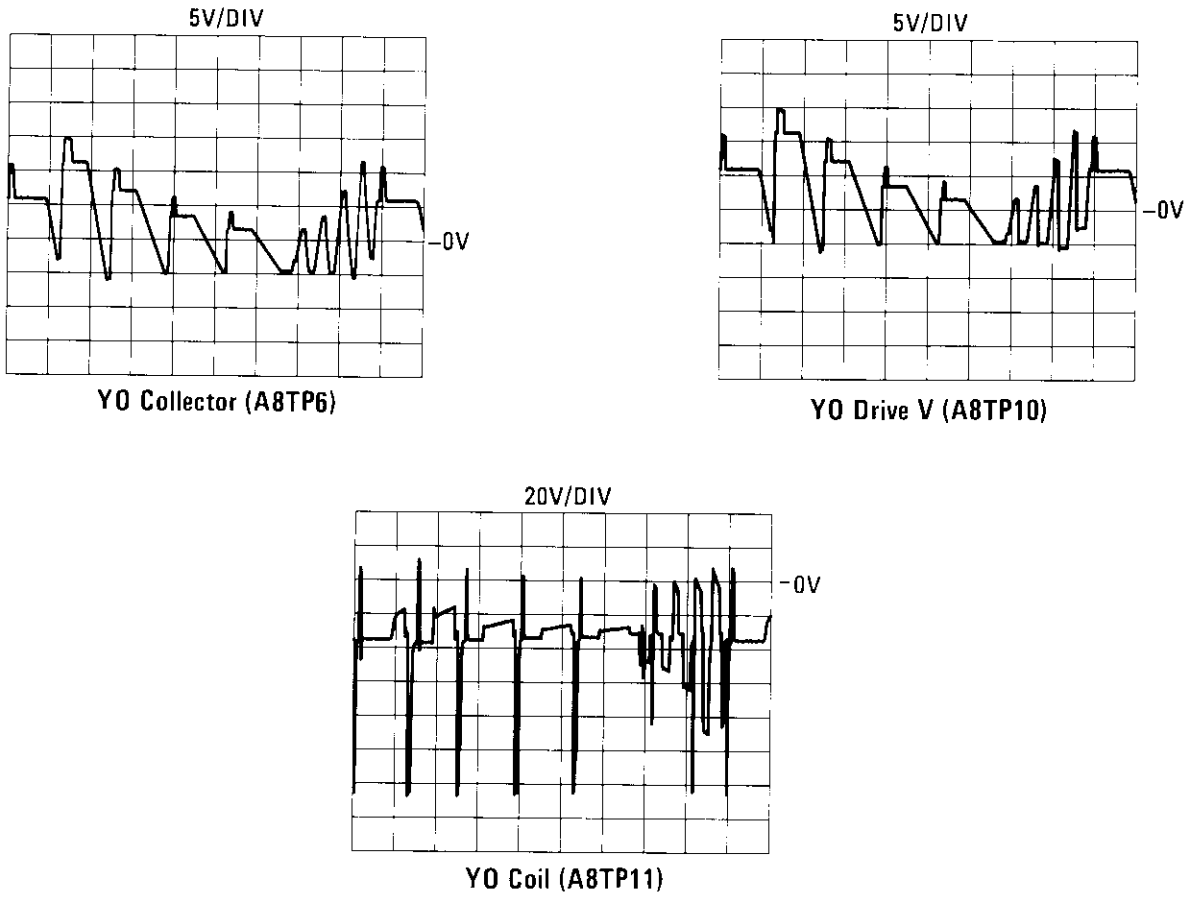


Figure 8-61. YO Coil Current Source Waveforms

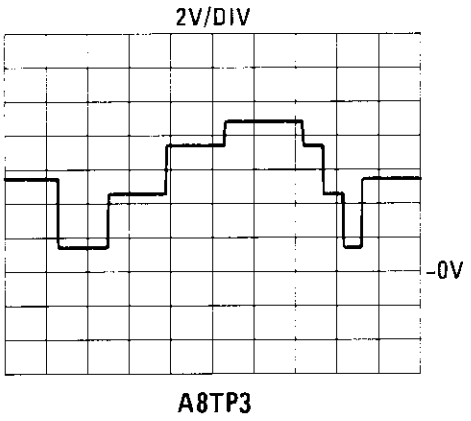


Figure 8-62. Offset Voltage (A8TP3)

2. If BVTUNE is correct, check SC VTUNE (TP2) against the waveform shown in Figure 8-64. If it appears to be bad, run the scale DAC test by setting a CW frequency of 20.0 GHz and pressing **[SHIFT] [5] [2]**. Check that U17 pin 15 is at −10 VDC. Then check TP2 for the waveform shown in Figure 8-63. If this fails, check address decoding using the digital control troubleshooting below.

3. Check +20V FREQ REF (A7TP12) for +20 VDC ±10 mV. If it is not, trace the supply voltage back to the HP 8350. Then check that SUPPLY VOLTAGE CORRECTION (U11 pin 6) is at approximately −7.5 VDC. If it is not, troubleshoot U11.

4. Finally, check that the summing junction, U20 pin 2, is at 0 VDC. If it is not, troubleshoot U20.

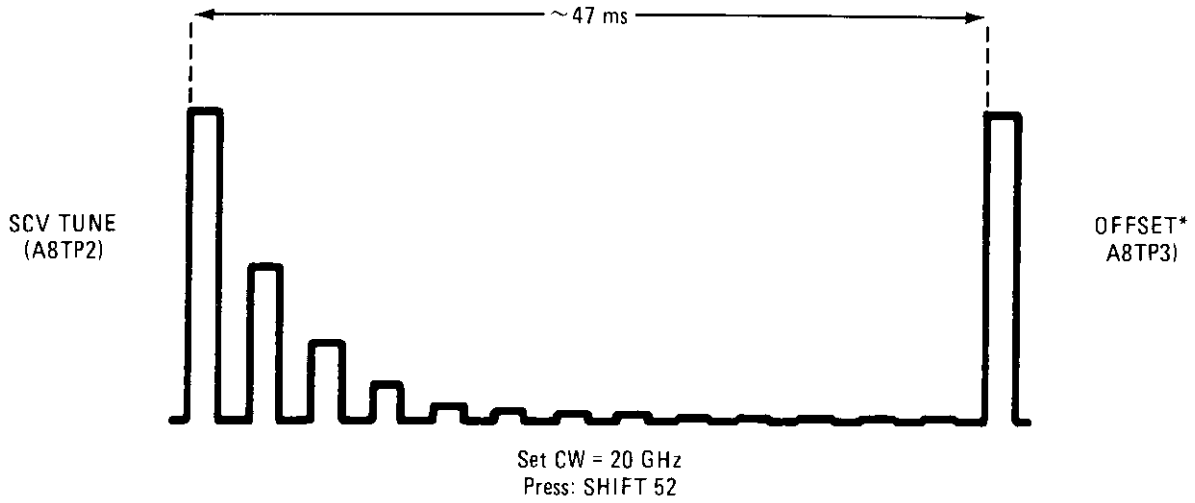


Figure 8-63. DAC Test

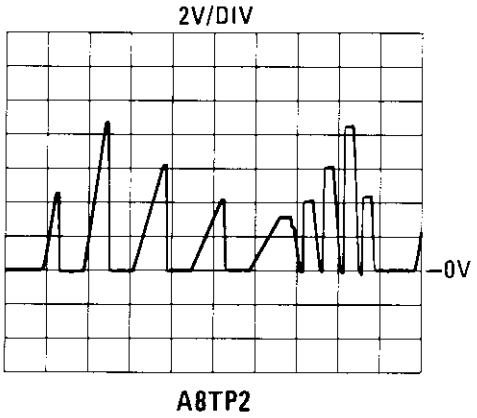


Figure 8-64. Scaled Tuning Voltage (A8TP2)

DELAY COMPENSATION

A failure in the delay compensation circuit is indicated by frequency errors that change with sweep time. For sweep times greater than 100 milliseconds, delay compensation has little effect on the frequency accuracy. On the HP 8350, enter **[INSTR PRESET]** and check waveforms in Figure 8-65.

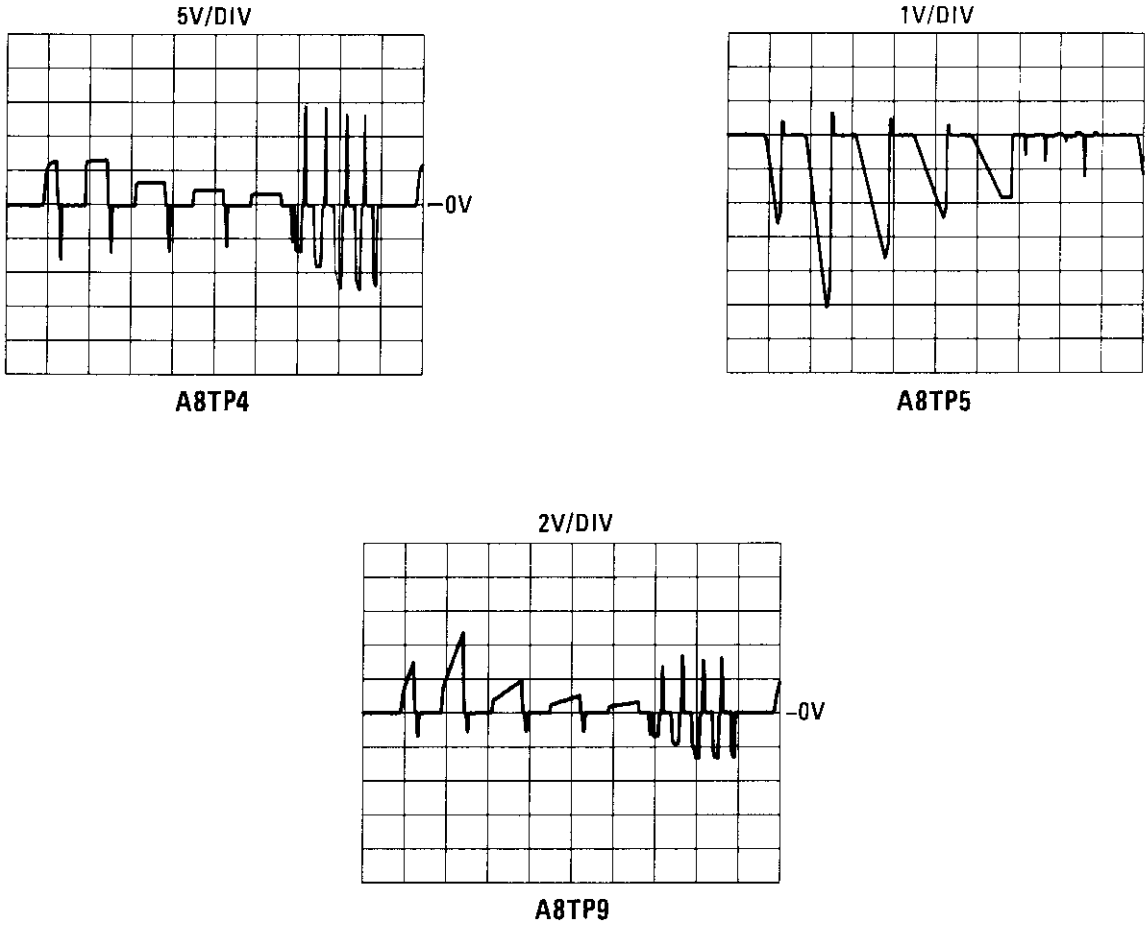


Figure 8-65. YO Delay Compensation Waveforms

YO DRIVE CIRCUITS

1. Check +20V FREQ REF at A7TP12 for +20V ±10 mV. If it is not, troubleshoot back to the mainframe supply.

The circuitry surrounding U21 and A9Q1 is responsible for converting the YO DRIVE V to a drive current for the YO coil. A failure here will usually result in extreme frequency errors.

2. Press **[INSTR PRESET]** to sweep the entire range of the plug-in. Check TP11 for the waveform shown in Figure 8-61. This represents the voltage (not the current) across the YO's main coil, and will give an indication as to whether current is passing through the coil. If this waveform is correct, suspect the YIG oscillator. Refer to the RF section troubleshooting information.

3. Check TP6. This voltage should track the YO DRIVE V (Figure 8-61). If it does not, troubleshoot U21, Q3, Q4, chassis mounted R1, and A9Q1.

    a. To verify proper operation of U21, ground TP6 (R1 is a 25 Watt resistor). Press HP 8350 **[CW]**. Vary the voltage at U21 pin 3 by changing the CW frequency as indicated on the front panel (20.0 GHz = −5V; 2.4 GHz = +12V). With TP6 at 0 VDC, U21 pin 6 should be at approximately +20 VDC for positive input voltages, and approximately −10 VDC for negative input voltages. If it is not, replace U21.

    b. Chassis mounted R1 should be checked by removing the A9 assembly from the instrument. The ohmmeter reading should be approximately 155 ohms.

    c. While the A9 assembly is removed from the instrument, check the collector-base and base-emitter junctions of A9Q1 with an ohmmeter. These junctions should show only a few hundred ohms when forward biased, and a high impedance in the reverse direction. If A9Q1 is found to be shorted or opened, make sure that protection diodes VR1 and CR5 are good before replacing the transistor.

    d. Q3 and Q4 can be checked, using the procedure above, while they are still in the circuit. The line power should be off.

DIGITAL CONTROL

The address decoder and data latch, and frequency cal switches comprise the digital control for the A8 assembly. A failure in these components usually results in large frequency errors.

To check the address decoding circuitry enter **[SHIFT] [5] [4]** and perform the following:

1. Examine L INST2 (P1-18) for activity. If none is found, troubleshoot the A3 assembly.

2. If L INST2 is functional, check each of the LENn lines (U16) for the pulses shown in Figure 8-66. If these are incorrect, but the address lines show activity, replace U16. If the address lines seem locked high or low, troubleshoot the address buffer on the A3 assembly.

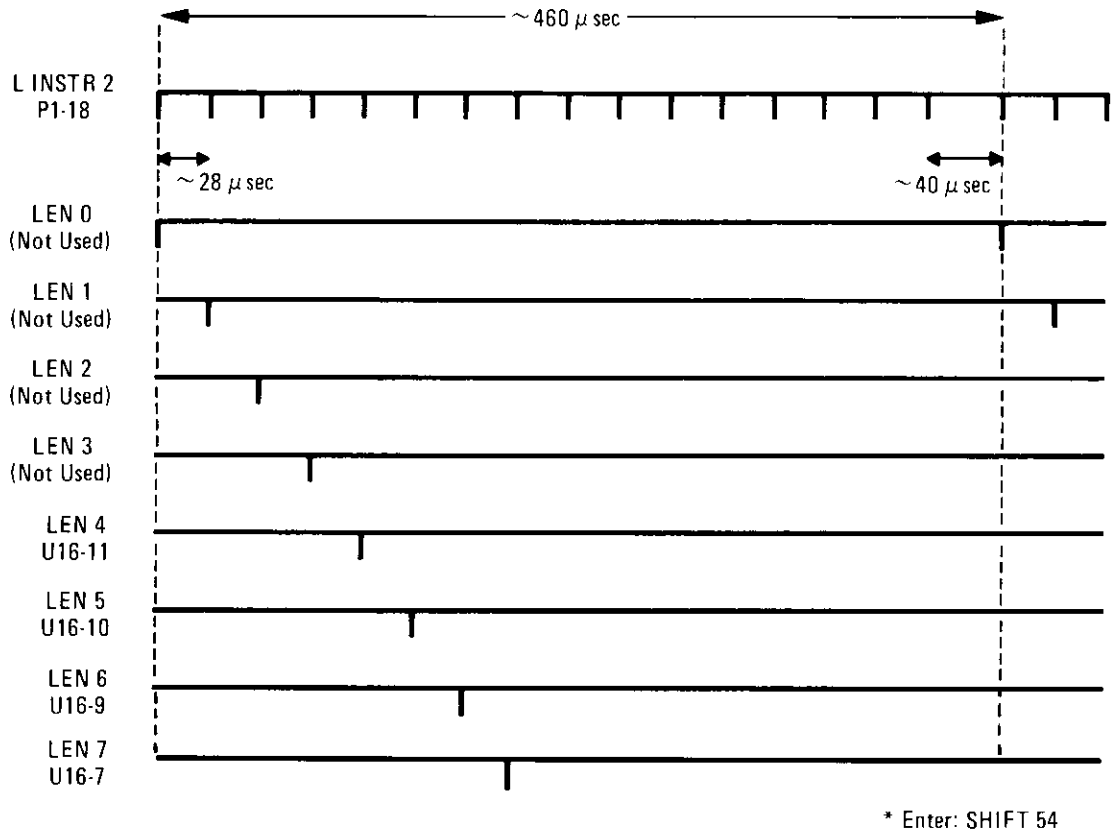


Figure 8-66. A8 Address Decoder Timing Diagram

NOTE: U3, U4, and U7 are checked by reading data while changing switch settings. Before altering the switch settings on A8S1 and A8S2, write down the present configuration. Return the switches to their original status after troubleshooting. If this is not done, the frequency endpoints will have to be recalibrated.

3. To check output buffer U7, press **[INSTR PRESET]**, and make the following key entry:

Press **[SHIFT] [0] [0]**	hex data mode
[2] [GHz] [8] [6]	address location 2C86 (U7)
[M3]	hex data read

The hex digits displayed in the HP 8350 front panel FREQUENCY/TIME window should change as the S1 and S2 switch positions 8 and 9 are toggled.

4. U3 and U4 can each be checked with hex data read (see above) at address 2C84 or 2C85. The hex digits should change when the corresponding freq cal switches are changed.

5. Exercise U13 with hex data rotation write. Enter:

Press **[SHIFT] [0] [0]**	hex data mode
[2] [GHz] [8] [7]	address location 2C87 (U13)
[M4]	hex data rotation write

Check the outputs of U13 against the waveforms shown in Figure 8-2.

−10V REFERENCE

Check TP12 for −10 VDC ±1 mV. If this voltage is incorrect, perform the −10V Reference adjustment procedure provided in Section 5 of this manual. If the adjustment cannot be made, check the anodes of VR2-4 for −6.2 VDC. If a voltage is incorrect, replace the zener diode. Check U5 pins 2 and 3 for −6.2 VDC ±0.15 mV. If either measurement is incorrect, troubleshoot U5 and associated circuitry.

5V REGULATOR

Check A9U1 pin 1 for slightly over +5 VDC (+5V UNREG from the HP 8350). Remove RF ribbon cables W4 and W14 to check for the possibility of excess loading. Then check A9U1 pin 2 for +5 VDC. If incorrect, replace A9U1.

CW FILTER

Relay K1 and C21 reduce residual FM by filtering the noise from the YO coil current. The relay is actuated by a line from U13. To check the data line, press HP 8350 **[CW]**.

Press **[SHIFT] [0] [0]**	hex data mode
[2] [GHz] [8] [7]	address location 2C87 (U13)
[M2]	hex data write
[0] [0] [BKSP] [BKSP]	hex data 00 and FF

Alternate between 00 and FF. Check U13, pin 7. If it is inactive, make sure protection diode CR6 is good. Then replace U13.

If U13 is working, alternate between 00 and FF, as described above, and verify that contacts in relay K1 are opening and closing.

A8 YO Driver/A9 Reference Resistor, Circuit Description

NOTE: All reference designators refer to the A8 assembly unless otherwise noted.

GENERAL

The A8 YO driver assembly converts the buffered tuning voltage from the A6 sweep control assembly into a drive current. The A9 reference resisitor assembly provides the current driver to control the frequency of the YIG oscillator.

Multiplying digital-to-analog converters (DACs) scale and offset the buffered tuning voltage to the frequency end-points in each band. Delay compensation is generated and summed with the tuning voltage. Also summed with the tuning voltage are low frequency external FM, and the FREQ CAL offset from the front panel. The resultant waveform at TP10 is then converted to a current-drive for the YO's main coil.

ADDRESS DECODER AND DATA LATCH, BLOCK A

The A8 YO driver uses hexadecimal address locations 2C84 through 2C87, decoded by U16 from signals BA0, BA1, and BA2. U16 is a 3-to-8 decoder that is enabled when L INST2 and address line BA3 are both low. L INST2, BA0, BA1, and the L DAC EN output of U8D are used by the scaled voltage tune and offset DACs.

U13 is a control latch which stores commands from the HP 8350 for the control lines used on the A8 YO driver assembly, primarily for delay compensation. The command byte is latched into U13 when LEN 7 pulses low. Refer to the delay compensation, summing amplifier, and YO coil current source sections for detailed descriptions of these control lines.

SCALED VOLTAGE TUNE DAC, BLOCK B
OFFSET DAC, BLOCK C

The scaled voltage tune and offset DACs function together to determine the frequency of the YIG oscillator. The offset DAC determines the start frequency of each band while the scaling DAC scales the BVTUNE input to tune the YIG oscillator over the required frequency range for each band.

U17 and U14 are 12-bit microprocessor-compatible DACs, which latch data in three four-bit nibbles. These DACs share the same address locations, but are loaded by different data lines (D0-D3 load U14 and D4-D7 load U17).

BVTUNE is a series of 0 to −10V ramps with each ramp corresponding to a frequency band. DAC U17 scales each ramp differently according to the frequency range the YO must sweep to cover the frequency range of the band. (See SC VTUNE waveform at TP2 in Figure 8-64.).

U17 scales the buffered tuning voltage (BVTUNE) according to the binary pattern loaded at its inputs. Inverting amplifier U18 is included in the feedback path to convert the current output of the DAC to a voltage. CR1 prevents transients from damaging the DAC during turn-on. C14, along with the DAC's internal feedback resistor, determine the bandwidth of the circuit. The waveform at TP2 is a scaled ramp (sawtooth waveform for multiband sweeps), with a maximum range of 0 to +10 VDC. See Figure 8-64.

U14 scales a stable −10V REF voltage according to the binary pattern loaded at its inputs. Inverting amplifier U15 works with the DAC's internal feedback resistor to provide a programmable offset voltage between 0 and +10 VDC at TP3. See Figure 8-62. CR7 protects the DAC from turn-on transients. C15 and the DAC's internal feedback resistor determine the bandwidth of the circuit.

DELAY COMPENSATION, BLOCK E

The delay compensation block circuitry is used to compensate the A13 YIG oscillator for the inherent inaccuracy caused by delay in the magnets at fast sweeps. The input signal is SC VTUNE, a scaled ramp from the scaled voltage tune DAC, the slope of which is proportional to the change in frequency. SC VTUNE is sent to two separate signal processors:

1. A voltage follower/subtractor whose output is equal to zero at start of sweep and at the band switch points. The amplitude is proportional to sweep width.
2. A differentiator whose output is proportional to the rate of frequency change while sweeping. These two signals are then mulitiplied in the analog multiplier U12. If the sweep oscillator is in a swept mode, U6 enables the delay compensation which is summed into the main coil driver voltage in the summing amplifier.

During retrace, and momentarily during bandswitching, analog switch U19B closes. In this condition, U10C together with R6, R8, R9, and R7 form a subtractor circuit. Both inputs are the input signal so they cancel in the operational amplifier and the resulting output is 0V, regardless of the input level. With U19B closed, C4 charges to one half the value of the input signal (R8 and R9 form a voltage divider). Ul9B opens again during the sweep which leaves only C4 in the feedback path of U10C. Since there is no discharge path with U19B and U19A open, C4 remains charged to the level it had just before U19B was opened. U10C now operates as a voltage follower, with the output level shifted by the voltage across C4. Therefore, the output of U10C has one half the slope of the input signal and returns to 0V whenever U19B is closed during retrace and bandswitching. The output of U10C is scaled by the HI adjust potentiometer and is applied, with an offset from the LO adjust potentiometer, to inverting amplifier U10D. The output generated at TP5 is one input to the analog multiplier.

If the sweep is stopped momentarily, such as when an external counter is used, L SSRQ is pulled low by the HP 8350 mainframe. When U19A is closed by a low on the L SSRQ control line to U8A, C4 slowly recharges through R62. Thus when L SSRQ is pulled the output of U10C will begin to go to zero volts, but may or may not reach zero volts depending on the length of time L SSRQ was pulled. When L SSRQ goes high again and the sweep continues, U19A opens and U10C resumes its voltage follower operation.

SC VTUNE is also applied to differentiator C3 and U10B. The output is amplified and inverted by U10A and is applied at TP4 to the second input of the analog multiplier. The output at TP9 is connected to U12 pin 7 to provide feedback for an operational amplifier internal to U12. The Z adjust at U12 pin 6 allows nulling of the offset voltage appearing at DLY COMP. This is done when in CF F mode where F equals zero.

During sweep retrace or at bandswitch points, the YIG oscillator must change frequency rapidly from the high end of its range to the low end, and does not have enough time to naturally settle to the proper start frequency. Unless the YO is forced to the low end of its range, this could result in a frequency error at the start of each sweep and each bandswitch point. In order to force the YO to settle quicker, C20 is charged during the YO retrace by the differentiator output through CR2. Timer U9 is triggered by L RTC COMP at each bandswitch point and at the end of sweep retrace. The timer pulse output momentarily closes analog switch U19C, and C20 discharges through R67 and is applied as retrace compensation to the summing amplifier. This compensation voltage forces the YO to the low end of its range to avoid frequency errors after a retrace or bandswitch. The amount of compensation applied is proportional to the pulse width of the timer output, and is adjusted by R55. As the RF plug-in is sequentially sweeping up between band, the frequency range the YO must retrace to reach the start frequency of the next band decreases. Thus, the amount of retrace compensation required is reduced. The timer output pulse width is reduced accordingly. This is accomplished by inverting the offset DAC output through Q1, and applying this negative voltage to the timer control voltage input at U9 pin 5. VR5 level shifts the offset DAC output for proper biasing of Q1.

+20V TRACKING, BLOCK F

Inverting amplifier U11 monitors the +20V line used to supply current to the YIG oscillator. If the +20V supply becomes loaded down or drifts, the YO main coil current and, consequently, the frequency will try to change. However, U11 senses any drift in the +20V FREQ REF line, and provides a correction signal so that the resultant YO DRIVE voltage (TP10) is compensated for the drift. ZRO adjustment R22 compensates for inaccuracies between U11 and summing amplifier U20.

SUMMING AMPLIFIER, BLOCK G

U20 provides the summing point for the scaled tuning and offset voltages, and provides a drive voltage (YO DRIVE V) for the current driver. Several correction signals are summed at this junction:

SC VTUNE provides the scaled ramp portion of the YO DRIVE voltage. R19, GAIN, fine-tunes the range of the scaling DAC.

OFFSET adjusts the YO DRIVE voltage so that the YO coil is driven between the proper end points, as determined by the front panel controls. R24, "OFS", fine-tunes the range of the offset DAC.

SUPPLY VOLTAGE CORRECTION provides a compensation signal, from the +20V tracking amplifier, to offset changes in the reference supply.

DLY COMP, from the delay compensation circuit, is added to correct for lags in the response time of the YIG oscillator. This compensation is derived from SC VTUNE.

RTC COMP, from the delay compensation circuit, is a momentary correction voltage that forces the YIG oscillator to the low end of its frequency range after a sweep retrace and each bandswitch point. This compensation is derived from SC VTUNE.

FREQ CAL (from the A1/A2 front panel) is summed in through U19 when the BAND 0 line from U13 is high. This offset corrects for errors in the fixed cavity and YIG oscillator frequencies while in band 0.

YO LO FM sums low frequency components of external FM signals onto the drive voltage when crossover coupling of the FM signal is selected. (Configuration switch A3S1 provides this adjustment. Refer to the A3 service section for further detail.) Due to the response time limitations of the YIG oscillator's main coil, only frequencies below 700 Hz are passed from the A5 FM driver assembly to the A8 YO assembly.

−10V REFERENCE, BLOCK H

Operational amplifier U5 generates a −10V output from the −6.2V reference voltage at its non-inverting input. The amplifier gain is determined by feedback resistors R43, R44, and R45. Emitter follower Q2 provides the current. The −6.2V reference input to U5 is developed across 3 parallel zener diodes to reduce noise. Further noise reduction is provided by the RC network on the non-inverting input of U5 and C17 across the feedback path. −15 VF, through R1, provides the initial start-up bias.

FREQUENCY CAL SWITCHES/OUTPUT DATA BUFFERS, BLOCK D

DIP switches S1 and S2, with their corresponding data bus buffers, are used to digitally calibrate the low and high end frequencies in band 2. The data on these switches is read by the microprocessor during power-up and INSTR PRESET and is used to calculate the settings for the scale and offset DACs. S1, with pull-up resistor package U1, is read through U3 when enabled by LEN4. S1 determines the value of the offset DAC and calibrates the low end frequency. S2, with pull-up resistor package U2, is read through U4 when enabled by LEN5. This establishes the scale DAC values, and calibrates the high end frequency. The ninth and tenth bits from S1 and S2 are read through U7.

S1 and S2 switch positions encode binary numbers to set up the offset and scaling DACs. Refer to the frequency accuracy adjustment procedure in Section 5 for instructions. Figure 8-67 illustrates the switch configurations.

YO COIL CURRENT SOURCE, BLOCK I
YO COIL CURRENT DRIVER A9, BLOCK K

The YIG coil current driver works with the chassis mounted reference resistor R1 and YO coil driver A9Q1 to drive a current proportional to the drive voltage through the YIG's main tuning coil.

U21, Q3, Q4, and A9Q1 comprise a voltage-to-current converter and current driver for the YO's main coil. The non-inverting input of U21 receives the YO DRIVE voltage signal. The inverting input of U21 monitors the voltage drop across reference resistor R1, which is directly proportional to the coil current. If the drive current is not tracking the drive voltage, U21 will produce an error voltage to correct the difference. Emitter-follower Q4 and common-emitter-stage Q3 provide the current gain needed to drive A9Q1. Q4 and Q3 emitter currents are also drawn through chassis mounted R1, and therefore, sensed by U21. VR1 and CR5 protect the current drive transistors by limiting voltage spikes due to sudden changes in the coil current. R33 helps to dampen ringing caused by the parasitic capacitance and the inductance of the YO coil.

When HP 8350 **[CW]** and RF plug-in **[CW FILTER]** are selected, LCW goes low, energizing relay K1. C21 filters out noise in the YIG coil current, reducing the residual FM noise in the CW mode.

CR4, CR8, and their associated factory-select resistors provide a two break-point compensation network to correct for non-linearities in the YO characteristics.

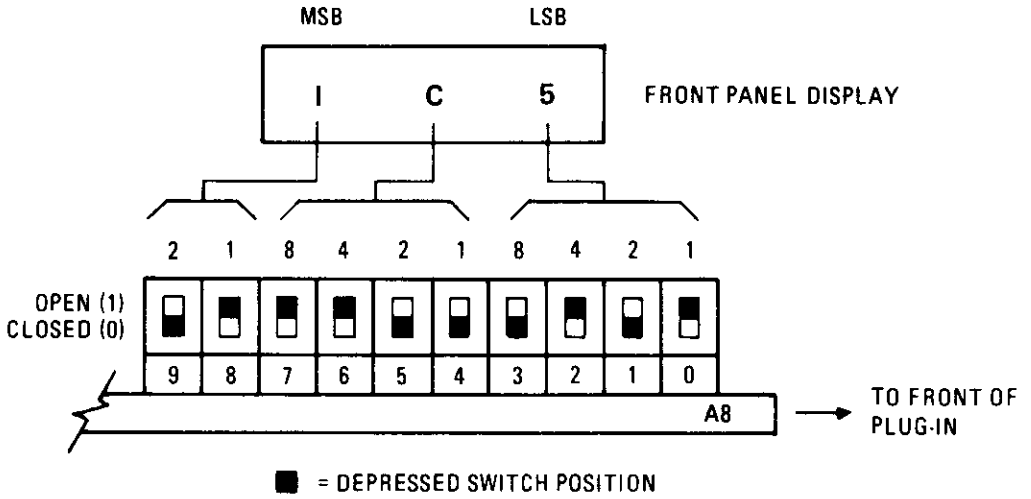
NOTE: The values of the factory-select resistors are stamped on a label, attached to the RF casting. Matching resistor sets (mounted on a header) are supplied with replacement YOs and must be installed on the A8 YO assembly. The new label, indicating the replacement resistor values should be attached to the RF casting.

If the A8 YO driver assembly is replaced, the shaping resistors from the defective assembly (which are mounted on a header) must be reinstalled in the new assembly.

NOTE: If the YO needs little or no compensation, some or all of the factory-select resistors may be omitted.

+5V REGULATOR A9, BLOCK L

A9Q3 is a +5 VDC regulator mounted in a single package. It receives the +5V UNREG line (slightly more than 5V) from the mainframe, and regulates it for use in the plug-in RF components.



Hexadecimal	Binary	Decimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
A	1010	10
b	1011	11
C	1100	12
d	1101	13
E	1110	14
F	1111	15

Figure 8-67. A8S1/S2 Switch Configuration

Table 8-21. A8P1 and A9P1 Pin-Outs

A8P1

PIN	SIGNAL	I/O	TO/FROM	FUNCTION
1 23	YO LO FM FREQ CAL	IN IN	A5P-2 A10J1-37	G G
2 24	 GND ANLG		NOT USED	 L
3 25	−10VREF BVTUNE	OUT IN	A4P1-43,A6P1-39, A7P1-3 A6P1-42	H B
4 26	 GND ANLG		NOT USED	 L
5 27	L SSRQ +5V	IN IN	A6P1-23 A3P1-6,7	E L
6 28	−40V −15V	IN IN	P1-11 P2-28	L L
7 29	+10V GND ANLG	IN	P1-8	L L
8 30	GND DIG GND DIG			L L
9 31	BD1 BD0	I/O I/O	A3P1-9 A3P1-31	A,C,D A,C,D
10 32	BD3 BD2	I/O I/O	A3P1-10 A3P1-32	A,C,D A,C,D
11 33	BA1 BA0	IN IN	A3P1-11 A3P1-33	A,B,C A,B,C
12 34	BA3 BA2	IN IN	A3P1-12 A3P1-34	A A
13 35	BD5 BD4	I/O I/O	A3P1-13 A3P1-35	A,B,D A,B,D
14 36	BD7 BD6	I/O I/O	A3P1-14 A3P1-36	B,D B,D
15 37	GND ANLG GND ANLG			L L
16 38	+20V +15V	IN IN	P1-7 P2-29	L L
17 39	−10V −40V	IN IN	P1-13 P1-11	L L
18 40	LINST 2	IN	A3P1-29 NOT USED	A
19 41	GND ANLG		 NOT USED	L
20 42	YO COLLECTOR		A9P1-2 NOT USED	I
21 43	YO BASE	OUT	A9P1-2 NOT USED	I
22 44	YO COIL +20V FREQ REF	 IN	A9P1-4 A9P1-5,A7P1-44	I I

Table 8-21b. A8P1 and A9P1 Pin-Outs

A9P1

PIN	SIGNAL	I/O	TO/FROM	FUNCTION
1 7	YO BASE +5V REG	IN OUT	A8P1-21 A10J4-7,A10J5-3,11	K J
2 8	YO COLLECTOR SYTM COIL	OUT OUT	A8P1-1 A7P1-22,A10J4-8	K
3 9	+20V SYTM BASE	IN IN	P1-7 A7P1-21	K
4 10	YO COIL SYTM COLLECTOR	OUT IN	A8P1-22 A7P1-20	K
5 11	+20V FREQ REF +20V	OUT IN	A7P1-44,A8P1-44 P1-7	K K
6 12	GND ANLG +5V UNREG	 IN	P2-27,58-59 P2-63	J J

Troubleshooting the RF Section

NOTE: Many RF path failure symptoms are closely related to A4 ALC failures. Refer to A4 troubleshooting for additional information.

INTRODUCTION

The RF path consists of the microcircuits and their bias boards that produce the actual front-panel RF output. These microcircuits are sealed, cannot be repaired, and are costly to replace. Ensure that associated control circuits (i.e. the other printed circuit boards) are working correctly before replacing any microcircuit components. When certain of a failure in the RF components, isolate the problem to a single microcircuit assembly.

Five RF assemblies have bias boards attached directly to the microcircuit packages:

The A17 band 0 amplifier is directly attached to its bias assembly. The A17A1 amplifier bias assembly cannot be repaired, is not separately replaceable, and is supplied with the A17 microcircuit.

The bias boards for A12, A13, A14, and A16 contain factory adjusted or factory selected components, and cannot be separately replaced. If a bias assembly component (e.g. protection diode or transistor) has been externally damaged, it is acceptable (and economical) to replace that individual component. However, a bias assembly failure often indicates a failure inside the microcircuit and may require that the entire assembly be replaced.

WARNING

Many microcircuits are extremely sensistive to static electric discharges (more so when the microcircuits are removed from their bias boards or control circuits).

Before handling a microcircuit, discharge your own body by touching the instrument chassis or microcircuit package. Avoid touching the center conductors of the RF connectors and bias feedthrus at all times.

Microcircuits should be stored and transported in static-protective packaging. Never package microcircuits with styrofoam, cellophane (unless treated for static), or adhesive tape.

Do not attempt to test any microcircuits, at a bias feedthru or the RF connectors, with an ohmmeter. Resistance measurements are rarely useful, and will often destroy a working microcircuit. Measure DC voltages at the bias feedthrus with a high-impedance DC voltmeter only with bias or control connections intact.

The following troubleshooting procedure traces power levels through the RF path. RF measurements should be made with a high-frequency spectrum analyzer or an RF power meter. A type-N female to SMA adapter, along with a short flexible RF cable terminated at both ends with SMA male connectors, will make troubleshooting easier.

Breaking RF connections within the ALC loop will cause the loop to go unleveled, producing abnormally high power levels (up to +20 dBm) and harmonic distortion. In band 0, the ALC loop includes all connections between the A18 modulator/mixer and DC1 directional detector. In bands 1 through 4, the ALC loop includes connections between A16 modulator/splitter and DC2 directional coupler. (Figure 8-24, within the A4 troubleshooting section, provides a graphic definition of the loop.) If necessary, the modulators may be externally biased using the open loop procedure described in the A4 troubleshooting section. If possible, avoid breaking the ALC loop to make RF measurements. In any case, it is a good idea to begin troubleshooting just outside the ALC loop.

FAILURE SYMPTOMS

The information below should be used to help systematically troubleshoot to the individual RF assembly. Based on the failure symptom, the components most likely to have failed are listed, with the most probable failure cited first. Hints for ensuring that the RF path is actually responsible for the failure are also given. For troubleshooting information related to a specific assembly, refer to the paragraphs titled Microcircuit Verification By Assembly.

NOTE: All references to test points, pin connections, etc., can be located on the RF schematic.

NO RF POWER – All Bands

A13 YIG Oscillator

A YO failure is indicated if the RF power at the rear panel AUX OUTPUT connector is less than −10 dBm (nominally 0 dBm). Check power supplies and bias levels. L RF ON (TP "ON") should be at −10 VDC. TP "G" should be approximately −2 VDC. Check TP "M" for the waveform entitled YO COIL, Figure 8-67, within the A8 service section. This waveform represents the current across the main coil. Check the RF output directly at the YO for approximately +14 dBm at several frequencies.

A16 Modulator/Splitter

A modulator/splitter failure is indicated if there is at least −10 dBm at the rear panel AUX OUTPUT connector. Disconnect PULSE MOD input to A16J4 to eliminate the possibility of the pulse modulation circuit (on the A6 sweep control assembly) turning the RF power off. If there is still no RF output power, check the modulator/splitter output power at A16J6 and J7.

A12 Switched YTM

The easiest place to access the A12 SYTM RF output is at the W15 input to DC2 directional coupler. Also check the SYTM power supplies and bias voltages.

NO RF POWER — Band 0

A17 Amplifier

Check power supplies. Check the power directly out of A17. This will open the ALC loop. Expect to measure approximately +20 dBm unleveled RF output with high harmonic distortion. If this is undesirable, refer to A4 troubleshooting and follow the open loop procedure to externally level the RF while opening the ALC loop.

A18 Modulator/Mixer

If A18 is the suspected component, remove the A4 assembly. This removes all modulator current and provides an unrestricted path for RF. If full unleveled RF power is achieved, refer to A4 troubleshooting. If band 0 remains dead, disconnect W23 and check the RF output directly out of the mixer (open loop power should measure approximately −12 dBm).

A11 Cavity Oscillator

Check power supplies. Check RF output for approximately +9 dBm at 3.8 GHz.

NO RF POWER — Bands 1 through 4

A16 Modulator/Splitter

Remove the A4 assembly. This removes all bias current from the modulator and provides an unrestricted path for RF. If full unleveled power is achieved, refer to A4 troubleshooting. If bands 1 through 4 remain dead, disconnect W20 and check the RF output directly out of A16 (open loop power should measure approximately +9 dBm).

A14 Power Amplifier

Check power supplies. Verify that L AMP OFF is a logic high (it is pulled high on A14A1 and is a "no connection" on the A10 motherboard). The easiest place to access the A14 output power is at the output of the AT1 isolator (approximately +26 dBm). If there is no power at this point check the power directly at the A14 output.

A12 Switched YTM

Verify the PIN SW control voltage (A6TP6) is +10V for band 0 and −5V for bands 1 through 4. The easiest place to access the SYTM RF output is at the W15 input to DC2 directional coupler.

MAXIMUM RF UNLEVELED POWER — All Bands

Refer to this symptom under A4 troubleshooting.

MAXIMUM UNLEVELED RF POWER — Band 0

DC1 Directional Detector

Select a CW frequency in band 0. Verify maximum unleveled RF output power. Check INT DET 0 output to be equal to or more negative than −0.2 VDC. (It may be necessary to perform INT DET 0 BIAS adjustment. Refer to Section 5, Adjustments.) For more information, refer to A4 troubleshooting. HSA17 Modulator/MixerCheck modulator bias line MOD 0. It should be slightly negative. If it is approximately +4 VDC while A4TP6 is approximately +4 VDC, the modulator diode is probably open. If MOD 0 is at 0.0 VDC, but A4TP6 is at +4 VDC, troubleshoot the A4 modulator drivers and connections to the modulator.

MAXIMUM UNLEVELED RF POWER — Bands 1 through 4

CR1 Detector

Select a CW frequency in band 1 and check for maximum unleveled RF output power. Check the output of CR1 for approximately −0.05 VDC, using an SMC tee or by probing A4P1-20.

A16 Modulator/Splitter

If CR1 produces about −0.05 VDC, check that A4TP6 is at +4 VDC. If not troubleshoot A4. Then check MOD 1. It should be slightly negative. If it is approximately +4 VDC the modulator diode is open. If MOD 1 is near 0.0 VDC while A4TP6 measures +4 VDC, check A4 mod drivers and the connections to the modulator.

HARMONIC DISTORTION — All Bands

A13 YIG Oscillator

Refer to Section 5, Adjustments, and perform the harmonic adjustments. If harmonics are still unacceptable in all bands, check the spectral purity of the YO output. If harmonics are less than 14 dB below the fundamental, replace A13.

HARMONIC DISTORTION — Band 0

A17 Amplifier

Check the power level into A18 modulator/mixer, and trace the problem back through the RF path if it is too low. Measuring power or spectral content directly out of A18 or A17 will break the ALC loop, causing maximum unleveled power and high harmonic distortion even without a failure. Refer to A4 troubleshooting and perform the open loop procedure. This procedure externally biases the modulators to level RF power while the ALC loop is open.

HARMONIC DISTORTION – Bands 1 through 4

A14 Power Amplifier

Check power supplies and biases. Check power levels into A14. Measuring power or spectral content into or out of A14 will break the ALC loop and cause distortion even without a failure. Refer to A4 troubleshooting and perform the open loop procedure. This procedure externally biases the modulators to level RF power while the ALC loop is open.

SPURIOUS DISTORTION – Band 0

A18 Modulator/Mixer

Select a CW frequency in band 0, and check RF output for spurs 3.8 GHz removed from the carrier. The mixer may be leaking the swept LO frequency (3.81 – 6.2 GHz). However, the A17 amplifier should filter these out.

POWER DROP-OUTS – Any Band

A13 YIG Oscillator

If power is present and leveled across part of a band, but drops out entirely for the rest of the band, suspect A13. Check for power dropouts at the rear panel AUX OUTPUT connector.

POWER HOLE – Any Band

Check all RF connections in the proper loop(s). Narrow-band power dips or "holes" are usually the result of loose or faulty RF connections. Tighten all RF connectors internally. Secure the front-panel RF connection. Inspect the front-panel RF connector for damage or wear, and clean or replace parts as necessary Section 6, Replaceable Parts, provides an exploded view of this connector.

DC BIAS AT RF OUTPUT

A12 Switched YTM

The SYTM provides the DC blocking function for the RF plug-in output port. If a DC bias exists at the front-panel connector, the failure is almost certainly in A12.

MICROCIRCUIT VERIFICATION BY ASSEMBLY

The information below is organized by microcircuit assembly in RF signal flow order. It provides troubleshooting tips to isolate a particular microcircuit failure. This information is intended as a guide. Any suspected failure should be thoroughly researched before replacements are made.

The general approach to troubleshooting is:

1. Make sure that all power supply voltages are present. If not, trace the problem back through the RF plug-in to the HP 8350.
2. Make sure all bias and control signals are present. If not, trace the problem back to the supplying assemblies.
3. Check the RF levels into the suspected microcircuit. If faulty, trace the problem back through the RF path.
4. Check the RF levels out of the suspected microcircuit. If faulty, replace the assembly.

IN EVERY CASE, check power supply voltages. Make sure control signals and bias voltages are being supplied from the other circuits before replacing any microcircuit. Refer to the troubleshooting information appropriate to the assembly supplying the control signals for voltage levels and waveforms.

A13 YIG Oscillator

Check RF output at the rear panel AUX OUT for greater than −10 dBm, then check power directly from the YO for about +14 dBm.

A16 Modulator/Splitter

RF power into A16 can be checked at the rear panel AUX OUT. The pulse modulator can be disabled by disconnecting the PULSE MOD input at A16J4. Verify output power at both A16 outputs.

A11 Cavity Oscillator

The output of this assembly should measure approximately +9 dBm RF power at 3.8 GHz.

A18 Modulator/Mixer

Ensure that A11 is functioning, and A16 modulator/splitter is transmitting power in band 0. Control line MOD 0 should be near +0.7 VDC. If not, remove the modulation control wire and check for approximately +5 VDC. If this is not the case, troubleshoot A4. To verify the modulator/mixer, remove the A4 assembly. Monitor the RF output directly from A18. In this open loop condition the power should measure approximately −12 dBm. (Expect high harmonic distortion.).

A17 Amplifier (Band 0)

Check for power input as described under A18, above. Verify RF output at approximately +20 dBm unleveled with high harmonic distortion. When trying to isolate harmonic sources, refer to A4 troubleshooting and follow the open loop procedure. This procedure externally biases the modulators to level the RF power under open loop conditions.

DC1 Directional Detector

Check for approximately +15 dBm of leveled output power. Ensure that band 0 power is nominally +10 dBm and check the detector output, E2, for approximately −0.2 VDC or more negative. If temperature drift is suspected, check that the INT DET 0 BIAS adjustment (A4R4) has an effect on the detected output level. If it does not, replace DC1.

A15 DC Return

An A15 failure is extremely unlikely. However, this component can be tested OUT OF CIRCUIT with an ohmmeter. Verify that both connectors provide a DC short to ground.

A14 Power Amplifier

Ensure that A16 transmits approximately +9 dBm RF power. If not, trace the problem back to the YO.

AT1 Isolator

Check the RF output directly from the isolator. Insertion loss through this device should be less than 1 dB.

A12 SYTM

For band 0, the RF path through A12 is essentially a straight through path. Verify the PIN SW input is +10 VDC when in band 0.

For bands 1 through 4, check the PIN SW and SRD BIAS levels. If RF output power is significantly increased by adjusting the front panel PEAK control, perform the SYTM to YO tracking adjustment in Section 5.

DC2 Directional Coupler

Insertion loss through the coupler should be less than 1 dB in all bands. Failures here are extremely unlikely.

CR1 Detector

Check the detector output for approximately −0.05 VDC in bands 1 through 4 when leveled at +10 dBm, and slightly more negative when unleveled. This measurement can be taken at the detector output using an SMC tee or by probing A4P1-20 (accessible on the underside of motherboard A10).

A19 Step Attenuator (Option 002 Only)

Check the output of DC2 for approximately +10 dBm. Verify that A3 configuration switch is set for Option 002 (see A3 troubleshooting, Table 8-10). Set the HP 8350 front panel step keys, [▲] [▼], for 5 dB steps. Increment the power setting with the step keys to run the attenuator through its 55 dB range. (Power meters will typically NOT have the dynamic range to verify this operation.) The control circuits can be manually exercised by operating the sweep oscillator in the CW mode and performing a hex data write to address 2F00. Enter two hex digits in the format 0x'', where 00 equates with 0 dB attenuation, 01 with 5 dB attenuation, 02 with 10 dB attenuation, and so on.

RF Section, Circuit Description

INTRODUCTION

The RF Section includes the high frequency microcircuits, with their bias boards, that produce the actual RF output power. These components include A11 through A19, AT1, DC1, DC2, and CR1. All other plug-in assemblies function essentially to control these RF components. The connections between microcircuits and other assemblies are provided on the overall block diagram. Refer to the overall block diagram circuit description for a more general, functional description.

NOTE: Assembly circuit descriptions are discussed in signal flow order. Headings indicate in which frequency band(s) the assembly is active.

BANDS 0 THROUGH 3

A13 YIG Oscillator

The A13 YIG oscillator is a solid-state tunable microwave source. Its output frequency ranges from 2.4 to 7.0 GHz, with approximately +12 to +14 dBm of output power. The oscillator's resonant tank circuit is basically a small YIG sphere with a resonant frequency which depends on the surrounding magnetic field strength. The magnetic field is established by an opposing pair of electromagnetic "main coils". Changing the current through the coils changes the magnetic field strength, and hence the frequency of oscillation. The sphere is lightly coupled to a bipolar transistor, providing the gain necessary to sustain oscillation. A FET amplifier provides the final output power gain.

The A13A1 YO bias assembly supplies the biasing for the oscillator and YO amplifier. This assembly is matched to the YO, and cannot be separately replaced. The bias assembly provides zener protection against high voltage transients that appear across the main coils. It also supplies current for a resistive heater that helps maintain the oscillator at a constant temperature. Factory adjustment R4 optimizes the FET gate bias for minimum harmonics.

A16 Modulator/Splitter

The A16 modulator/splitter divides the YO output into two paths (one for band 0 and the other for bands 1 through 4). The RF input from the YO is coupled off and supplied to the rear panel AUX OUTPUT with a power level of approximately 0 dBm.

The modulator/splitter uses two PIN diode modulators (a third is not used). The PULSE MOD input switches its PIN diode modulator full on or full off, and provides an RF on/off ratio of greater than 30 dB. Since this modulator is positioned before the splitter, it provides pulse modulation for all bands.

The MOD 1 input provides amplitude control for bands 1 through 4 and is used for amplitude leveling.

BAND 0

A18 Modulator/Mixer

The A18 modulator/mixer mixes a fixed 3.8 GHz signal with the swept 3.81 to 6.2 GHz YO output, producing the 0.01 to 2.4 GHz RF output in band 0. Unwanted mixing products are minimized by frequency selective circuits within the microcircuit. The swept YO output, after passing through the A16 modulator/splitter, acts as the local oscillator signal for the mixer. The internal PIN diode modulator attenuates the fixed 3.8 GHz input, providing both amplitude leveling and square wave modulation (generated by the HP 8350 mainframe) for band 0. The mixer has a high conversion loss, and produces approximately −12 dBm of mixed output with +9 dBm of 3.8 GHz input and no modulator attenuation.

A11 Cavity Oscillator

The A11 cavity oscillator provides a fixed 3.8 GHz RF output at approximately +9 dBm to mix down the swept YO output, yielding the band 0 heterodyned low-frequency output. This source is extremely stable in both frequency and amplitude. The +20V and −10V lines provide power for the A11 assembly, and two large, separately replaceable capacitors help filter these supplies to reduce residual FM noise.

A17 Amplifier

The A17 amplifier provides approximately 40 dB of gain from 0.01 to 2.4 GHz for band 0. The amplifier gain drops sharply at higher frequencies, providing a low-pass nature which rejects the unwanted mixing products. The A17A1 amplifier bias assembly provides the various bias currents for the band 0 amplifier. It is matched and attached to the microcircuit at the factory, has no adjustments or replaceable parts, and cannot be replaced separately as an assembly. The +20V and L B0RF ON lines provide the power. When the RF is "off" or the plug-in is operating in bands 1 through 4, the bias is removed, shutting down the amplifier altogether.

DC1 Directional Detector

The DC1 directional detector detects the RF power amplitude for band 0 leveling. The insertion loss for the entire package is less than 3.5 dB.

A simple resistive directional bridge samples a portion of the RF energy to a diode detector. The RF is rectified and filtered, providing a voltage proportional to the peak RF amplitude, which is used for leveling in band 0. A single resistor (A16A1R9) biases the detector diode through feedthrough E1. Feedthrough E2 carries the detected signal, but also carries a second bias current from the A4 assembly for a second, temperature-compensating diode. An internal resistor helps protect the static-sensitive diodes.

A15 DC Return

The A15 DC return is simply a shunt RF choke which allows DC bias currents to flow to ground without shunting any RF energy. Insertion loss is typically less than 0.5 dB.

BANDS 1 THROUGH 4

A14 Power Amplifier

The A14 power amplifier amplifies the fundamental YO output, covering the 2.4 to 7.0 GHz range. The amplifier provides approximately 25 dB of gain at maximum leveled power.

The A14A1 amplifier bias assembly contains several factory adjusted bias adjustments. These are adjusted at the factory to minimize harmonics.

AT1 Isolator

AT1 provides 20 dB of isolation and is accountable for less than 1 dB of insertion loss. AT1 improves the match to the SYTM.

BANDS 0 THROUGH 4

A12 SYTM

The A12 switched YIG tuned multiplier uses a PIN diode switch to select one of two RF inputs. For band 0, the SYTM provides a straight through path for the 0.01 to 2.4 GHz RF from the A15 DC return. Insertion loss for band 0 is typically less than 0.5 dB.

For bands 1 through 4, the RF from the AT1 isolator is selected. This RF input is applied through an impedance matching circuit to a SRD (step recovery diode) which has an output that is rich in harmonics. The SRD BIAS applied to the diode is changed for each band to optimize the generation of the harmonic used for that band (band 1 = fundamental, band 2 = second harmonic, band 3 = third harmonic, band 4 = fourth harmonic). The YIG tuned filter is a tunable bandpass filter which is tuned to the RF output frequency by the SYTM coil drive-current supplied by the A7 SYTM driver.

The filter's bandpass frequency is determined by a small YIG sphere with a resonant frequency that depends on the surrounding magnetic field strength. The magnetic field is established by an opposing pair of electromagnet coils. Changing the current through the coils changes the magnetic field strength, and hence the bandpass frequency.

The dynamic response of the SYTM (i.e. how fast the bandpass frequency changes for a fast change in coil current) is limited, due to the inductive and magnetic delays of the electromagnet coils and poles. Delay compensation circuits help during a sweep, but frequency modulation is limited to low modulation frequencies. Since the range of deviation for high-frequency modulation is limited by the YIG oscillator, the RF frequency stays within the bandpass of the SYTM, and the SYTM does not need to be modulated at higher rates.

DC2 Directional Coupler

The DC2 directional coupler has a −16 dB coupling coefficient. The reverse-coupled port is terminated. The coupled output is sent to the CR1 detector for leveling in bands 1 through 4. Although the band 0 output (0.01 to 2.4 GHz) must pass through the DC2 assembly, it plays no part in band 0 leveling. The insertion loss is less than 0.8 dB, not including the coupled power loss.

CR1 Detector

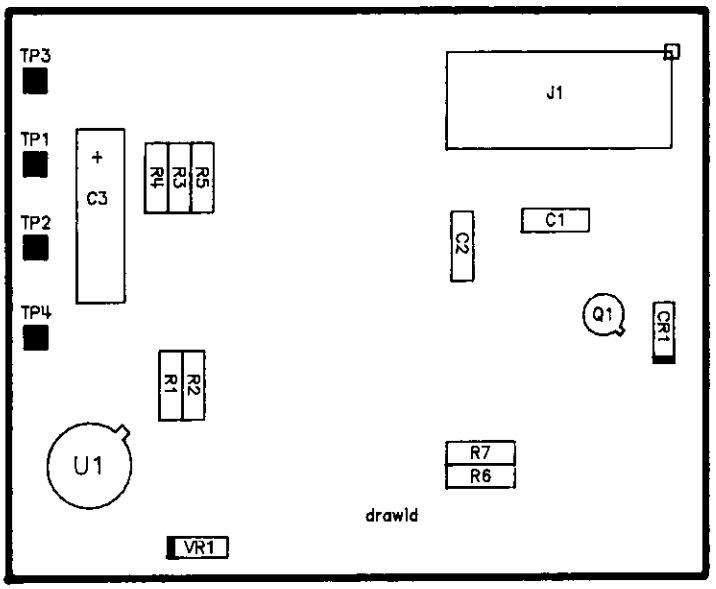
The CR1 detector rectifies and filters the RF output coupled by the DC2 directional coupler for leveling in bands 1 through 4.

A19 Step Attenuator (Option 002 Only)

On RF plug-ins equipped with Option 002, the A19 step attenuator provides 55 dB of attenuation in 5 dB steps. Combined with the range of the ALC loop, this yields a maximum power range of +10 to −60 dBm. The step attenuator functions as four fixed attenuators, with 5, 10, 20, and 20 dB of attenuation. Latching relays close contacts which either insert these attenuators in the RF path or bypass them. The control and drive circuitry for the attenuator is located on the A2 front panel interface assembly. The insertion loss, with 0 dB attenuation selected, is may be as much a 4.6 dB at 26.5 GHz (See specifications in Section 1). By pressing **[SHIFT] [POWER SWEEP]** the control of power is within the ALC range without changing the attenuator settings. The display in the **[SHIFT] [POWER SWEEP]** mode disregards attenuator settings and displays the ALC settings. Pressing **[SHIFT] [SLOPE]** allows control of attenuator steps without affecting the ALC setting. In this mode the attenuator setting is displayed.

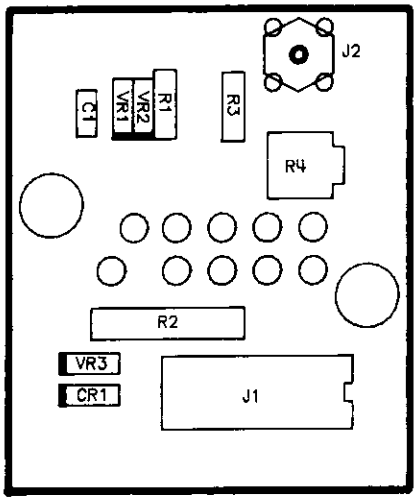
RF Output Connector

On standard or Option 002 instruments, the RF output is directed to the front panel. On plug-ins with Option 004 (with or without other options), the output is directed to the rear panel. The standard RF output connector is a female type-N.



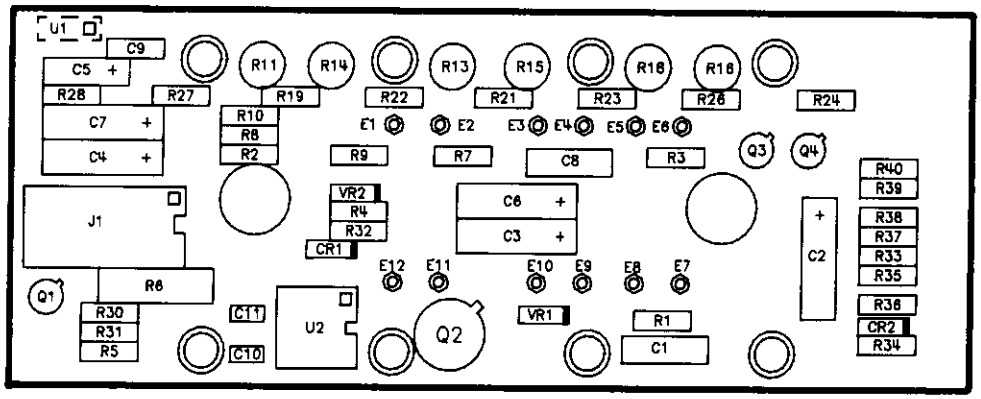
P/O HP P/N 5086-7440

Figure 8-72. A12A1 SYTM Bias, Component Locations



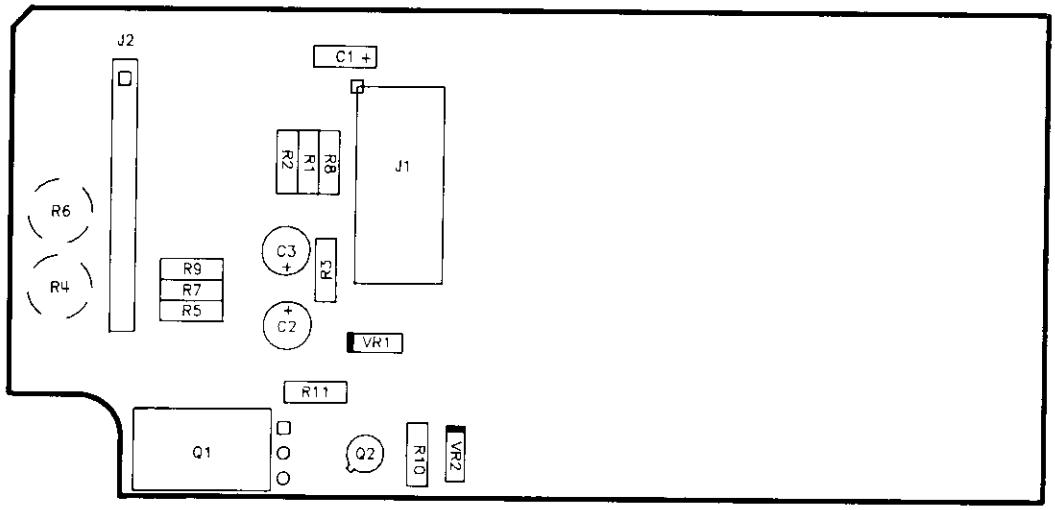
P/O HP P/N 5086-7337

Figure 8-73. A13A1 YO Bias, Component Locations



P/O HP P/N 5086-7217

Figure 8-74. A14A1 Power Amplifier Bias, Component Locations



P/O HP P/N 5086-7339

Figure 8-75. A16A1 Modulator/Splitter Bias, Component Locations

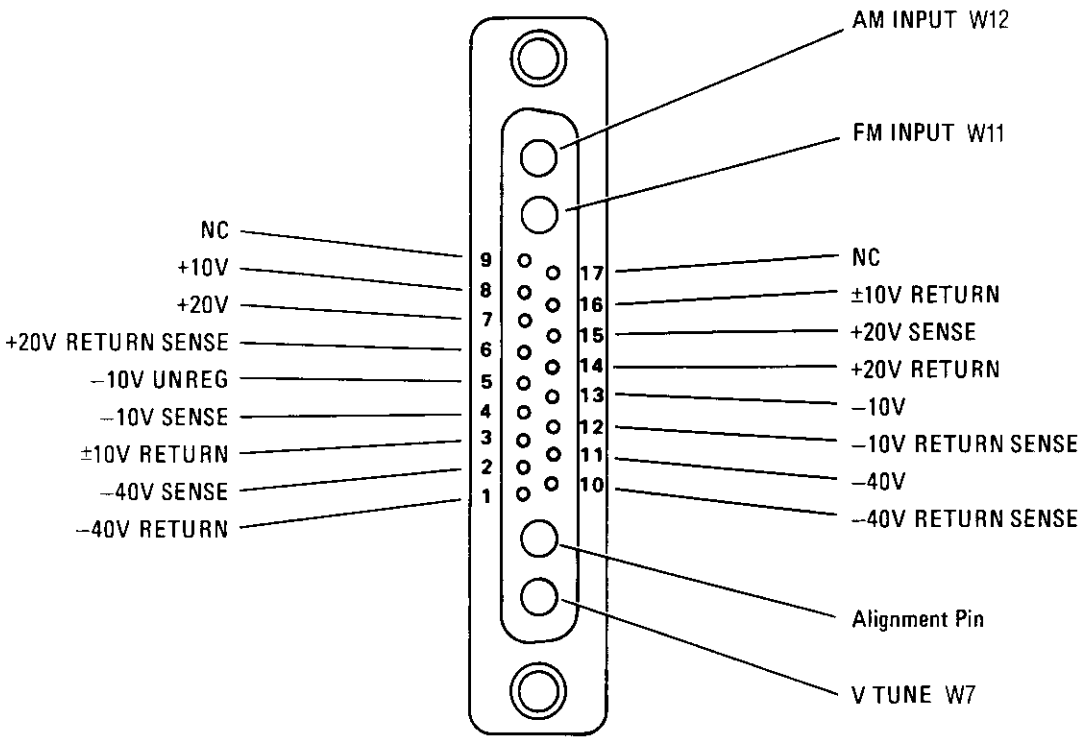


Figure 8-77. Interface Signals on Connector P1

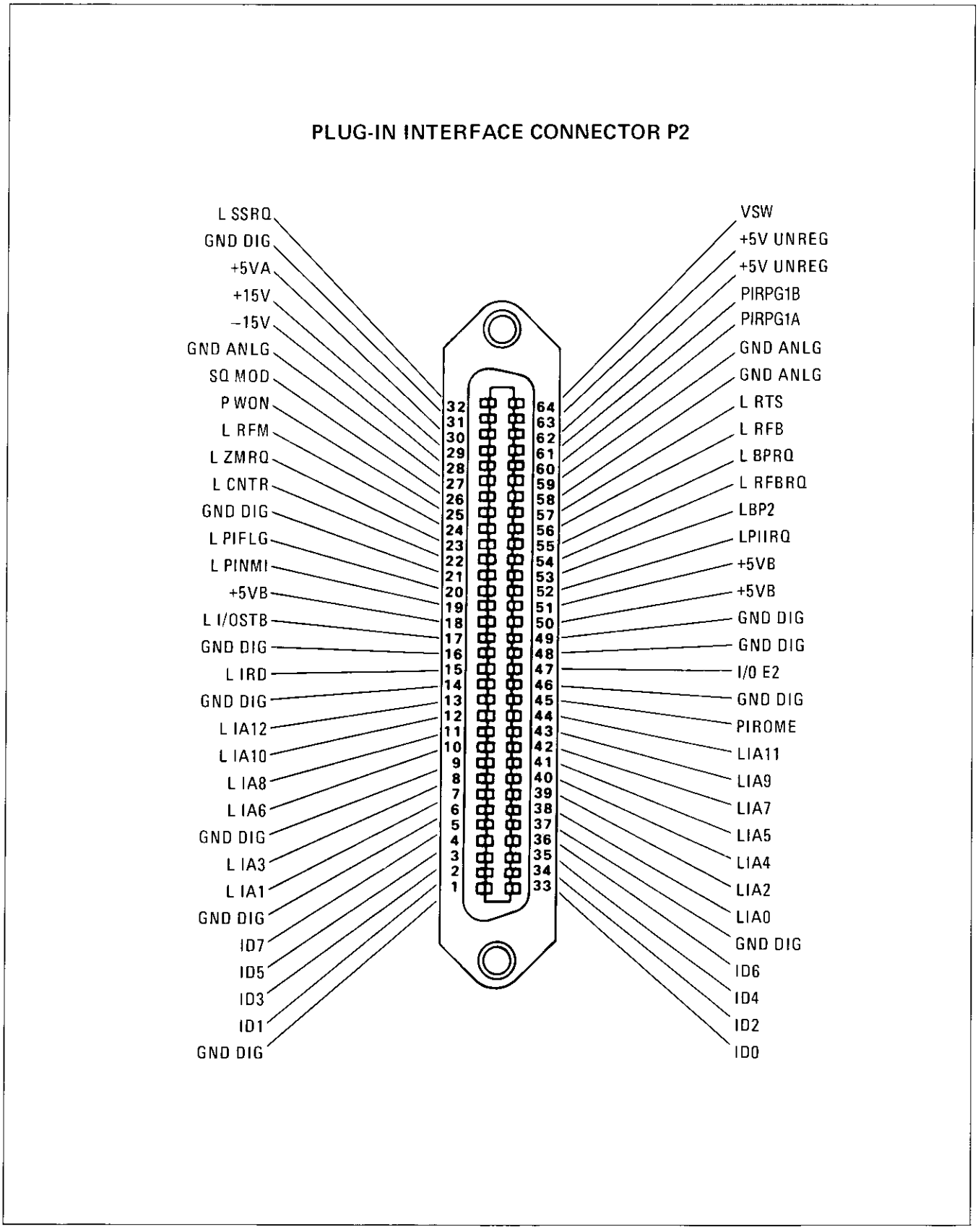


Figure 8-78. Interface Signals on Connector P2

Table 8-22. HP 83595A Cable List (1 of 2)

Cable	Description	Connections	
W1	Cable Assembly, Rigid RF, RF Out	DC2 J1	Directional Coupler Front Panel RF Output (Type-N)
W2	Cable Assembly, Coax. Blue	J2 A10J6	Front Panel EXT/MTR ALC Input Motherboard
W3	Cable Assembly, Ribbon, Front Panel	A10J1 A2J1	Motherboard Front Panel
W4	Cable Assembly, Ribbon, RF Section	A10J4 A12 A13	Motherboard SYTM YO
W5	Cable Assembly, Coax, White, Pulse In	J4 A10E9	Rear Panel BNC (PULSE IN) Motherboard
W6	Cable Assembly, Coax, Red, Pulse Mod	A10E8 A16	Motherboard Modulator/Splitter
W7	Cable Assembly, Coax, Orange, Vtune	P1-A1 A10E7	Rear Panel Interface Motherboard
W8	Cable Assembly, Coax, Gray	CR1 A10E6	Detector (Bands 1 through 4) Motherboard
W9	Cable Assembly, Coax, Blue, FM	A10E5 A12A1J2	Motherboard YO (FM Coil)
W10	Cable Assembly, Coax, Purple	DC1 A10E4	Directional Detector Motherboard
W11	Cable Assembly, Coax, Green, FM In	A10E3	Motherboard
W12	Cable Assembly, Coax, Brown, AM In	P1-A4 A10E2	Rear Panel Interface Motherboard
W13	Cable Assembly, Coax, Yellow, Mod 1	A10E1 A16	Motherboard Modulator/Splitter
W14	Cable Assembly, Ribbon, RF Section	A10J5 A14A1J1 A16A1	Motherboard Power Amplifier (2.3 to 26.5 GHz) Modulator/Splitter
W15	Cable Assembly, Rigid RF	A12 DC2	SYTM Directional Coupler
W16	Cable Assembly, Rigid RF	AT1 A12	Isolator SYTM
W17	Cable Assembly, Rigid RF	A14 AT1	Power Amplifier (2.3 to 26.5 GHz) Isolator

Table 8-22. HP 83595A Cable List (2 of 2)

Cable	Description	Connections	
W18	Cable Assembly, Rigid RF	DC1 A15	Directional Detector DC Return
W19	Cable Assembly, Rigid RF	A17 DC1	Amplifier (0.01 to 2.4 GHz) Directional Detector
W20	Cable Assembly, Rigid RF	A16 A14	Modulator Splitter Power Amplifier (2.3 to 26.5 GHz)
W21	Cable Assembly, Rigid RF	A16 A18	Modulator/Splitter Modulator/Mixer
W22	Cable Assembly, Rigid RF	A11 A18	Cavity Oscillator Modulator/Mixer
W23	Cable Assembly, Rigid RF	A18 A17	Modulator/Mixer Amplifier (0.01 to 2.4 GHz)
W24	Cable Assembly, Rigid RF	A15 A12	DC Return SYTM
W25	Cable Assembly, Rigid RF	A13 A16	YO Modulator/Splitter
W26	Cable Assembly, Rigid RF	A16 J3	Modulator/Splitter Rear Panel Type-N (AUX OUTPUT)
W27	Cable Assembly, RF Section	A16A1 A11 A17 A18 DC1	Modulator/Splitter Cavity Oscillator Amplifier (0.1 to 2.4 GHz) Modulator/Mixer Directional Detector
W28	Cable Assembly, Power Supply	P1 A10J3	Rear Panel Interface Motherboard
W29	Cable Assembly, Ribbon	P2 A3J3 A10J2 J5	Rear Panel Interface Digital Interface Board Motherboard Rear Panel BNC (1V/0.5V/GHz Output)

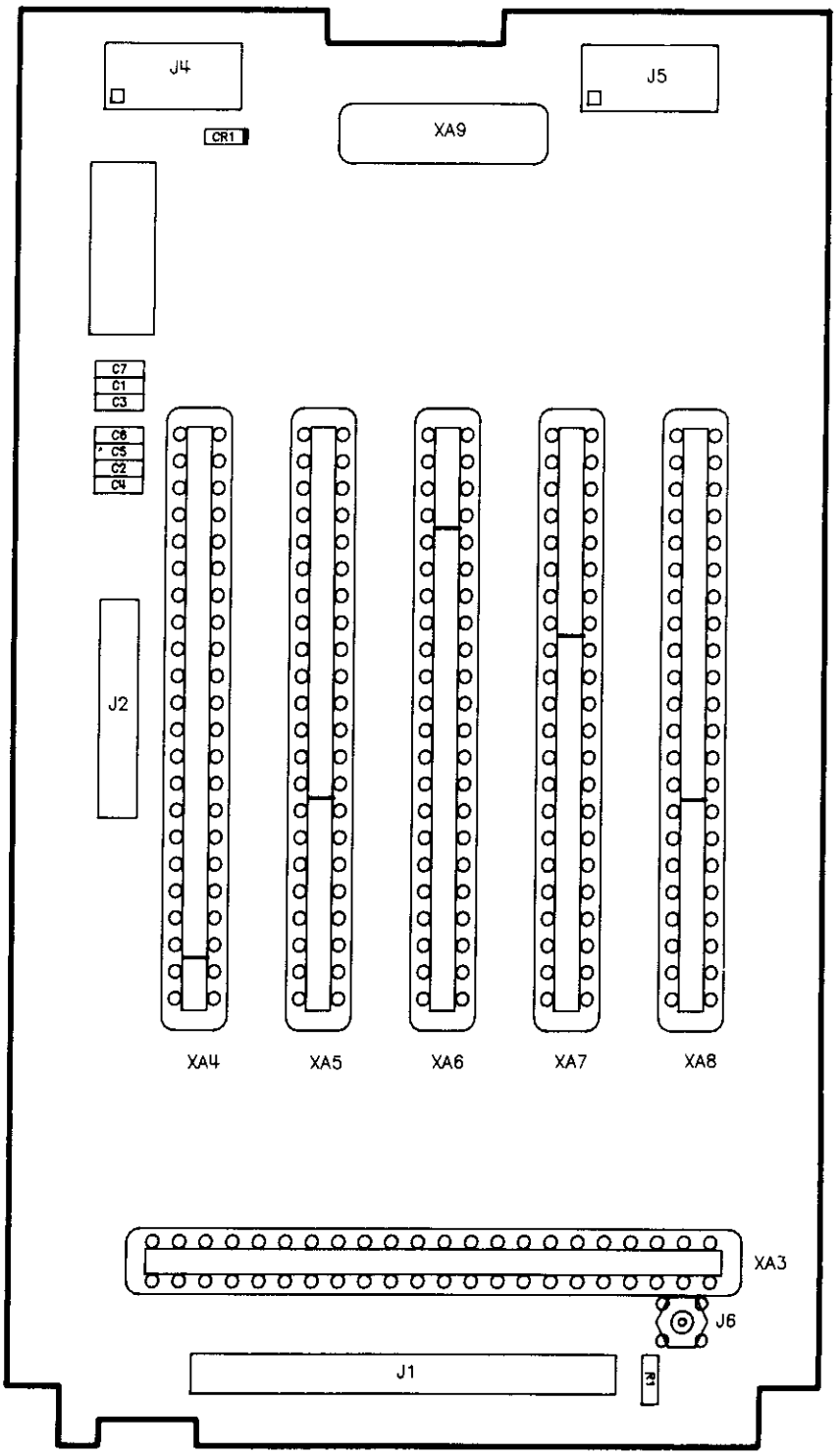


Figure 8-79. A10 Motherboard, Component Locations

Table 8-23. HP 83595A Motherboard Wiring List (1 of 3)

Mnemonic	Signal Source	Mnemonic Description	Power Supply Interface P1	Plug-in Interface P2	—Dig Intfc— A3P1	A3J1	ALC A4P1	FM A5P1	Sweep Control A6P1	SYTM A7P1	YO A8P1	Ref. Resistor A9P1	F.P. Interface A10J1	P/O Plug-in Interface A10J2	Power Supply Interface A10J3	YO/SYTM Ribbon Cable A10J5	RF Ribbon Cable A10J4	Miscellaneous
AM	P1-A4	Amplitude Modulation	A4-C				4											E2-C[1]
L AMP OFF	None	L=Amplifier Off (Not Used)															8	
BAND 0 AMP	A6P1-19	Band 0 RF Amplifier Enable							19								7	
BA0	A3P1-33	Buffered Addr 0			33		33	33	33	33	33		11					
BA1	A3P1-11	Buffered Addr 1			11		11	11	11	11	11							
BA2	A3P1-34	Buffered Addr 2			34		34	34	34	34	34							
BA3	A3P1-12	Buffered Addr 3			12		12	12	12	12	12							
BD0	A3P1-31	Buffered Addr 0			31		31	31	31	31	31		5					
BD1	A3P1-9	Buffered Addr 1			9		9	9	9	9	9		3					
BD2	A3P1-32	Buffered Addr 2			32		32	32	32	32	32		7					
BD3	A3P1-10	Buffered Addr 3			10		10	10	10	10	10		9					
BD4	A3P1-35	Buffered Addr 4			35		35	35	35	35	35		15					
BD5	A3P1-13	Buffered Addr 5			13		13	13	13	13	13		13					
BD6	A3P1-36	Buffered Addr 6			36		36	36	36	36	36		19					
BD7	A3P1-14	Buffered Addr 7			14		14	14	14	14	14		17					
L BPRQ	A6P1-2	L=Blanking Pulse Request							2					4				
L BP2	P2-53	L=Blanking Pulse		53	44	42			15									
BVTUNE	A6P1-42	Buffered Tune Voltage							42	25	25		49					
L CNTR	P2-22	L=Counter Trigger (Not Used)		22														
EXT DET	A10J6	External Leveling Input					23											J6-C[1]
EXT DET RET	A10J6	External Leveling Return					1											J6-S[2]
EXT CAL	A10J1-41	External Leveling Power Cal					24						41					
FLAG	A10J1-31	Front Panel Flag			42								31					
FM IN	P1-A3	Frequency Modulation Input	A3-C[1]						40									E3-C[1]
FM IN RET	P1-A3	Frequency Modulation Return	A3-S[2]						39,41									E3-S[2]
L FP1	A3P1-15	L=F.P. Display Write			15								21					
L FP2	A3P1-37	L=F.P. Keyboard Read			37								23					
L FP3	A3P1-16	L=F.P. Annunciator Write			16								25					
L FP4	A3P1-26	L=F.P. Annunciator Write			26								6					
L FP5	A3P1-30	L=F.P. RF Control			30								1					
FREQ CAL	A10J1-37	Band 0 Freq Cal									23		37					
FREQ TRK V	A10J1-36	Freq Tracking Voltage					26	24					36					
HI FREQ FM	A5P1-21	YO FM Coil Drive						21										E5-C[1]
HI FREQ FM RET	A5P1-20,22	YO FM Coil Return						20,22										E5-S[2]
L IA0	P2-38	Instr Bus — Inv Addr 0		38		12												
L IA1	P2-7	Instr Bus — Inv Addr 1		7		13												
L IA2	P2-39	Instr Bus — Inv Addr 2		39		14												
L IA3	P2-8	Instr Bus — Inv Addr 3		8		15												
L IA4	P2-40	Instr Bus — Inv Addr 4		40		16												
L IA5	P2-41	Instr Bus — Inv Addr 5		41		18												
L IA6	P2-10	Instr Bus — Inv Addr 6		10		19												
L IA7	P2-42	Instr Bus — Inv Addr 7		42		20												
L IA8	P2-11	Instr Bus — Inv Addr 8		11		21												
L IA9	P2-43	Instr Bus — Inv Addr 9		43		22												
L IA10	P2-12	Instr Bus — Inv Addr 10		12		23												
L IA11	P2-44	Instr Bus — Inv Addr 11		44		24												
L IA12	P2-13	Instr Bus — Inv Addr 12		13		25												
ID0	P2-33	Instr Bus — Data 0		33		2												
ID1	P2-2	Instr Bus — Data 1		2		3												
ID2	P2-34	Instr Bus — Data 2		34		4												
ID3	P2-3	Instr Bus — Data 3		3		5												
ID4	P2-35	Instr Bus — Data 4		35		6												
ID5	P2-4	Instr Bus — Data 5		4		7												
ID6	P2-36	Instr Bus — Data 6		36		8												
ID7	P2-5	Instr Bus — Data 7		5		9												

1. Coaxial Cable
2. Shielded Cable
* Not used on this assembly

Table 8-23. HP 83595A Motherboard Wiring List (2 of 3)

Mnemonic	Signal Source	Mnemonic Description	Power Supply Interface P1	Plug-in Interface P2	—Dig Intfc— A3P1	—Dig Intfc— A3J1	ALC A4P1	FM A5P1	Sweep Control A6P1	SYTM A7P1	YO A8P1	Ref Resistor A9P1	F.P. Interface A10J1	P/O Plug-in Interface A10J2	Power Supply Interface A10J3	YO/SYTM Ribbon Cable A10J5	RF Ribbon Cable A10J4	Miscellaneous
L INST1	A3P1-8	L=Plug-In Control			8		18	5	18									
L INST2	A3P1-29	L=Plug-In Control			29					18	18							
INT DET 0	J4-5	Band 0 RF Detector					21											E4-C[1]
INT DET 1	CR1	Band 1 RF Detector					20											E6-C[1]
INT DET RET	CR1	Band 1 RF Detector Return					42											E6-S[2]
I/O E2	P2-47	Plug-In I/O Enable		47		30												
L I/OSTB	P2-17	Inv I/O Strobe		17		33												
L IRD	P2-15	L=Instr Bus Read		15		29												
MOD 0	A4P1-44	Band 0 RF Modulation					44											16
MOD 1	A4P1-19	Bands 1 to 3 RF Modulation					19		6									E1-C[1]
MOD DRIVE	A4P1-22	Modulator Drive (Not Used)					22											
L PIFLG	A3A10J1-39	L=Plug-In Flag		20		39												
L PIIRQ	A3A10J1-40	L=Plug-In Interrupt Request		52		40												
L PINMI	(NC)	L=Plug-In Non-Maskable Interrupt		19														
PIN SW	A6P1-29	PIN Diode Switch for SYTM							29							15		
PIROME	P2-45	Plug-In ROM Enable		45		26												
PIRPGA	A10J1-35	Plug-In RPG A		60									35	14				
PIRPGB	A10J1-34	Plug-In RPG B		61									34	16				
PULSE IN	J5(BNC)	External Pulse Input							26									E9-C[1]
L PULSE	A6P1-25	L=RF Pulse Mod					41		25									
PULSE MOD	A6P1-44	Pulse Modulation							44									E8
PWON	P2-25	Power On		25	22				5				29	7				
PWR REF	A4P1-3	Power Level Reference (Not Used)					3											
PWR SW/COMP	A5P1-23	Power Sweep, Level Compensation					5	23										
L RFB	P2-56	L=RF Blanking		56			29							6				
L RFBRQ	A6P1-24	L=RF Blanking Request		54					24					2				
L RFM	P2-24	L=RF Marker		24					40					5				
L RFON	A10J1-38	−10V=RF On; 0V=RF Off											38			6	14	
L RTS	P2-57	L=Retrace Strobe		57					1					8				
SCAN CLK	A3P1-38	F.P. Scan Clock			38								27					
L SIRQ	A6P1-3	L= Sweep Interrupt Request			18				3									
SQMOD	P2-26	Square Modulation (27.8,1.0 kHz)		26			40							9				
SRD BIAS	A6P1-22	Step Recovery Diode Bias							22							14		
L SSRQ	A6P1-23	L=Stop Sweep Request		32					23	5	5			21				
SYTM BASE	A7P1-21	SYTM Current Drive Control								21		9						
SYTM COIL	A7P1-22	SYTM Coil Current								22		8				8		
SYTM COLLECTOR	A7P1-20	SYTM Ref Resistor Sense								20		10						
UNL LAMP EN	A6P-16	Unleveled Lamp Enabled							16				4					
L UNLVL	A4P1-2	L=Unleveled					2		4				12					
VSW	P2-64	Sweep Voltage		64				25						22				
VTUNE	P1-W7	Tune Voltage	A1-C[1]						20									E7-C[1]
VTUNE RET	P1-W7	Tune Voltage Return	A1-S[2]						21									E7-S[2]
YO BASE	A8P1-21	YO Current Drive Control									21	1						
YO COIL	A8P1-22	YO Coil Current									22	4				4, 11		
YO COLLECTOR	A8P1-20	YO Ref Resistor Sense									20	2						
YO LO FM	A5P1-2	YO Low Freq FM (Main Coil)						2			1							
SYTM DRIVE V	A7P1-23	SYTM Drive Voltage								23			39					
SYTM LO FM	A5P1-1	SYTM Low Frequency FM						1		1								
1V/GHz	A10J1-50	1V per GHz Output											50	23				J4(BNC)
−10V REF	A8P1-3	−10V Reference Voltage					43		39	3	3							
+20V FREQ REF	A9P1-5	+20V Frequency Reference Sense								44	44	5						

1. Coaxial Cable
2. Shielded Cable
* Not used on this assembly

Table 8-23. HP 83595A Motherboard Wiring List (3 of 3)

Mnemonic	Signal Source	Mnemonic Description	Power Supply Interface P1	Plug-in Interface P2	—Dig Intfc— A3P1	—Dig Intfc— A3J1	ALC A4P1	FM A5P1	Sweep Control A6P1	SYTM A7P1	YO A8P1	Ref Resistor A9P1	F.P. Interface A10J1	P/O Plug-in Interface A10J2	Power Supply Interface A10J3	YO/SYTM Ribbon Cable A10J5	RF Ribbon Cable A10J4	Miscellaneous
+20V +20V RET +20V RET SENSE +20V SENSE	P1-7 P1-14 P1-6 P1-15	+20V Regulated +20V Return +20V Return Sense +20V Sense	7 14 6 15				16	16	16	16	16	3, 11	42		7 14 6 15	3, 9	2, 10	C7
+15V	P2-29	+15V Regulated		29			38	38	38	38	38			15				C6
+10V ±10V RET	P1-8 P1-3, 16	+10V Regulated ±10V Return	8 3, 16				7	7	7	7	7		46		8 3, 6		15	C5
+5V +5VA +5VB +5V REG +5V UNREG	A3P1-6,7 P2-30 P2-18,50,51 A9P1-7 P2-63	+5V Internal for RF Plug-In +5V for 8350 +5V for RF Plug-In +5V Regulated +5V Unregulated		30 18,50,51 63	6,7	35,36,38	27	27	27	27	27	7 12	2	18, 20		7	3, 11	C4
−10V −10V RET SENSE −10V SENSE −10V UNREG	P1-13 P1-12 P1-4 P1-5	−10V Regulated −10V Return Sense −10V Sense −10V Unregulated	13 12 4 5				17	17	17	17	17		40		13 12 4 5	10	5	C3
−15V	P2-28	−15V Regulated		28			28	28	28	28	28			13				C2
−40V −40V RET −40V RET SENSE −40V SENSE	P1-11 P1-1 P1-10 P1-2	−40V Regulated −40V Return −40V Return Sense −40V Sense	11 1 10 2				6,39			6,39	6,39				11 1 10 2	12,16	6	C1
GND ANLG	W28P1-8 P2-27,58,59	Analog Ground					15,37	15,37	37,41 43	15,19 24,26, 29,37	15,19 24,26, 29,37	6	48	10,11 12,24	10,12,14 16,1,3,6	1,2 13	1,9	C1-C7, R1
GND DIG	P2-1,6,14, 16,21,31, 37,46,48,49	Digital Ground		1,6,14, 16,21,31, 37,46,48,49	4,5		8,30	8,30	8,30	8,30	8,30		8					R1
GND SENSE	W28P1-4	Analog Ground Sense													4			

1. Coaxial Cable
2. Shielded Cable
* Not used on this assembly

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